

FIG. 1A
PRIOR ART

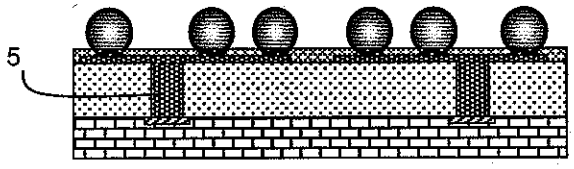

FIG. 1B
PRIOR ART

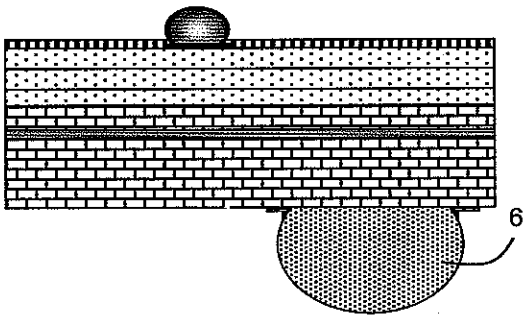

FIG. 1C
PRIOR ART

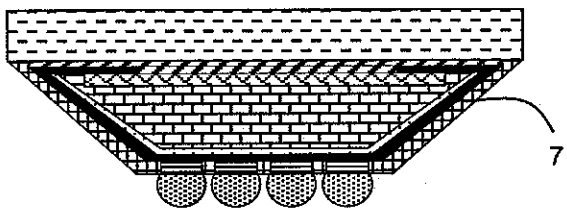

FIG. 1D
PRIOR ART

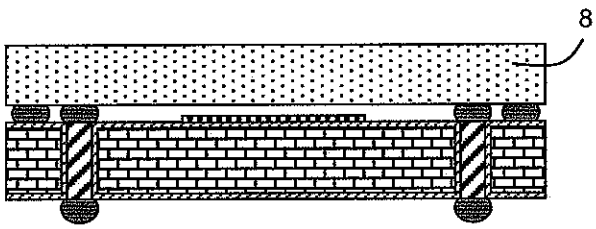

FIG. 1E
PRIOR ART

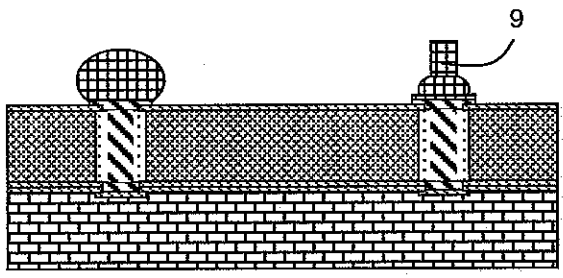

FIG. 1F
PRIOR ART

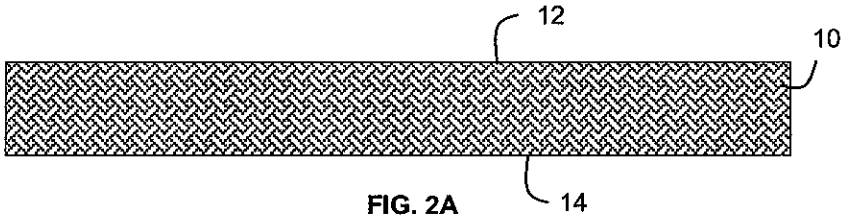

FIG. 2A

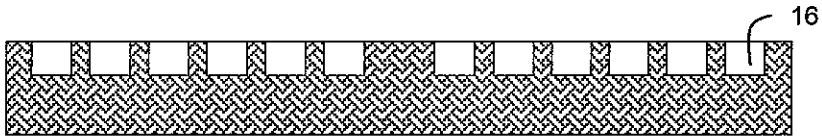

FIG. 2B

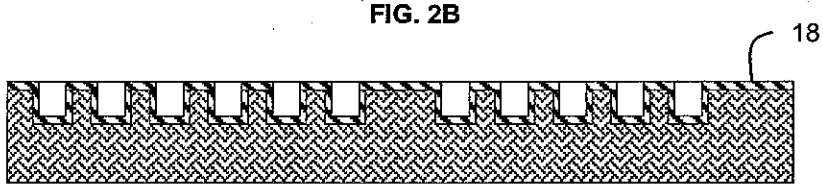

FIG. 2C

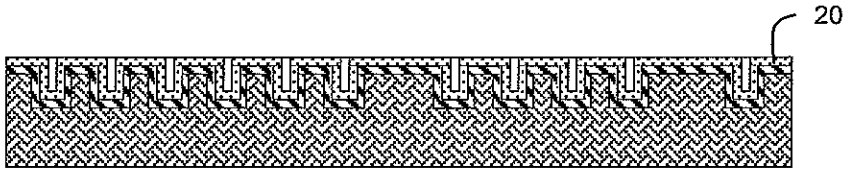

FIG. 2D

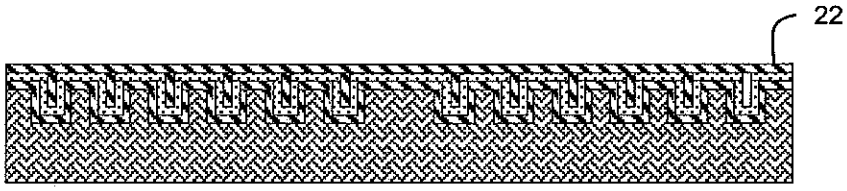

FIG. 2E



FIG. 2F

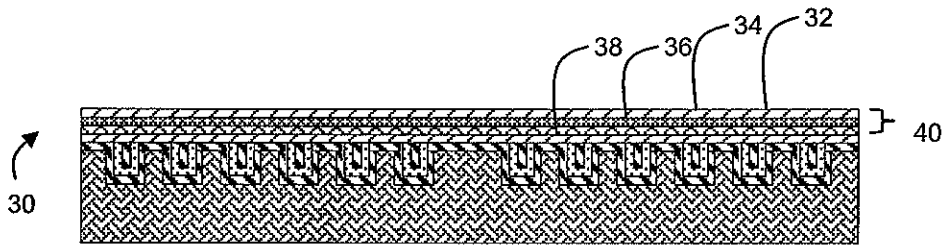

FIG. 2G

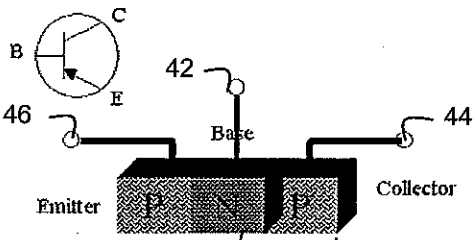

FIG. 3A

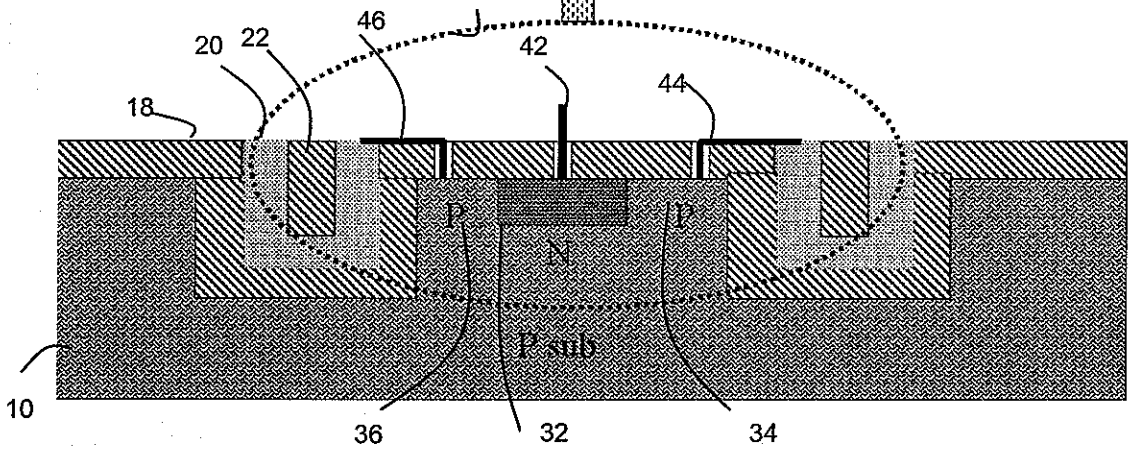

FIG. 3B

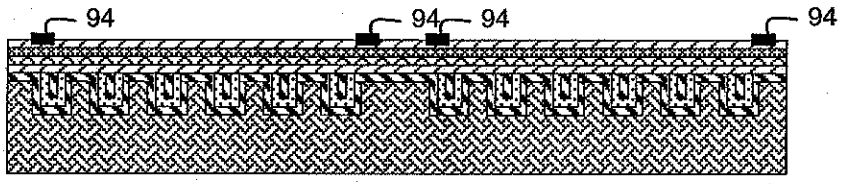

FIG. 2H

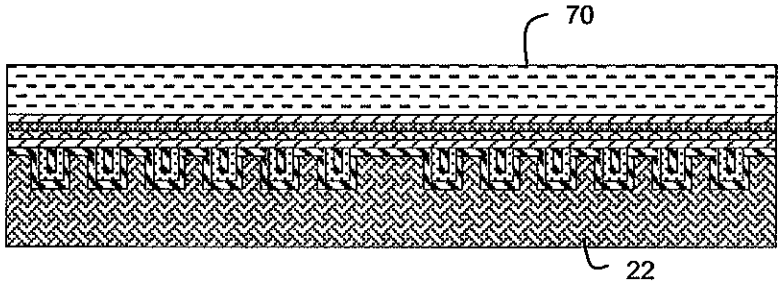

FIG. 2I

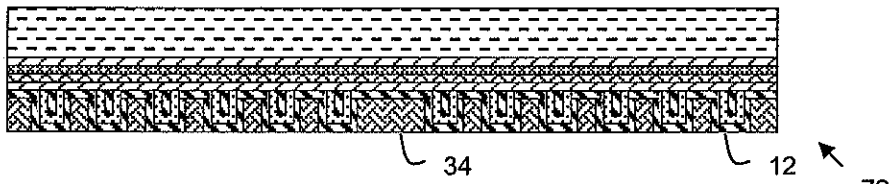

FIG. 2J

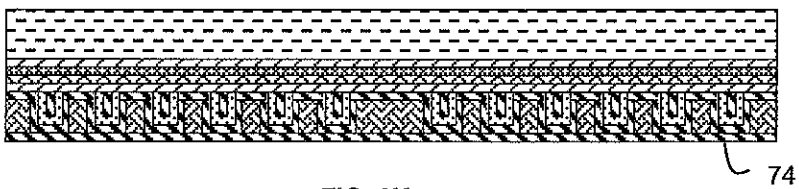

FIG. 2K

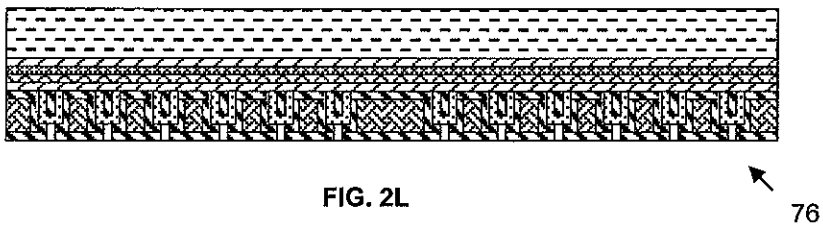

FIG. 2L

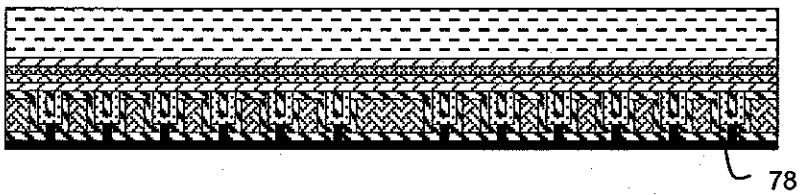

FIG. 2M

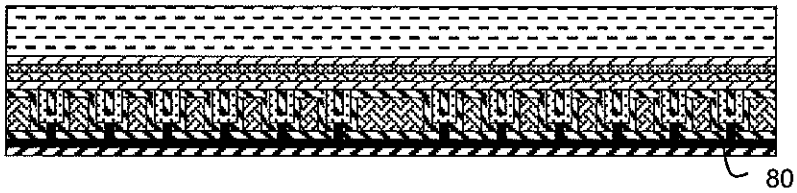

FIG. 2N

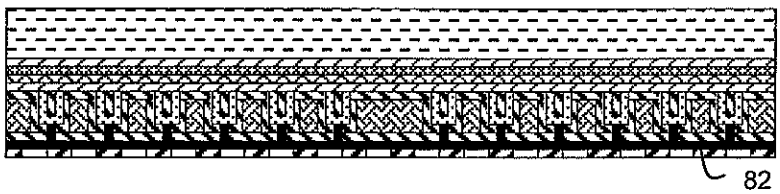

FIG. 2O

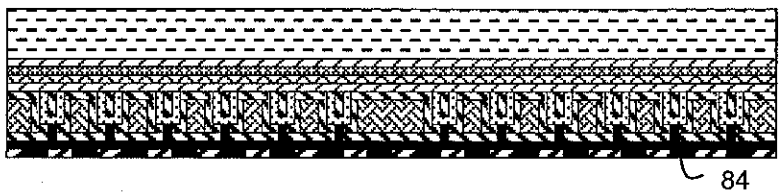

FIG. 2P

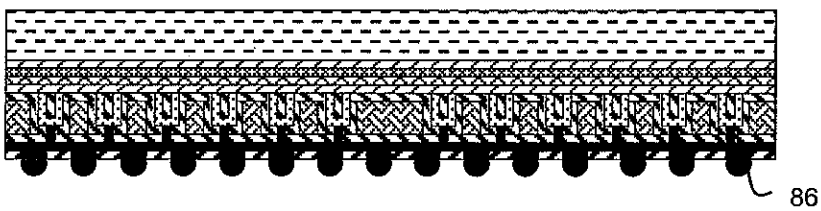

FIG. 2Q

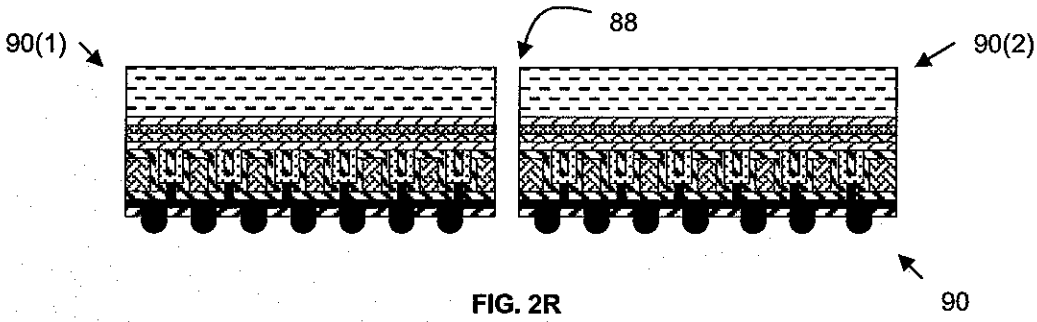

FIG. 2R

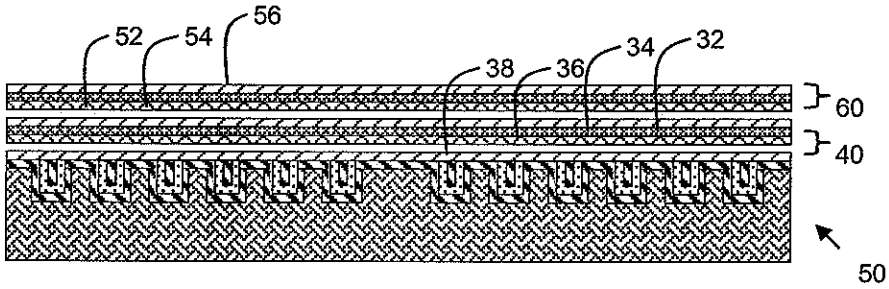

FIG. 5

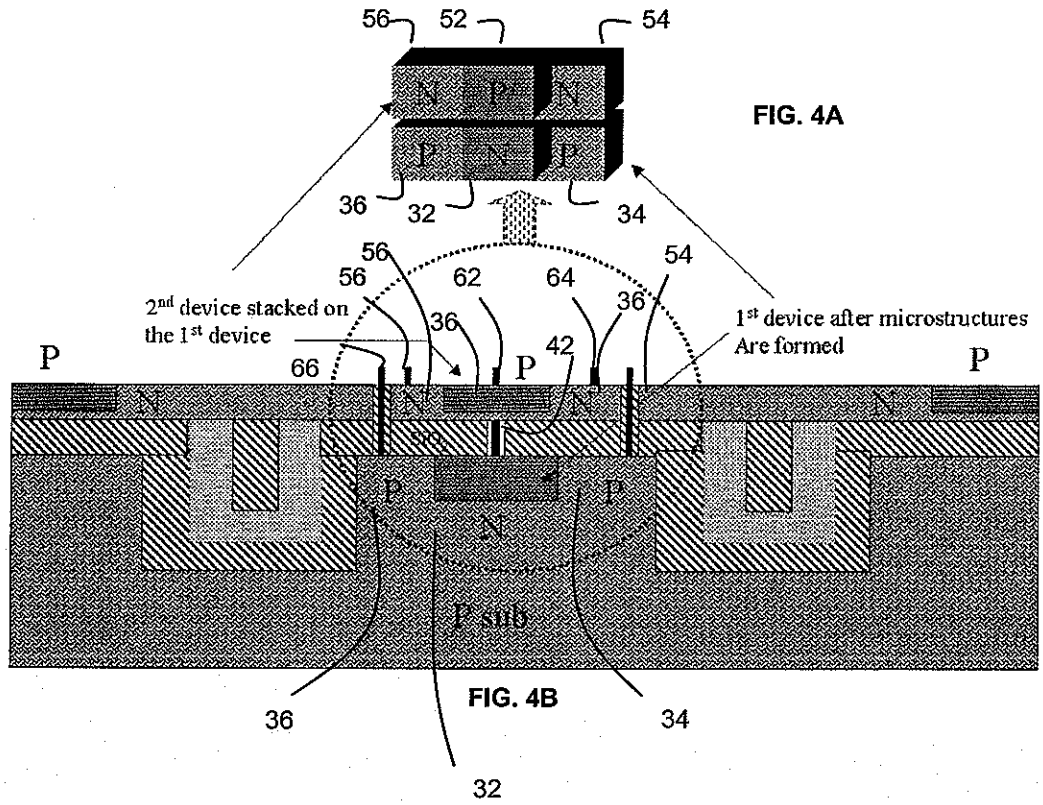

FIG. 4A

FIG. 4B

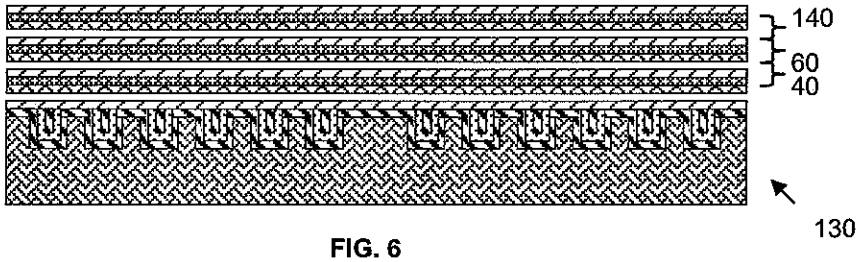

FIG. 6

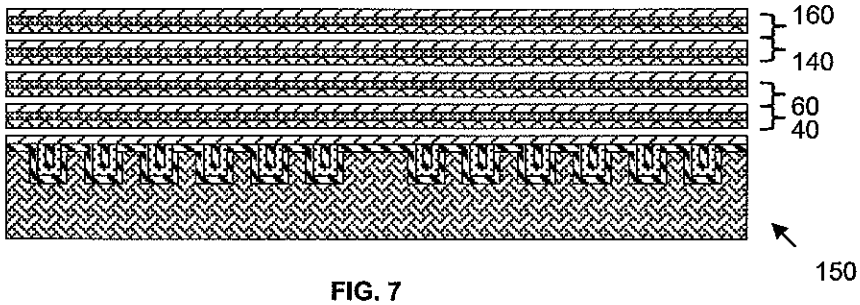

FIG. 7

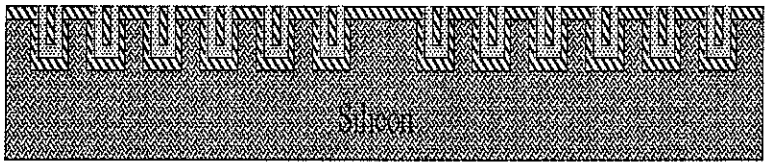

FIG. 8A

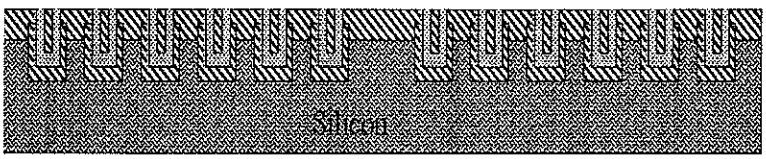

FIG. 8B

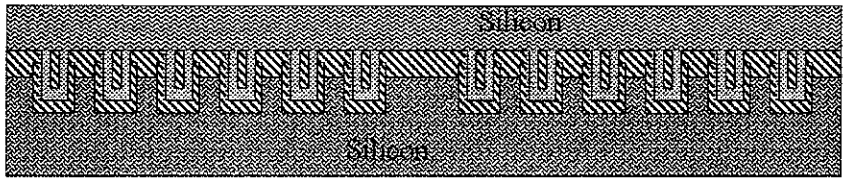

FIG. 8C

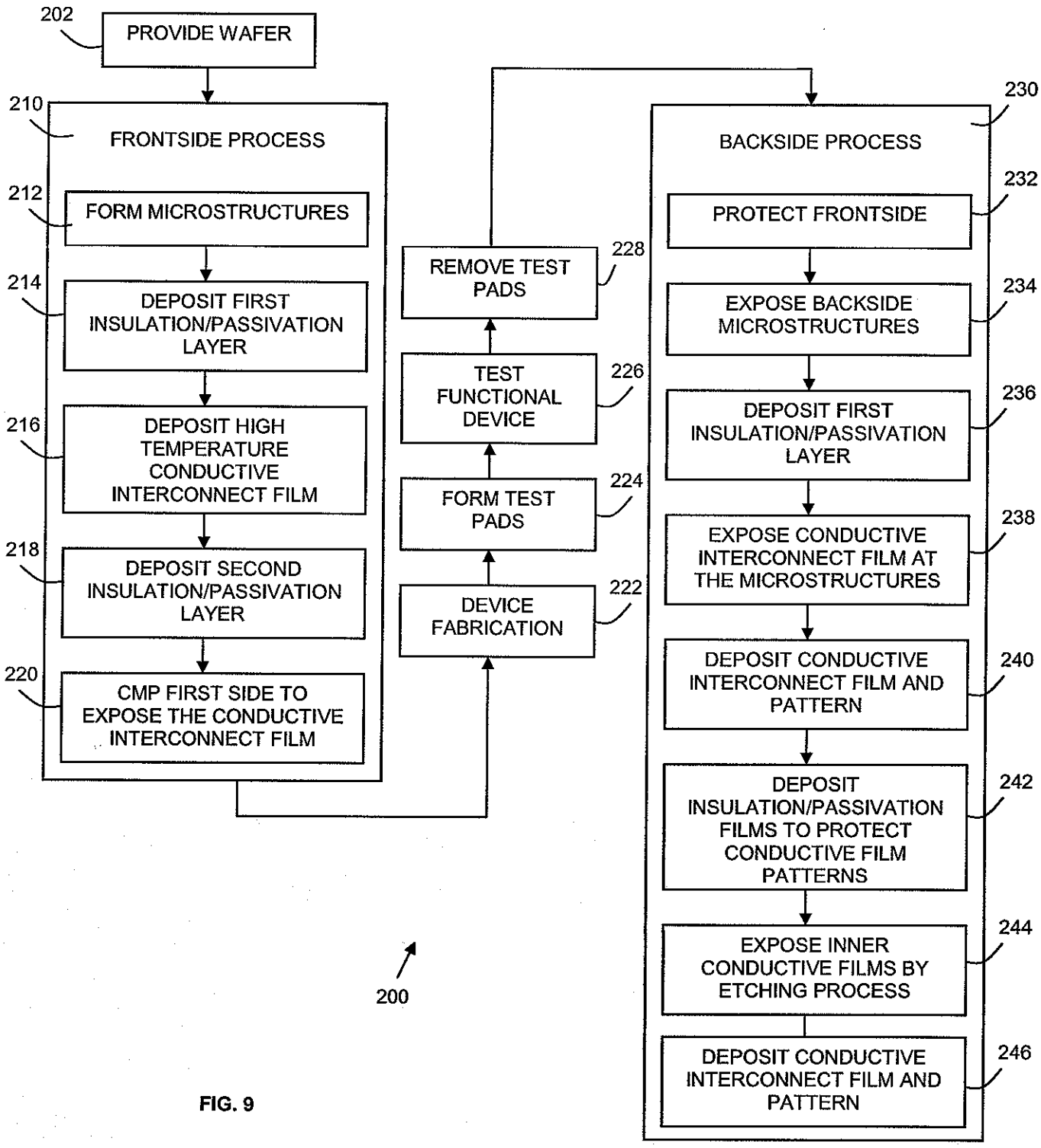
202
PROVIDE WAFER
210
FRONTSIDE PROCESS
212
FORM MICROSTRUCTURES
214
DEPOSIT FIRST INSULATION/PASSIVATION LAYER
216
DEPOSIT HIGH TEMPERATURE CONDUCTIVE INTERCONNECT FILM
218
DEPOSIT SECOND INSULATION/PASSIVATION LAYER
220
CMP FIRST SIDE TO EXPOSE THE CONDUCTIVE INTERCONNECT FILM
222
DEVICE FABRICATION
224
FORM TEST PADS
226
TEST FUNCTIONAL DEVICE
228
REMOVE TEST PADS
230
BACKSIDE PROCESS
232
PROTECT FRONTSIDE
234
EXPOSE BACKSIDE MICROSTRUCTURES
236
DEPOSIT FIRST INSULATION/PASSIVATION LAYER
238
EXPOSE CONDUCTIVE INTERCONNECT FILM AT THE MICROSTRUCTURES
240
DEPOSIT CONDUCTIVE INTERCONNECT FILM AND PATTERN
242
DEPOSIT INSULATION/PASSIVATION FILMS TO PROTECT CONDUCTIVE FILM PATTERNS
244
EXPOSE INNER CONDUCTIVE FILMS BY ETCHING PROCESS
246
DEPOSIT CONDUCTIVE INTERCONNECT FILM AND PATTERN
200

FIG. 9