



Converter circuit

The invention relates to a converter circuit consisting of a first transistor to whose base an input signal can be supplied, a second transistor which is complementary to the first transistor and whose base is connected to the emitter of the first transistor and whose emitter is connected via a first resistor to an output terminal and including a current supply circuit which ensures a substantially equal flow of current through the emitter - collector paths.

A converter circuit of this type is known from DE 30 35 471 C2. The circuit illustrated there in Figure 3 thus consists of two emitter followers connected together in cascaded manner. Due to the positive temperature coefficients of the bipolar transistors used, the quiescent current in the complementary stages has to be stabilised by the first resistor forming a current feedback coupling. As a result of this, there is a voltage drop across the feedback resistor which is dependent on the output current and this thereby leads to a reduction in the voltage modulation since the control voltage swing is greater than the swing of the output voltage. The emitter follower of this arrangement thus does not have the properties demanded of an ideal impedance converter, namely, a very low output resistance that is roughly zero. In a known circuit arrangement, the disadvantage of the limited, very low value output resistance is frequently compensated by means of a heavy feedback coupling over all the stages (voltage and current amplifier stages) of the converter.

Furthermore, one has tried to reduce the negative effect of the current feedback resistor at the latter itself e.g. by bridging the resistor with diodes, by current discharge circuits or quad bridge circuits. However, each of these circuits always requires expensive means for stabilising the quiescent current, selected transistors and (in the case of the quad circuit), a circuit concept that requires heavy outlay to dimension it properly. The diode bridging only works from a voltage of 0.6 V, the quiescent current having to be under 0.6 V, so that the setting of the quiescent current cannot be freely selected. For complementary

amplifiers, there are transfer distortions in the Class A or AB modes. The current discharge circuits only permit of an approximation to zero for the output resistance at relative great expense.

The circuit concept mentioned hereinabove has the advantage that mutually inverse emitter followers, which are traversed by basically equal currents, effect a compensation of the non-linear characteristic curves of the transistors. The known circuit concept is regularly employed for non-distorting amplifiers but cannot be formed as an impedance converter that approximates to the ideal.

The object of the invention is to develop a converter circuit of the type mentioned hereinabove such that an output resistance of practically zero can be achieved and wherein the control characteristic curve distortions are fully compensated.

This object is achieved in accordance with the invention in the case of a converter circuit of the type mentioned hereinabove by means of a second resistor which is connected to the emitter of the first transistor and is traversed by the collector-emitter current of the first transistor and via which the emitter of the first transistor is connected to the base of the second transistor.

Due to the introduction of the resistor in accordance with the invention into the connection between the emitter of the first transistor and the base of the second transistor so that the emitter-collector current of the first transistor flows through the second resistor, there is an automatic compensation of the voltage drop across the first resistor acting as a current feedback resistor, in that the voltage on the base of the second transistor is exactly compensated by the voltage drop across the first resistor when the two resistors are of equal size. In addition, by suitably dimensioning the second resistor relative to the first resistor, positive or negative output resistances of the converter can be set up as desired.



Obviously, safeguarding measures have to be provided in the case of a negative output resistance.

The compensation is limited due to the different polarity of the input and output transistor and the different working points connected therewith in the case of equal currents.

In order to produce a complete symmetry of the characteristic curves between the input and output transistors in the case of equal currents, a respective complementary transistor, which is connected as a diode, is added in series with each of them as a compensating resistor. The two characteristic curves (transistor and diode) produce, when put together, a new control characteristic curve which is the same for both sides and can be completely compensated.

The current supply circuit preferably comprises a known current mirror including two transistors whose bases are interconnected.

A particularly advantageous embodiment of the circuit in accordance with the invention can be realised in that, the two transistors of the current mirror exhibit a different polarity so that they exhibit the same polarity as the respective first and second transistor which is associated therewith and traversed by the same current. In this case namely, it is possible to form the respective two transistors which are traversed by the same current as identical double transistors on a common substrate whereby similar properties and similar characteristic curves are ensured for the two transistors.

It can be expedient thereby, if the first transistor, together with the second resistor and the transistor of the current mirror appertaining thereto, has a configuration including two like-poled transistors and a resistor connected therebetween, the configuration for the second transistor, together with an intermediately connected resistor and the transistor of the current mirror appertaining thereto, being implemented inversely. In this way, the circuit concept in accordance with the invention can be formed using two double transistors.



The converter circuit in accordance with the invention may be formed as a complementary converter circuit, whereby the components used, double in number in inverse and mirror-like manner. In this embodiment, four similar configurations may form the successively connected arms of a bridge. A fully symmetrical arrangement having exactly the same formation in each arm of the bridge can be achieved in that a respective resistor, whose value corresponds to the first resistor, is connected into each arm of the bridge. The first resistor, which acts as a feedback resistor, is then also integrated into the bridge circuit.

The working-point setting of the converter is selectable by a bias voltage source which is connected to the base of the second transistor. In the complementary construction of the converter circuit, the bias voltage source is arranged between the bases of the mutually inverse second transistors.

However, the bias voltage source may also take the form of a linear resistor or of a voltage dependent resistor in a quiescent current limiting sub-path of the circuit.

The circuit in accordance with the invention permits an internally, freely selectable quiescent current to be set without disturbing the symmetry of the circuit.

The technique used for the circuit in accordance with the invention permits universal modules having ideal properties to be realised. In particular, it is possible to realise ideal transistor arrangements wherein the vertical symmetry of the current branches formed by the first and the second transistors is of decisive significance.

The invention will be explained in more detail hereinafter by means of the embodiments illustrated in the drawing. Therein

Figure 1: shows a complementary impedance converter circuit

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Figure 2A: a schematic illustration of the basic construction of an impedance converter circuit including a current mirror consisting of two similar transistors (horizontal symmetry)

Figure 2B: a variant using additional complementary transistor-diodes that produce a horizontal symmetry

Figure 3: a variant of the circuit in accordance with Figures 2A and B including a current supply circuit having complementary transistors that produce a vertical symmetry

Figure 4: a schematic illustration of the circuit in accordance with Figure 3 having pairs of transistors assembled on a common substrate

Figure 5A: a complementary impedance converter constructed according to the principles of Figures 3 and 4 including a current discharge means and a quiescent current sub-path internally of the circuit.

Figure 5B: a complementary impedance converter constructed according to the principles of Figures 3 and 4 using a doubly symmetrical quiescent current feed

Figure 5C: a complementary impedance converter constructed according to the principles of Figure 2B including similar, but non-linear resistors and an active transistor bias voltage source in the current limiting sub-path

Figure 5D: a complementary impedance converter constructed according to the principles of Figures 3 and 4 using an active bias voltage source

Figure 6: a universal transistor module constructed using the circuit techniques of Figures 3 and 4

Figure 7A: a module using lateral pnp transistors

Figure 7B: a module having a Darlington output circuit

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Figure 7C: a module in accordance with Figure 6 using a hybrid technique

Figure 7D: a module in accordance with Figure 6 using MOSFET techniques without additional resistors in the output circuit

Figure 8A: an integrated, power Darlington transistor

Figure 8B: a discrete construction for the control stage and the current discharge means

Figure 8C: a compensated source follower

Figure 8D: a current discharged source follower

Figure 9: a pnp transistor module

Figure 10: an npn transistor module

Figure 11: a universally employable integrated circuit

Figure 12: a dual circuit using complementary techniques

Figure 13: a transistor module including a current discharge circuit

Figure 14: a circuit having the same effect but which is modified vis a vis Figure 13

In the embodiment illustrated in Figure 1, an input signal terminal A is connected to a tap on a potentiometer P supplying the input signal. The base of a first bi-polar transistor T1 which is in the form of an npn transistor, and the base of an inverse (pnp) transistor T1', are connected to the input signal terminal A. The emitter of the transistor T1 is connected to the base of a second transistor T2 which is (likewise) connected up as an emitter follower and its emitter is connected via a first resistor R1 to an output terminal B. A second resistor is

connected into the connection between the emitter of the first transistor T1 and the base of the second transistor T2.

The current supply to the two transistors T1 and T2 is effected by a current mirror which consists of two transistors T3 and T4 which have their bases connected to one another. Their emitters are connected via a respective emitter resistor R3 and R4 to a negative supply voltage D. The transistor T4 of the current mirror associated with the second transistor T2 is connected up as a diode, i.e. there is a direct connection between its collector and its base. This known current mirror causes equal currents to flow through the two transistors T1 and T2. The collector of the first transistor T1 is connected thereby to a positive supply voltage D+. The voltage dropped across the first resistor R1, which varies with the signal being transferred, is added to the output signal with exactly the same magnitude if the second resistor R2 is selected to be equal in size to the first resistor R1. Since equal currents flow through the two resistors R1, R2, equal voltages are dropped across them. The input signal voltage, which is present on the emitter of the first transistor T1, would be reduced by the voltage dropped across the first resistor R1 without the second resistor R2. The signal voltage is increased by the voltage dropped across the resistor R1 due to the increase in voltage across resistor R2, so that the voltage E- on the base of the second transistor T2 corresponds to the negative signal voltage increased by the voltage drop across the resistor R2 (or R1). Thus, by virtue of the circuit arrangement in accordance with the invention, not only are the non-linear diode paths of the two transistors T1, T2 mutually compensating but so too are the voltage drops across the resistors R1, R2 when these are selected to be equal large. An impedance converter having an output resistance of zero can thus be realised in this way. If the resistance is selected as $R2 < R1$, then a positive output resistance will remain while the output resistance will be negative if $R2 > R1$ is selected.

The circuit arrangement illustrated in Figure 1 is a complementary arrangement. The half of the circuit provided for the positive signal voltage corresponds to the half of the



circuit described for the negative signal voltage and is identified by corresponding reference numerals supplemented by " ' " .

Zener diodes ZD1, ZD1' are arranged between the respective supply voltages D+ and D- and the appertaining bases of the transistors T3, T4 of the current mirror, the diodes limiting the maximum current through the transistors T1, T2 or the transistors T3, T4 in the event for example that a short circuit should occur on the output terminal.

A Zener diode ZD2 connected between the bases of the two second transistors T2 and T2' defines the working point on the characteristic curves of the two transistors T2, T2'. A resistor R5 connected to the collectors of the two transistors T4, T4' forms a quiescent current sub-path and permits a quiescent current to flow when the circuit is switched on.

Figure 2A illustrates the basic circuit which was embodied in Figure 1. The two transistors T3, T4, which are as similar as possible, form the current mirror and cater for equally large currents through the transistors T1, T2 which are arranged to be mutually complementary.

In order to achieve the wanted result for each working point of the circuit, not only do the characteristic curves of the transistors T3, T4 have to be the same but so too do the characteristic curves of the complementary transistors T1, T2. The circuit is thus based on having horizontal symmetry between the pairs of transistors T3, T4 and T1, T2. Adherence to this condition for symmetry can only be approximated to by the complementary transistors T1, T2.

Figure 2B shows how the input and output transistors are supplemented by a respective complementary diode-transistor (T5, T6). Due to the connection of two different diode paths in series, the same control characteristic curve results on both sides in the case of horizontal symmetry of the transistor and the diode-transistor. The circuit is constructed to be



horizontally symmetrical and achieves a complete compensation of the distortions in the control characteristic curves in the case where the transistors have been manufactured with sufficient accuracy.

Figure 3 shows a variant of the circuit in accordance with Figure 2 which is based on another functional concept. The transistors T11 and T12 are connected together in the same way as the transistors T1 and T2 in the circuit in accordance with Figure 2. A transistor T13 is arranged in series with the collector - emitter path of the transistor T11 in a similar manner to the transistor T3 in Figure 2. In contrast however, a transistor T14 having another polarity than the transistor T13 is connected from its emitter via the resistor R4 to the collector of the transistor T12. In the case of this circuit construction, there results a vertical symmetry since the transistors T11 and T13 have the same polarity namely, they are constructed as pnp transistors, and the transistors T12 and T14 as npn transistors. Figure 4 makes it clear that the pnp transistors T11, T13 are expediently assembled on a common chip so that they can exhibit an exactly similar characteristic curve behaviour relative to one another. The npn transistors T12, T14 are assembled on a same chip in a similar manner. The resistors R1, R2, R3, R4 may likewise be similarly assembled in pairs so that there ensues an arrangement having complete vertical symmetry. The functional concept of this circuit is now no longer based on there being completely equal currents flowing through the two transistors T1, T2 due to the current mirror, but rather, on the basis that, due to the vertical symmetry, the connections occur in the form of a bridge in which there exist equal partial-path voltages so that, vis a vis the reference potential, the input voltage occurring on the base of the transistor T11 is equal to the output voltage occurring across a load resistor L. Completely different currents may thereby flow through the two respective current branches T11, T13 and T12, T14 without disturbing the compensation process for the non-linear characteristic curves of the transistors T11 to T14. Here, the resistors R1 to R4 have to be appropriately dimensioned for the different currents. The circuits in



accordance with Figure 3 and 4 thus use "current mirrors" constructed in complementary manner and they are based on a vertically symmetrical construction in which the similar npn transistors subject to faults on the one side are exactly compensated by two npn transistors which are subject to (in general, other) faults, but which too are similar, on the other side.

Figure 5A shows a circuit which corresponds in substance to the circuit construction in accordance with Figure 1 wherein however, the principle of the circuit in accordance with Figure 3 and 4 is implemented. A frequency dependent regenerative feedback compensation is effected by a respective capacitor C_1 , C_1' that is connected in parallel with the respective Zener diode ZD_1 , ZD_1' . The complementary impedance converter can be relieved of the load current, and thus simply serve as a control circuit, by means of a load current mirror formed by two transistors T_{15} , T_{16} and T_{15}' , T_{16}' respectively. The current source I_1 in a current sub-path of the circuit caters for a quiescent current occurring in the circuit only when the supply voltage (U_b) is switched on. In the on state, the current from the current source I_1 flows via the complementary current mirrors (T_{13} , T_{14} ; T_{13}' , T_{14}') into the bias voltage source ZD_2 .

Figure 5B shows how one can avoid having an additional quiescent current loading of the complementary current mirrors which would destroy the vertical symmetry. The two equally weighted current sources (I_2 , I_2') feed the current directly into the bias voltage source ZD_2 .

A lesser low-impedance component, such as a simple resistor for example, may also be employed for the bias voltage source ZD_2 since a limiting quiescent current feedback circuit exists here. The resistor can only accept as much current as is fed in externally via the current sources (I_2 or I_1). Any further increase in the voltage across the resistor is coupled with a withdrawal of current from the circuit which manifests itself as a lowering of the efficiency of the regenerative feedback in the



whole circuit. This manner of procedure stabilises the quiescent current.

An offset trimming can also be effected by means of the current sources.

Figure 5C shows a circuit which was implemented in accordance with Figure 2B. The linear resistors are replaced by field effect transistor-diodes which are non-linear as regards their voltage - current characteristics. Voltage dependent resistors, which are similar to one another as regards their characteristic curves and the internal resistance associated therewith, are achieved in this manner. The symmetry is maintained.

The reason for the use of non-linear resistors lies in the asymmetrical voltage and current distribution between the upper and lower part of the complementary circuit. In the case of equal voltage swings internally of the circuit in the upper and lower parts of the circuit during a modulation of the signal, there is a higher current gain, by some orders of magnitude, in the (e.g.) upper part of the circuit than is effected thereby in the form of a reduction in current in the lower part. The circuit operates in a dynamically extended Class A region and so needs a lower quiescent current for a certain output power. The bias voltage source ZD2 is implemented as a diode path in the quiescent current limiting sub-path of the circuit.

Figure 5D shows an active, thermally coupled transistor bias voltage source (T7, T8) in a circuit in accordance with Figure 5B. The transistor bias voltage sources represent a steeply voltage controlled resistor which is controlled by the voltage via the two base terminals of the complementary transistors. An excessive quiescent current increase or increase in current is leaked off via the collector leads, also in correspondingly excessive manner, into a sub-path, possibly of the bias voltage source.

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The circuit arrangement in accordance with the invention with its strict vertical symmetry opens up ways for universal application.

Figure 6 shows an unwired module whose circuitry corresponds to Figure 3. The connection of the supply voltage terminal U_b of the first transistor (T_{11} , T_{14}) to the emitter of the second transistor (T_{12} , T_{13}) saves one external terminal on the module.

The base terminal B_p of the transistor T_{14} may thereby be wired up as the base of an npn transistor arrangement. Due to the interconnection of the collector C_n and the base B_n of the transistor T_{11} (C_n) to the emitter terminal of the transistor T_{12} at the free end of the resistor R_1 (E_p) and the collector of the transistor T_{14} (C_p) to the emitter terminal of the transistor T_{13} on the other side of the resistor R_3 (E_n), these two mergers form the emitter and the collector of the npn transistor.

The module in accordance with Figure 6 may be used as a pnp transistor in a similar manner whereby the base of the transistor T_{11} (b_n) is used as the base input.

The remaining terminals of the universal structure in accordance with Figure 6 may be used for the purposes of compensation and trimming.

The Figures 7A to 7D show modules having maintained upright vertical symmetry that are put together in various combinations. Figure 7D shows a corresponding module using MOSFET techniques including corresponding field effect transistors FT_{11} to FT_{14} and an output circuit without any auxiliary resistors. This is possible in the case of a sufficiently high internal resistance of the transistor source and sufficient similarity of the characteristic curves of the two transistors (FT_{11} , FT_{13}).

The universal module in accordance with Figure 6 can also be realised without any complications using hybrid techniques, wherein the two field effect transistors FT_{11} and FT_{13} are combined with two bipolar transistors T_{12} and T_{14} into a module



for example, since, under the conditions of vertical symmetry, one is concerned exclusively with the amplifying components that are connected together in series being identical.

The Figures 8A to 8D show different power transistor applications wherein the universal circuit serves both as a control stage for a load current source that basically operates non-linearly as well as for the purposes of control voltage de-emphasis for a power emitter or source follower.

Two special transistor circuits using pnp and npn techniques are shown in Figures 9 and 10. The two circuits are distinguished merely by virtue of the complementary formation of the transistors T11 to T14. They form synthetic linear transistor equivalent arrangements.

Figure 11 shows the universal structure illustrated in Figure 6 in the form of an integrated circuit having symmetrically arranged Zener diodes ZD1 and ZD3 as protection diodes.

The complementary, doubled arrangement of the circuit in accordance with Figure 11 leads to the circuit illustrated in Figure 12 which is not pre-wired and hence has 20 terminals available. Naturally, the number of terminals can be reduced without difficulty by pre-wiring it internally.

It can be perceived that the structures illustrated in the Figures 6 to 12 can be used universally and open up a multiplicity of ways in which they can be employed merely in dependence on the external wiring. In particular, ideal transistors i.e. transistors that have a lossless output voltage, can be realised, the transistors being fully compensated in respect of their characteristic-curves and the temperature while maintaining the vertical symmetry in accordance with Figures 3 and 4. The ways in which modules of this type may be utilised and their advantages may be inferred without any further explanation.

It is immediately possible to construct the transistors in accordance with Figures 9 and 10 directly as power transistors

in which the transistors T13 and T14 are formed as a Darlington circuit and are thus suitable for power purposes. Thereby, it is obviously equally possible to form the transistors T11 and T12 as Darlington circuits in order to thus produce a completely Darlington-type structure which leads to an internal reduction of the base current.

Figure 13 shows a synthetic transistor equivalent structure which is constructed using a converter circuit such as is illustrated in principle in Figure 3. This forms a base terminal B at the base of the transistor T11 and an emitter terminal E at its collector. A collector terminal C is decoupled from the converter circuit via a further current mirror T15, T16. A supply voltage U_B is supplied to the current mirror via a special terminal. The transistor structure including the terminals B, E and C arising therefrom allows equal settings of the quiescent voltage potentials on all three terminals B, E and C.

Figure 14 likewise shows a transistor equivalent structure including the terminals B, E and C wherein the current discharge is undertaken by means of a transistor T 16' which forms a current mirror together with the transistor T14. The transistor T14 is thus doubly utilised for two current mirrors T13, T14 and T14, T16'. A capacitive collector interaction relative to the converter circuit takes place via the collector - base capacitance of the transistor T16'.

The modules illustrated in the Figures 13 and 14 permit of a voltage amplification process in which the amplified voltage can be taken off at the same potentials as the input potentials so that a plurality of stages can be connected directly in series.

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Claims

1. Converter circuit consisting of a first transistor (T1, T1'; T11, T11'; FT11) to whose base an input signal can be supplied, a second transistor (T2, T12'; T12, T12'; FT12) which is complementary to the first transistor (T1, T1'; T11, T11'; FT11) and whose base is connected to the emitter of the first transistor (T1, T1'; T11, T11'; FT11) and whose emitter is connected via a first resistor (R1) to an output terminal (B) and including a current supply circuit (T3, T4; T3', T4'; T13, T14; T13', T14'; FT13, FT14) which controls the current flow through the emitter - collector paths of the two transistors (T1, T1'; T11, T11'; FT11; T2, T2'; T12, T12'; FT12), characterised by a second resistor (R2, R2') which is connected to the emitter of the first transistor (T1, T1'; T11, T11'; FT11) and which is traversed by the collector-emitter current of the first transistor (T1, T1'; T11, T11'; FT11) and via which the emitter of the first transistor (T1, T1'; T11, T11'; FT11) is connected to the base of the second transistor (T2, T2'; T12, T12'; FT12).
2. Converter circuit in accordance with Claim 1, characterised in that, the second resistor (R2, R2') and the first resistor (R1, R1') are supplemented in series by a respective complementary transistor (T5, T6; T5', T6') which is connected as a diode.
3. Converter circuit in accordance with Claim 1 and 2, characterised in that, the current supply circuit comprises a current mirror including two transistors (T3, T4; T3', T4'; T13, T14; T13', T14'; FT13, FT14) whose bases are interconnected.
4. Converter circuit in accordance with Claim 1 to 3, characterised in that, the transistors of the current mirror exhibit the same polarity as the respective first and second transistor (T1, T1'; T11, T11'; FT11; T2, T2'; T12, T12'; FT12) which is associated therewith and is traversed by the same current.

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5. Converter circuit in accordance with Claim 1 to 4, characterised in that, the two transistors, which are respectively traversed by the same current, are formed as similar double transistors on a common substrate.
6. Converter circuit in accordance with Claim 5, characterised in that, each of the mutually symmetrically oriented transistors and their resistors are formed on a common substrate.
7. Converter circuit in accordance with any of the Claims 1 to 6, characterised in that, the second resistor (R_2 , R_2') is dimensioned relative to the first resistor (R_1 , R_1') and produces a positive output resistance in the case of $R_1 > R_2$, a negative output resistance in the case of $R_1 < R_2$ and an output resistance of zero in the case of $R_1 = R_2$.
8. Converter circuit in accordance with any of the Claims 1 to 7, characterised in that, the resistors of the current mirror (R_3 , R_4 ; R_3' , R_4') are dimensioned relative to one another and determine the output resistance.
9. Converter circuit in accordance with any of the Claims 1 to 8, characterised in that, the resistors (R_1 , R_4 ; R_2 , R_3), which are traversed vertically by the same current, are dimensioned relative to one another and determine the output resistance.
10. Converter circuit in accordance with any of the Claims 1 to 9, characterised in that, the axially symmetrical resistors are non-linear voltage dependent resistors having similar characteristic curves.
11. Converter circuit in accordance with any of the Claims 1 to 10, characterised in that, the resistors are bridged by an axis of symmetry.
12. Converter circuit in accordance with any of the Claims 1 and 4 to 11, characterised in that, the first transistor, together with the second resistor and a transistor of the current mirror appertaining thereto, form a configuration having two like-poled





transistors and a resistor connected therebetween, the configuration for the second transistor, together with an intermediately connected resistor and a transistor of the current mirror appertaining thereto, being implemented inversely.

13. Converter circuit in accordance with Claim 12, characterised in that, a respective resistor, whose value corresponds to the first resistor (R_1 , R_1'), is connected into each arm of the bridge.

14. Converter circuit in accordance with any of the Claims 1 to 13, characterised in that, it is formed as a complementary converter circuit.

15. Converter circuit in accordance with any of the Claims 5 to 14, characterised in that, four similar configurations are connected together in the form of a bridge, wherein two mutually inverse configurations form respective, successively connected arms of the bridge.

16. Converter circuit in accordance with any of the Claims 1 to 15, characterised by a bias voltage source (ZD_1 , ZD_1') for limiting the power dissipation which is connected between the base and emitter resistor of the transistors (T_2 , T_2' ; T_{12} , T_{12}' ; FT_{12}).

17. Converter circuit in accordance with Claim 14, characterised in that, the bias voltage source (ZD_2) for setting the quiescent current is arranged between the bases of the mutually inverse second transistors (T_2 , T_2' ; T_{12} , T_{12}' ; FT_{12}).

18. Converter circuit in accordance with Claim 14 and 17, characterised in that, the bias voltage source for setting the quiescent current is a linear resistor in the limiting quiescent current sub-path.

19. Converter circuit in accordance with Claim 14 and 17, characterised in that, the bias voltage source for setting the

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quiescent current is a voltage dependent resistor in the limiting quiescent current sub-path.

20. Converter circuit in accordance with Claim 14 and 17, characterised in that, an active bias voltage source forms a quiescent current feedback path.

21. Converter circuit in accordance with Claim 14 and 17 and 19 to 20, characterised in that, the bias voltage source is thermally coupled directly to the circuit.

22. Converter circuit in accordance with Claim 14 and 17 to 21, characterised in that, the quiescent current is initiated by a current source in a current sub-path of the circuit.

23. Converter circuit in accordance with Claim 14 and 17 to 21, characterised in that, the quiescent current is initiated by additionally feeding in two similarly dimensioned current sources from both sides of the voltage supply.

24. Converter circuit in accordance with Claim 14 and 17 to 23, characterised in that, the quiescent current is defined by variable current sources.

25. Converter circuit in accordance with any of the Claims 1 to 24, characterised in that, the supply voltage (U_B) can be supplied via a current discharge circuit (T_{15} , T_{16} ; T_{13} , $T_{16'}$).

26. Converter circuit in accordance with Claim 25, characterised in that, the current discharge circuit is formed by a current mirror.

27. Converter circuit in accordance with any of the Claims 1 to 26, characterised in that, in each case, it forms a synthetic linear transistor equivalent arrangement having transistor terminals (B , E , C , U_B).

28. Converter circuit in accordance with Claim 27, characterised in that, the transistor terminals (U_B and E) are connected.

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29. Converter circuit in accordance with Claim 25 or 26 and 27, characterised in that, the collector terminal (C) of the transistor equivalent arrangement is decoupled in respect of voltage via the current discharge circuit (T15, T16; T13, T16').

30. Converter circuit in accordance with Claims 1 to 29, characterised in that, the transistor arrangement described forms a universal transistor equivalent arrangement that is termed a "Synthetic Linear Transistor", in short an "SLT".

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