ABSTRACT

REDUCED LEAKAGE DRAM MEMORY CELLS WITH VERTICALLY ORIENTED NANORODS AND MANUFACTURING METHODS THEREOF

Methods and structures are described for reducing leakage currents in semiconductor memory storage cells. Vertically oriented nanorods may be used in the channel region of an access transistor. The nanorod diameter can be made small enough to cause an increase in the electronic band gap energy in the channel region of the access transistor, which may serve to limit channel leakage currents in its off-state. In various embodiments, the access transistor may be electrically coupled to a double-sided capacitor. Memory devices according to embodiments of the invention, and systems including such devices are also disclosed.

FIGURE 1C