DESCRIPTION

METHOD OF FORMING FIELD EFFECT TRANSISTORS AND METHODS OF FORMING INTEGRATED CIRCUITY COMPRISING A TRANSISTOR GATE ARRAY AND CIRCUITY PERIPHERAL TO THE GATE ARRAY

TECHNICAL FIELD

This invention relates to fabrication of field effect transistors and components thereof.

BACKGROUND ART

Field effect transistors are common devices utilized in integrated circuitry, for example in logic circuitry, memory circuitry and control circuitry for memory circuitry. Such devices typically comprise a pair of source/drain regions having a channel region received therebetween. A conductive gate is provided operably proximate the channel region, and is spaced therefrom by a gate dielectric region. Application of a suitable voltage to the conductive gate causes current flow between the source/drain regions through the channel region.

By way of example only, the conductive material of the gate might be formed above or over semiconductive material or within openings formed in the semiconductive material, and for example whether within bulk monocrystalline substrate material or within semiconductor-on-insulator material. When formed within trenches or other openings in semiconductive material, some of such are referred to as recessed access devices. Here, masking material is provided over the semiconductive material of the substrate and patterned to form gate line trenches within the substrate. With the trenches so formed, the masking material is removed, and then a gate dielectric is formed within the trench openings, for example by thermal oxidation of exposed semiconductive material within the trench. Gate material is then deposited to overfill the trenches. The gate material received outwardly of the trenches is then patterned, typically using photolithography and etch, to form desired gate outlines over the trenches within which the gate material is also received.

Typically, the gate material patterning forms the gate lines over the trenches to be very close to or of the same width as the underlying trenches. Photomask misalignment can undesirably place an edge of the desired gate line pattern within the lateral confines of the previously etched trench. This is highly undesirable, as the gate pattern etch can etch gate material within the trench, ultimately leading to circuitry failure or at least unacceptable device configuration and performance.

While the invention was motivated in addressing the above identified issues, it is in no way so limited. The invention is only limited by the accompanying claims as literally worded, without interpretative or other limiting reference to the specification, and in accordance with the doctrine of equivalents.

SUMMARY

The invention includes methods of forming field effect transistors, methods of forming field effect transistor gates, methods of forming integrated circuitry comprising a transistor gate array and circuitry peripheral to the gate array, and methods of forming integrated circuitry comprising a transistor gate array including first gates and second grounded isolation gates. In one implementation, a method of forming a field effect transistor includes forming masking material over semiconductive material of a substrate. A trench is formed through the masking material and into the semiconductive material. Gate dielectric material is formed within the trench in the semiconductive material. Gate material is deposited within the trench in the masking material and within the trench in the semiconductive material over the gate dielectric material. Source/drain regions are formed.

In one implementation, a method of forming a field effect transistor gate includes forming a silicon nitride-comprising masking material over semiconductive material of a substrate. A trench is formed through the silicon nitride-comprising masking material and into the semiconductive material. Silicon nitride of the masking material is removed after forming the trench into the semiconductive material. Prior to removing silicon nitride of the masking material, gate dielectric material is formed within the trench in the semiconductive

material. Gate material is deposited within the trench in the semiconductive material over the gate dielectric material.

In one implementation, a method of forming integrated circuitry comprising a transistor gate array and circuitry peripheral to the gate array includes forming masking material over semiconductive material of a substrate. Array circuitry trenches are formed through the masking material and into the semiconductive material. Array gate material is deposited within the array circuitry trenches in the masking material and within the array circuitry trenches in the semiconductive material. After depositing the array gate material, peripheral circuitry trenches are formed through the masking material. Peripheral circuitry gate material is deposited within the peripheral circuitry trenches within the masking material.

In one implementation, a method of forming integrated circuitry comprising a transistor gate array and circuitry peripheral to the gate array includes forming masking material over semiconductive material of a substrate. Array circuitry trenches are formed through the masking material and into the semiconductive material. Array gate material is deposited within the array circuitry trenches in the masking material and within the array circuitry trenches in the semiconductive material. Peripheral circuitry trenches are formed through the array gate material and through the masking material. Peripheral circuitry gate material is deposited within the peripheral circuitry trenches within the array gate material and within the masking material.

In one implementation, a method of forming field effect transistor gates includes forming masking material over semiconductive material of a substrate. The substrate comprises a trench isolation region. In a common masking step, a first trench is formed through the masking material and into the semiconductive material and a second grounded isolation gate trench is formed through the masking material over the trench isolation region. In a common deposition step, gate material is deposited within the first trench and second trench.

In one implementation, a method of forming integrated circuitry comprising a transistor gate array including first gates and second grounded isolation gates comprises forming masking material over semiconductive material of a substrate. The substrate comprises trench isolation regions. First trenches are formed

through the masking material and into the semiconductive material for the first gates. Second grounded isolation gate trenches are formed through the masking material over the trench isolation regions. Gate material is deposited within the first and second trenches.

Other aspects and implementations are contemplated.

BRIEF DESCRIPTION OF THE DRAWINGS

Preferred embodiments of the invention are described below with reference to the following accompanying drawings.

Fig. 1 is a diagrammatic sectional view of a semiconductor substrate fragment in process in accordance with an aspect of the invention.

Fig. 2 is a view of the Fig. 1 substrate fragment at a processing step subsequent to that shown by Fig. 1.

Fig. 3 is a view of the Fig. 2 substrate fragment at a processing step subsequent to that shown by Fig. 2.

Fig. 4 is a view of the Fig. 3 substrate fragment at a processing step subsequent to that shown by Fig. 3.

Fig. 5 is a view of the Fig. 4 substrate fragment at a processing step subsequent to that shown by Fig. 4.

Fig. 6 is a view of the Fig. 5 substrate fragment at a processing step subsequent to that shown by Fig. 5.

Fig. 7 is a view of the Fig. 6 substrate fragment at a processing step subsequent to that shown by Fig. 6.

Fig. 8 is a view of the Fig. 7 substrate fragment at a processing step subsequent to that shown by Fig. 7.

Fig. 9 is a view of the Fig. 8 substrate fragment at a processing step subsequent to that shown by Fig. 8.

Fig. 10 is a view of the Fig. 9 substrate fragment at a processing step subsequent to that shown by Fig. 9.

Fig. 11 is a view of the Fig. 10 substrate fragment at a processing step subsequent to that shown by Fig. 10.

Fig. 12 is a view of the Fig. 11 substrate fragment at a processing step subsequent to that shown by Fig. 11.

Fig. 13 is a view of the Fig. 12 substrate fragment at a processing step subsequent to that shown by Fig. 12.

Fig. 14 is a view of the Fig. 13 substrate fragment at a processing step subsequent to that shown by Fig. 13.

Fig. 15 is a diagrammatic sectional view of an alternate embodiment semiconductor substrate fragment in process in accordance with an aspect of the invention.

Fig. 16 is a view of the Fig. 15 substrate fragment at a processing step subsequent to that shown by Fig. 15.

Fig. 17 is a view of the Fig. 16 substrate fragment at a processing step subsequent to that shown by Fig. 16.

Fig. 18 is a diagrammatic sectional view of another alternate embodiment semiconductor substrate fragment in process in accordance with an aspect of the invention.

Fig. 19 is a view of the Fig. 18 substrate fragment at a processing step subsequent to that shown by Fig. 18.

Fig. 20 is a diagrammatic sectional view of still another alternate embodiment semiconductor substrate fragment in process in accordance with an aspect of the invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

The invention includes methods of forming field effect transistor gates, methods of forming field effect transistors, and methods of forming integrated circuitry comprising a transistor gate array and circuitry peripheral to the gate array. The discussion proceeds primarily with reference to forming integrated circuitry comprising a transistor gate array and circuitry peripheral to the gate array, while the artisan will appreciate aspects of the invention apply to forming a single field effect transistor as well as to multiple field effect transistors, and one or more field effect transistor gates thereof.

Referring initially to Fig. 1, a semiconductor substrate in process is indicated generally with reference 10. In the context of this document, the term "semiconductor substrate" or "semiconductive substrate" is defined to mean any

construction comprising semiconductive material, including, but not limited to, bulk semiconductive materials such as a semiconductive wafer (either alone or in assemblies comprising other materials thereon), and semiconductive material layers (either alone or in assemblies comprising other materials). The term "substrate" refers to any supporting structure, including, but not limited to, the semiconductive substrates described above. Substrate 10 is depicted as comprising an array area or region 12 within which a field effect transistor gate array will be fabricated and a peripheral circuitry area 14 peripheral to gate array area 12. By way of example only, array area 12 might be utilized for fabrication of memory circuitry, for example DRAM circuitry, while peripheral circuitry area 14 might include control circuitry for operating/controlling memory circuitry within array area 12. Alternate configurations are of course contemplated, for example utilizing gate arrays and field effect transistors within logic, control or other circuitries.

Substrate 10 is depicted as comprising semiconductive material 11, for example bulk monocrystalline silicon. Other semiconductive material substrates are also of course contemplated, for example semiconductor-on-insulator substrates, and whether existing or yet-to-be developed. Semiconductive material 11 is ideally suitably background doped, or doped to form a doped well, to be of a suitable conductivity type(s) and concentration(s). Exemplary preferred trench isolation regions 13, 15, 16, 17 and 18 have been fabricated relative to semiconductive substrate material 11.

Referring to Fig. 2, masking material 20 has been formed over semiconductive material 11 of substrate 10. Such is depicted as comprising an innermost pad oxide layer 22 (exemplary preferred thickness range of from 30 Angstroms to 100 Angstroms), a masking layer 24 of different composition to that of material 22 received over material 22 (a preferred exemplary thickness range being from 50 Angstroms to 300 Angstroms), and a masking layer 26 formed over and of different material to that of masking layer 24 (an exemplary preferred thickness range being from 1,000 Angstroms to 3,000 Angstroms). Some or all of masking material 20 might be sacrificial, thereby being ultimately removed from the substrate. Accordingly, some portions or all of

masking material 20 might be any of electrically insulative, semiconductive, or conductive. An exemplary preferred material for layer 24 is silicon nitride, while an exemplary preferred material for layer 26 is undoped silicon dioxide. A further exemplary alternate embodiment, and by way of example, forms layer 24 to comprise silicon dioxide and layer 26 to comprise silicon nitride. Regardless and accordingly in but only one preferred implementation, masking material 20 comprises silicon dioxide and silicon nitride, and in a more preferred embodiment comprises silicon dioxide received over silicon nitride.

In one preferred implementation, layer 26 can be considered as comprising an outer insulative material layer and layer 24 can be considered as comprising an inner insulative material layer, wherein the outer insulative material layer is selectively etchable relative to the inner insulative material layer, and independent of whether another insulative material layer (such as layer 22) is received inwardly of inner insulative material layer 24. In one preferred implementation, outer insulative material layer 26 is thicker than inner insulative material layer 24, and in one preferred implementation as shown, contacts inner insulative material layer 24. Further in the depicted exemplary embodiment, outer insulative material layer 26 is the outermost material of masking material 20 at least at the conclusion of its patterning. Further, layer 24 is preferably thicker than layer 22 in but one exemplary implementation.

Referring to Fig. 3, array circuitry trenches 28 have been formed through masking material 20. An exemplary preferred technique includes photolithographic patterning and etch using one or more photoresist or other layers (not shown). Fig. 3 depicts such photoresist or other layers as having been removed over masking material 20, although some or all of such might remain at the conclusion of the Fig. 3 processing where photolithography is utilized.

Referring to Fig. 4, masking material 20 has been utilized as a mask to form array circuitry trenches 30 into semiconductive material 11. Accordingly in one preferred embodiment, depicted trenches 28 and 30 are formed using a single masking step, for example utilizing photolithography. An exemplary

preferred depth range for trenches 30 within semiconductive material 11 from an outer surface thereof is from 300 Angstroms to 2,500 Angstroms.

Referring to Fig. 5, gate dielectric material 32 has been formed within trenches 30 in semiconductive material 11. In one preferred implementation, at least a majority of gate dielectric material 32 is formed by thermal oxidation of semiconductive material 11 within trenches 30. The depicted exemplary embodiment depicts essentially all of such gate dielectric material having been formed by thermal oxidation, although deposition of gate dielectric material with or without thermal oxidation of material 11 within array trenches 30 is also of course contemplated.

Referring to Fig. 6, array gate material 34 has been deposited within array circuitry trenches 28 within masking material 20 and within array circuitry trenches 30 within semiconductive material 11, and over gate dielectric material 32. Preferably, array gate material 34 is deposited to at least fill trenches 28 and 30, and most preferably to overfill such trenches and also depositing gate material 34 to cover masking material 20. Exemplary preferred materials 34 include conductively doped semiconductive materials, such as conductively doped polysilicon either *in situ* doped during deposition or subsequently. Other conductive materials might also be utilized, such as conductive metal or metal compounds but are not preferred at this point in the process.

Referring to Fig. 7, after depositing array gate material 34, peripheral circuitry trenches 36 have been formed through masking material 20 and, in the depicted embodiment where material 34 is received thereover, also through array gate material 34. Fig. 7 also depicts in one implementation fabrication of a grounded gate trench 37 through masking material 20 within array region 12, for example over one or more of the trench isolation regions. In the context of this document, a grounded gate is an isolation gate which is fabricated to be received over at least some field isolation and held at ground or other suitable potential for providing an isolation function towards precluding or reducing formation of parasitic field effect transistor current flow beneath or around field isolation regions. If desired, some or all of trenches 36, 37 might be fabricated to

etch/extend into material of semiconductive material 11 and/or field/trench isolation material.

Referring to Figs. 7 and 8, preferred embodiment trenches 36, 37 preferably expose semiconductive material 11 of substrate 10. Fig. 8 depicts one preferred implementation wherein a gate dielectric layer 38 is formed over exposed semiconductive material 11 within peripheral circuitry trenches 36. Such might be formed, by way of example only, by a thermal oxidation wherein at least a majority of the gate dielectric layer is comprised of oxidized semiconductive material (as shown). Such might also of course be combined with or substituted by deposition of a gate dielectric layer with or without thermal oxidation of substrate material 11. Further in the depicted exemplary embodiment, gate dielectric layer 38 also essentially forms over (and "on" as shown) array gate material 34, and will typically be subsequently removed from thereover as described below. Regardless, the gate dielectric material 38 might be the same or different as gate dielectric material 32 of the array circuitry trenches 30, thereby enabling optimization of gate dielectric for different areas of circuitry. A preferred manner of forming trenches 36 and 37 is in a single masking step common to the formation of both types of trenches, for example utilizing photolithography. In certain implementations, one or both of trenches 36 and 37 might not be formed at all, or at other times if formed, and which is described below by way of example only in possible likely alternative embodiments.

Regardless, Fig. 7 depicts one exemplary preferred embodiment wherein grounded gate trenches in the array and peripheral circuitry trenches are formed in the same masking step. Further, of course, grounded gate trenches might also be fabricated within peripheral circuitry area 14.

Referring to Fig. 9, peripheral circuitry gate material 40 has been deposited within peripheral circuitry trenches 36 within masking material 20, and in the depicted exemplary embodiment within the corresponding peripheral circuitry trenches also formed within array gate material 34. Gate material 40 might be the same as or different from material 34, thereby enabling optimization of conductivity type and/or work function of the conductive gate material being formed for different gates. Further in the depicted exemplary embodiment,

peripheral circuitry gate material 40 is also utilized in the fabrication of grounded gates, depositing also within grounded gate trenches 37. In the depicted exemplary preferred embodiment, peripheral circuitry gate material 40 is deposited to a thickness to at least fill, and preferably overfill, peripheral circuitry trenches 36 with peripheral circuitry gate material 40, and to at least fill, and preferably overfill, grounded gate trenches 37.

Referring to Fig. 10, array gate material 34, peripheral circuitry gate material 40, and dielectric layer 38 therebetween have been removed selectively relative to and outwardly exposes masking material 20 effective to isolate the respective gate materials within the respective trenches in masking material 20 and in semiconductive material 11 where such are so formed. In the context of this document, a selective removal requires removal (for example by etching or other means) at a rate which removes one material relative to another at 2:1 or greater. In the depicted exemplary embodiment, such removing has been effective to recess gate materials 34 and 40 within the depicted trenches 28, 36 and 37 formed within masking material 20. Exemplary preferred techniques include any one or combination of chemical mechanical polishing, resist etch back or timed chemical etching. Where, for example, materials 34 and 40 comprise polysilicon and outer layer 26 of masking material 20 comprises silicon nitride, an exemplary etching chemistry capable of producing the Fig. 10 construction in a timed etch includes tetramethyl ammonium hydroxide followed by exposure to a hydrofluoric acid solution.

Referring to Fig. 11, an exemplary higher conductive layer 42 has been deposited (i.e., a refractory metal, other metal, or metal silicide) and polished or etched back, followed by deposition of an insulative material layer 44 followed by polishing or other etch back of it. Such thereby, in one exemplary preferred embodiment, caps recessed gate materials 34 and 40 within masking material 20 with insulative material 44. In one preferred embodiment, insulative material 44 is of common composition to that of inner layer 24 of masking material 20 where such is formed of insulative material. Accordingly by way of example only, materials 44 and 24 might comprise silicon nitride where material 26 comprises silicon dioxide, or the reverse in but preferred embodiments.

Referring to Fig. 12 and in but one preferred embodiment, outer layer 26 of masking material 20 has been etched selectively relative to inner layer 24 and to capping insulative material 44 received over recessed gate materials 34 and 40. In one preferred implementation, an aspect of the invention includes forming gate dielectric material within the trenches, for example material 32, prior to removing silicon nitride of the masking material when such is utilized.

Referring to Fig. 13 and in but one preferred embodiment, insulative material 50 preferably of common composition to that of inner insulative material layer 24 of masking material 20 has been deposited over substrate 10 as shown.

Referring to Fig. 14, material 50 and material 24 have been anisotropically etched effective to form insulative sidewall spacers 52 about gate materials 34, 40 and 42. Some or all of pad oxide layer 22 (when such is utilized) might be removed earlier or at this point in the process, or some might remain as part of the finished circuitry construction. Regardless in one preferred embodiment, aspects of the invention include removing at least a majority of the masking material at some point after at least gate material 34 has been deposited. In most preferred embodiments, such methods of forming field effect transistor gates, field effect transistors, and transistor gate arrays and circuitry peripheral to the gate array are preferably void of photolithographic patterning of any one or combination of gate materials 34, 38 and 42 after such has/have been deposited.

Fig. 14 depicts fabrication of source/drain regions 56, with such most preferably being formed within semiconductive material 11 of substrate 10. Such might be formed by one or a combination of ion implants of suitable conductivity enhancing dopant(s) during any of the above processing steps. Further of course, other channel, channel stopping, or other implants, whether existing or yet-to-be developed, could be conducted during any of the above processing.

Alternate embodiments are of course contemplated with the invention only being limited by the claims as literally worded without reading limitations from other claims, the drawings, or specifications into the claims. By way of example only, a few exemplary alternate embodiments will now be described. Referring to Fig. 15, such depicts a semiconductor substrate 10a corresponding to or a substitute for the Fig. 4 depicted processing with respect to the first described

embodiments. Like numerals from the first described embodiments have been utilized where appropriate, with differences being indicated with the suffix "a" or with different numerals. Fig. 15 depicts substrate fragment 10a which includes the forming of grounded gate trenches 37a through masking material 20 in the array in the same masking step in which array circuitry trenches 28 and 30 are formed. Further by way of example only in the depicted embodiment, grounded gate trenches 37a have been formed to extend into the trench isolation regions, such as trench isolation region 15.

Referring to Fig. 16, gate dielectric material 32 has been formed, and gate material 34a has been deposited to within grounded gate trench 37a.

Referring to Fig. 17, subsequent processing has occurred to a point of fabrication of anisotropically etched insulative sidewall spacers 52 and source/drain regions 56. Processing, materials, etc. are otherwise preferably as provided above in the first described embodiments of Figs. 1-14.

Further by way of example only, another exemplary embodiment processing with respect to a substrate fragment 10b is described with reference to Figs. 18 and 19. Like numerals from the first and second described embodiments have been utilized where appropriate, with differences being indicated with the suffix "b" or with different numerals. Fig. 18 corresponds in processing sequence to that of Fig. 4, and wherein one or more peripheral circuitry trenches 36b have been formed commensurate with formation of array circuitry trenches 28, 30. Such might be advantageously utilized wherein certain transistors of the peripheral circuitry and the array circuitry are desired to be of the same conductivity type and/or work function, and/or other desired property.

Fig. 19 depicts subsequent gate dielectric 32 fabrication, gate material 34b deposition, and then subsequent patterning of masking material 20b and gate material 34b to form, by way of example only, grounded gate trenches 37b and another peripheral circuitry trench 36b. Accordingly, some of the peripheral circuitry trenches might be formed commensurate with formation of the array circuitry trenches. Subsequent processing could occur, for example, analogously or otherwise to that depicted and described relative to Figs. 8-14.

Fig. 20, by way of example only, depicts alternate exemplary processing with respect to a substrate fragment 10c. Like numerals from the above-described embodiments have been utilized where appropriate, with differences being indicated with the suffix "c" or with different numerals. Fig. 20 depicts processing whereby array trenches 28, 30 have been fabricated using a masking step separate from fabrication of any other line trenches in the depicted cross section. Subsequent thereto, grounded gate isolation trenches 37 and one peripheral circuitry gate trench 70 have been fabricated in a common masking step, and gate material 40c deposited thereover. Thereafter, another masking has been conducted through masking material 20 and the previously deposited gate materials to form another peripheral circuitry trench 74. Gate dielectric 71 has been formed (for example by any of the above described processes relative to gate dielectric material fabrication). Subsequently, gate material 76 has been deposited which may be the same or different from any of the above exemplary gate materials. Processing could otherwise ideally proceed subsequently commensurate with or different from the above-described embodiments as depicted and described relative to Figs. 8-14 for example.

Aspects of the invention also encompass a method of forming field effect transistor gates which include forming masking material over semiconductive material of the substrate, and where the substrate comprises a trench isolation region. Exemplary embodiments, by way of example only, are those described above. In a common masking step, a first trench is formed through the masking material and into the semiconductive material and a second grounded isolation gate trench is formed through the masking material over the field isolation region. Such masking step in one preferred implementation comprises photolithography. Further in one implementation, the second grounded isolation gate trench might be fabricated to extend within the field isolation region during the stated common masking step.

Subsequently in a common deposition step, gate material is deposited within the first trench and the second trench. Such common deposition step preferably at least fills, and more preferably overfills, the first and second trenches with the gate material. In one preferred implementation, at least a

majority of the masking material is removed after depositing the gate material. In one preferred implementation, the process is void of any photolithographic patterning of the gate material after its deposition. In one implementation, the gate material as deposited covers the masking material with gate material, and the process further comprises removing the gate material selectively relative to and exposing of the masking material effective to isolate the gate material within the first and second trenches.

In one implementation, an aspect of the invention encompasses a method of forming integrated circuitry comprising a transistor gate array including first gates and second grounded isolation gates. Masking material is formed over semiconductive material of a substrate, and the substrate comprises trench isolation regions. First trenches are formed through the masking material and into the semiconductive material for the first gates. Second grounded isolation gate trenches are formed through the masking material over the field isolation regions for the second grounded isolation gates. Gate material is deposited within the first and second trenches.

The first and second trenches might be formed at the same time or at different times, for example either before or after the other. The second trenches might be formed within the field isolation regions or received only outwardly thereof.

Depositing of the gate material within the first and second trenches might occur in the same deposition step, or might occur in different deposition steps. Further, some of the depositing of the gate material within the first and second trenches might occur in the same deposition step, and another of some of the depositing of gate material within the first and second trenches might occur in different deposition steps. Regardless and preferably, depositing of the gate material at least fills, and even more preferably overfills, the first and second trenches with the gate material. Processing is otherwise preferably as described above with respect to the other embodiments.

Claims

What is claimed is:

1. A method of forming integrated circuitry comprising a transistor gate array and circuitry peripheral to the gate array, comprising:

forming masking material over semiconductive material of a substrate;

forming array circuitry trenches through the masking material and into the semiconductive material;

depositing array gate material within the array circuitry trenches in the masking material and within the array circuitry trenches in the semiconductive material;

after depositing the array gate material, forming peripheral circuitry trenches through the masking material; and

depositing peripheral circuitry gate material within the peripheral circuitry trenches within the masking material.

2. The method of claim 1 wherein forming the peripheral circuitry trenches exposes the semiconductive material of the substrate, and further comprising forming a gate dielectric layer over the exposed semiconductive material of the substrate prior to depositing the peripheral circuitry gate material, the gate dielectric layer also forming over the array gate material.

3. The method of claim 2 wherein the gate dielectric layer is formed on the array gate material.

4. The method of claim 3 wherein forming at least a majority of the gate dielectric layer comprises thermal oxidation of the exposed semiconductive material and of the array gate material.

5. The method of claim 1 wherein the array circuitry trenches are formed using a masking step, and further comprising forming grounded gate trenches through the masking material in the array in the same masking step in which the array circuitry trenches are formed.

6. The method of claim 1 wherein the peripheral circuitry trenches are formed using a masking step, and further comprising forming grounded gate trenches through the masking material in the array in the same masking step in which the peripheral circuitry trenches are formed.

7. The method of claim 1 wherein the masking material comprises silicon dioxide received over silicon nitride.

8. The method of claim 1 wherein the depositing of the array gate material at least fills the array circuitry trenches in the masking material and the array circuitry trenches in the semiconductive material with the array gate material.

9. The method of claim 1 wherein the depositing of the array gate material overfills the array circuitry trenches in the masking material and the array circuitry trenches in the semiconductive material with the array gate material.

10. The method of claim 1 wherein the depositing of the peripheral circuitry gate material at least fills the peripheral circuitry trenches in the masking material and the peripheral circuitry trenches in the semiconductive material with the peripheral circuitry gate material.

11. The method of claim 1 wherein the depositing of the peripheral circuitry gate material overfills the peripheral circuitry trenches in the masking material and the peripheral circuitry trenches in the semiconductive material with the peripheral circuitry gate material.

12. The method of claim 1 comprising removing at least a majority of the masking material after depositing the peripheral circuitry gate material.

13. The method of claim 1 being void of photolithographic patterning of the array gate material after its deposition.

14. The method of claim 1 being void of photolithographic patterning of the peripheral circuitry gate material after its deposition.

15. The method of claim 1 being void of photolithographic patterning of the array gate material after its deposition, and being void of photolithographic patterning of the peripheral circuitry gate material after its deposition.

16. The method of claim 1 comprising forming some peripheral circuitry trenches and some array circuitry trenches in the same masking step.

17. A method of forming integrated circuitry comprising a transistor gate array and circuitry peripheral to the gate array, comprising:

forming masking material over semiconductive material of a substrate;

forming array circuitry trenches through the masking material and into the semiconductive material;

depositing array gate material within the array circuitry trenches in the masking material and within the array circuitry trenches in the semiconductive material;

forming peripheral circuitry trenches through the array gate material and through the masking material; and

depositing peripheral circuitry gate material within the peripheral circuitry trenches within the array gate material and within the masking material.

18. A method of forming field effect transistor gates, comprising:

forming masking material over semiconductive material of a substrate, the substrate comprising a trench isolation region;

in a common masking step, forming a first trench through the masking material and into the semiconductive material and forming a second grounded isolation gate trench through the masking material over the trench isolation region; and

in a common deposition step, depositing gate material within the first trench and second trench.

19. The method of claim 18 comprising forming the second grounded isolation gate trench to within the trench isolation region during the common masking step.

20. The method of claim 18 wherein the depositing of the gate material at least fills the first and second trenches with the gate material.

21. The method of claim 18 wherein the depositing of the gate material overfills the first and second trenches with the gate material.

22. The method of claim 18 wherein the masking material comprises silicon dioxide received over silicon nitride.

23. The method of claim 18 comprising removing at least a majority of the masking material after depositing the gate material.

24. The method of claim 18 being void of photolithographic patterning of the gate material after its deposition.

25. The method of claim 18 wherein depositing the gate material covers the masking material with gate material, and comprising removing the gate material selectively relative to and exposing the masking material effective to isolate the gate material within the first and second trenches.

26. The method of claim 18 wherein the masking step comprises photolithography.

27. A method of forming integrated circuitry comprising a transistor gate array including first gates and second grounded isolation gates, comprising:

forming masking material over semiconductive material of a substrate, the substrate comprising trench isolation regions;

forming first trenches through the masking material and into the semiconductive material for the first gates;

forming second grounded isolation gate trenches through the masking material to within the trench isolation regions for the second grounded isolation gates; and

depositing gate material within the first and second trenches.

28. The method of claim 27 comprising forming the first and second trenches at the same time.

29. The method of claim 27 comprising forming the second trenches after forming the first trenches.

30. The method of claim 27 comprising forming the second trenches to within the trench isolation regions.

31. The method of claim 30 comprising forming the first and second trenches at the same time.

32. The method of claim 30 comprising forming the second trenches after forming the first trenches.

33. The method of claim 27 wherein the depositing of gate material within the first and second trenches occurs in the same deposition step.

34. The method of claim 27 wherein the depositing of gate material within the first and second trenches occurs in different deposition steps.

35. The method of claim 27 wherein some of the depositing of gate material within the first and second trenches occurs in the same deposition step, and another some of the depositing of gate material within the first and second trenches occurs in different deposition steps.

36. The method of claim 27 wherein the depositing of the gate material at least fills the first and second trenches with the gate material.

37. The method of claim 27 wherein the depositing of the gate material overfills the first and second trenches with the gate material.

38. The method of claim 27 wherein the masking material comprises silicon dioxide received over silicon nitride.

39. The method of claim 27 comprising removing at least a majority of the masking material after depositing the gate material.

40. The method of claim 27 being void of photolithographic patterning of the gate material after its deposition.

41. The method of claim 27 wherein depositing the gate material covers the masking material with gate material, and comprising removing the gate material selectively relative to and exposing the masking material effective to isolate the gate material within the first and second trenches.

42. A method of forming integrated circuitry comprising a transistor gate array and circuitry peripheral to the gate array, comprising:

forming masking material over semiconductive material of a substrate, the substrate comprising a trench isolation region;

in a common masking step, forming array circuitry trenches through the masking material and into the semiconductive material and forming a grounded isolation gate trench through the masking material into the trench isolation region;

in a common deposition step, depositing array gate material within the array circuitry trenches in the masking material, within the array circuitry trenches in the semiconductive material, and within the grounded isolation gate trench within the trench isolate region;

after depositing the array gate material, forming peripheral circuitry trenches through the masking material; and

depositing peripheral circuitry gate material within the peripheral circuitry trenches within the masking material.