

ABSTRACT OF THE DISCLOSURE

A vertical memory device includes gate electrodes on a substrate, a channel extending through the gate electrodes, and a contact plug extending through the gate electrodes. The gate electrodes are stacked in a first direction substantially vertical to an upper surface of the substrate and arranged to have a staircase shape including steps of which extension lengths in a second direction substantially parallel to the upper surface gradually increase from a lowermost level toward an uppermost level. A pad at an end portion of each of the gate electrodes in the second direction has a thickness greater than those of other portions thereof. The channel extends in the first direction. The contact plug extends in the first direction. The channel contacts the pad of a first gate electrode among the gate electrodes to be electrically connected thereto, and is electrically insulated from second gate electrodes among the gate electrodes.

FIG. 3A