

REDUNDANCY CIRCUIT FOR USE IN A
SEMICONDUCTOR MEMORY DEVICE

5 The present invention relates to semiconductor circuits, and more particularly, to circuits for replacing defective cells with redundant cells in a semiconductor memory device.

10 Recently, redundancy schemes have been widely used in the production of large scale semiconductor memory devices, in order to overcome reduced production yields caused by defects of memory cells generated during the manufacturing process, which often render an entire chip useless.

15 Redundancy techniques provide an on-chip spare memory array in addition to a normal memory array, and, when one or more memory cells in the normal memory array are faulty, replace rows or columns containing the
20 defective normal memory cell or cells with rows or columns containing the defect-free redundant cell or cells.

25 Currently, the substitution of good cells for defective cells in normal memory arrays is implemented by electrically or physically disconnecting faulty rows or columns of cells from the normal memory array and electrically connecting redundant rows or columns to the row or column address decoder in such a manner that each
30 responds to the address bit pattern which formerly selected the faulty row or column. Such redundancy is performed either before or after packaging of the memory chip and has been accomplished by using one of two methods, i.e., one of blowing polysilicon fuses by use of
35 pulses of electrical current, and the other of

vaporization of conductor material with accurately focused laser beam spots.

However, as memory arrays become more dense and
5 line widths grow smaller, the laser redundancy technology has an increased problem in a requirement for highly expensive apparatus for accurately controlling the magnitude and the position of the laser beam spots. Meanwhile, the electrically polysilicon fuse-blowing
10 redundancy technique has another problem of arranging on the same chip additional circuits for supplying such large currents as to cut open polysilicon fuses, as well as peripheral circuits for protecting circuit elements from destruction by large current. This creates the
15 drawback of inevitable increase in chip size or area.

In addition to the above mentioned redundancy schemes, there has been another one which is to substitute redundant rows or columns for defective rows
20 of columns by programming nonvolatile memory elements so as to selectively enable a corresponding redundant row or column whenever the row or column having defective normal memory cells is addressed.

25 Various circuits for performing such substitutions are set forth in U.S. Patent No: 4 422 161 to Kressel et al and 4 514 830 to Hagiwara et al. However, these patents need to employ a plurality of nonvolatile memory elements for the replacement of faulty
30 cells.

However, perhaps the greatest problem of the redundancy scheme using such nonvolatile memory elements is the reliability of the element itself. If any one of
35 the nonvolatile memory elements programmed for

substitution of rows or columns containing defective cells is faulty, information stored in memory elements will be lost and the replacement of bad cells will not be performed.

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Preferred embodiments of the present invention aim to provide a circuit for implementing redundancy which does not blow a fuse material, but employs a nonvolatile memory element.

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Preferred embodiments of the invention aim to provide circuits for implementing redundancy which employ a minimum number of nonvolatile memory elements. Further, preferred embodiments aim to provide circuits
15 for implementing redundancy which increase the reliability of a nonvolatile memory device storing the identity of rows or columns having bad cells.

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According to the present invention, there is provided a semiconductor memory device comprising:

a plurality of normal memory cells;

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a plurality of redundant memory cells for the replacement of any defective ones of said normal memory cells;

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a normal decoder connected to receive a plurality of address signals and operative to address normal memory cells identified by said address signals; and

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a redundant decoder connected to receive said address signals and operative to output a redundant signal upon a redundant line in dependence upon said address signals, the redundant decoder comprising a

plurality of first program devices connected in parallel between a reference potential and said redundant line and operative to output selectively said reference potential in dependence upon said address signals; and a second
5 additional program device connected in parallel with said first program devices between said reference potential and said redundant line and operative to output selectively said reference potential, said second program device being connected to receive an input signal which
10 is complementary to that of a selected one of said first program devices; the arrangement being such that, when the memory is addressed, then if none of said normal memory cells is defective, one of said one selected first program device and said second program device outputs
15 said reference potential and, if at least one of said normal memory cells is defective, none of said first program devices and said second program device outputs said reference potential, the presence or absence of said reference potential at the output of said first and
20 second program devices determining the presence or absence of said redundant signal upon said redundant line, and the redundant signal being operative to enable or inhibit addressing of either the normal memory cells or the redundant memory cells accordingly.

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Preferably, said normal detector is connected to receive and respond to said redundant signal, and each of said first program devices is connected to receive a respective one of said address signals and its
30 complement.

Said second program device is preferably connected to receive, in an inverse connection, the true and complementary address signals of said selected one of
35 said first program devices.

Preferably, said reference potential is ground.

Each program device preferably comprises a non-
5 volatile memory element capable of assuming first and
second program states.

Preferably, each program device comprises:

a true address signal line;

10 a complementary address signal line;

a nonvolatile memory element having a program
gate terminal, erase drain terminal, a drain terminal and
source terminal which is grounded;

a first means, connected to said program gate
15 terminal through an isolation transistor, for producing a
high potential in a second program mode, a low potential
in a first program mode, and supplying a predetermined
potential to said program gate terminal so that said
memory element has better conduction during reading
20 operation;

a second means, connected to said erase drain
terminal, for producing a high potential in said first
program mode;

a third means, connected between said true
25 address signal line and an input terminal of said
isolation transistor, and between said complementary
address signal line and the input terminal of said
isolation transistor, for supplying a sufficiently high
potential to said input terminal that the high potential
30 produced at the first means in said second program mode
transfers to said program gate terminal, when said true
address signal is true, thereby causing a change of
program state of said memory element as programmed in
said first program mode, and producing a low potential to
35 said input terminal, during said second program mode when

said true address signal is complementary, thereby causing no change of program state of said memory element as programmed in said first program mode; and

5 a sensing means, connected between said drain terminal and said true address signal line and said complementary address signal line, for grounding the output line connected to said redundant line when said true address signal is true, and floating said output line when said true address signal is complementary.

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Said nonvolatile memory element preferably comprises a plurality of nonvolatile memory devices of which program gates and erase drains are connected together with a program gate terminal and an erase drain
15 terminal respectively, and of which drains of said devices connected in parallel are connected to a drain terminal and of which source-drain junction points of said devices connected in series are connected together and of which other sources are grounded or connected to
20 reference potential.

Each said nonvolatile memory device is preferably a FLOTOX type nonvolatile memory device.

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Each of said first, second and third means may comprise a high voltage pump circuit.

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For a better understanding of the invention and to show how the same may be carried into effect,

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accompanying diagrammatic drawings, in which:

Figure 1 is a block diagram of an embodiment of the invention, showing the general layout of a normal row decoder and its coupling to a redundant row decoder containing row address program devices;

Figure 2 is a circuit diagram showing a row address program device comprising a part of Figure 1;

Figure 3 is a cross-sectional view of a known FLOTOX type non-volatile memory element;

Figure 4 is an equivalent circuit diagram of the element of Figure 3;

Figure 5 is a circuit diagram of four cell bridge connection FLOTOX type nonvolatile memory elements used in a row address program device embodying the present invention;

Figure 6 is a redundant circuit diagram showing a plurality of normal row decoders and their coupling to redundant row decoders; and

Figure 7 is a conventional circuit diagram showing a high voltage pump circuit used as a part of Figure 2.

Figure 1 illustrates a redundant circuit for replacing a row line containing faulty memory cells with a redundant row line. Although the redundancy circuit of Figure 1 applies to the redundancy of a row line (often referred as a "bit line"), it will be easily perceived that those skilled in the art can apply the same circuit

of Figure 1 also to a column line (often referred as a "word line").

The redundant circuit as shown in Figure 1 includes an ordinary normal decoder 20 which receives a combination of row address signals and their complements, $A_0/\overline{A_0}$, $A_1/\overline{A_1}$, to $A_i/\overline{A_i}$ (where $A_k/\overline{A_k}$ means A_k or $\overline{A_k}$ and k represents any number from 0 to i) from row address buffers (not illustrated) and which is connected to a line 5 coupled to the redundant row line 3. The normal decoder 20 is a NOR gate used in a usual semiconductor memory device and, when all of its input address signals are at logic low levels, operates so as to select memory cells connected to a normal row line 4.

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A redundant row decoder 10 comprises row address program devices $RAPD_0$ to $RAPD_i$ which receive respectively pairs of row address signals and their complements A_0 , $\overline{A_0}$; A_1 , $\overline{A_1}$;; A_i , $\overline{A_i}$, from row address buffers (not shown in the figure). An additional row address program device $RAPD_{i+1}$ receives input signals $\overline{A_i}$, A_i which are complementary to those A_i , $\overline{A_i}$ supplied to the row address program device $RAPD_i$. A redundant row line 3 is coupled to all of the output lines 2-0 through 2- $i+1$ of the row address program devices $RAPD_0$ to $RAPD_{i+1}$, and a MOS transistor 1 of D type (referred to as a "D type" hereinafter) operates as a driver whose gate and source are connected to the line 3 and whose drain is coupled to a supply voltage source V_{cc} (+ 5 volts).

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It will be noted that the number of row address program devices $RAPD_0$ to $RAPD_{i+1}$ is only one more than the number of row address bit patterns. For example, a semiconductor memory device having 2^n row lines of a normal memory array needs a number n of address bit

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patterns to select a unique row line. Therefore, the number of row address program devices in the illustrated embodiment will be $n+1$.

5 Now, if we assume that one added row address program device is $RAPDi+1$ as indicated in Figure 1, input signals $\overline{A_i}$ and A_i of said device $RAPDi+1$ will, respectively, become complementary signals of input A_i and $\overline{A_i}$ which are supplied to the contiguous device $RAODi$.
10 Therefore, if there is no need to enable the redundant row line 3 due to a defect-free memory cell in the normal memory array, the redundant row line 3 always maintains a logic low level so as not to select the redundant memory cell. This is the reason why the signals on the output
15 lines 2-i and 2-i+1 of row address program devices $RAPDi$ and $RAPDi+1$ have mutually inverted logic states, due to reset programming of all row address program devices, which will be described later in detail.

20 On the other hand, if the redundant row line 3 containing defect-free spare memory cells must be selected due to one or more defective normal memory cells on the line 4, row address program devices $RAPD0$ through $RAPDi+1$ will be programmed as will be described later so
25 that all of the devices $RAPD0$ to $RAPDi+1$ become nonconductive if they receive row address input signals which would otherwise select the normal row line 4.

30 Then, the redundant row line 3 is selected as a logic high level (+ 5 volts) by the transfer of the potential V_{cc} via the D type MOS transistor 1, and this logic level deselects the normal decoder 20 which then outputs a logic low level on the normal row line 4.

35 Figure 2 illustrates one schematic circuit

diagram of row address program devices RAPD0 to RAPDi+1, all of the same structure. The transistors used are all N type enhancement or depletion MOS transistors. The threshold voltage of the depletion MOS transistors will be about -3 volts and that of the enhancement MOS transistors will be about +3 volts. Pulse signals RS, CP and PR will be kept normally at low levels. A block 100 represents a nonvolatile memory element and each of blocks 200, 300 and 400 represents a high voltage pump circuit.

Each block 100 employs a FLOTOX type nonvolatile memory element. For details of FLOTOX type nonvolatile memory elements, one can refer to "16 K E²PROM Employing New Array Architecture", IEEE Journal of Solid State circuits, OCT. 1982, pp. 833-840.

Referring now to Figure 3 showing the structure of a FLOTOX type nonvolatile memory element, reference numeral 170 represents a p type substrate or body, and reference numerals 140, 131 and 121 represent an N⁺ source region, N⁺ drain region and N⁺ erase drain region, respectively. An oxide film 160 of 70Å to 200Å on the erase drain region 121 is a tunnel oxide film. An oxide film 180 on the substrate between the source region 140 and the drain region 131 is a gate oxide film, and reference numerals 161 and 162 represent insulating films, a first polycrystalline silicon layer 150 represents a floating gate, and a second polycrystalline silicon layer 111 represents a program gate.

Figure 4 is an equivalent circuit diagram of Figure 3 and like reference numerals in Figures 3 and 4 are used to designate like parts.

A writing operation of the FLOTOX type nonvolatile memory element can be accomplished by the application of a positive potential V_{pp} (approximately +20 volts) to the program gate 111 and by grounding the
5 erase drain 121. This potential provides an electric field across the tunnel oxide film 160 of sufficient magnitude to tunnel electrons from the erase drain 121 to the floating gate 150. Once electrons have been tunneled into the floating gate 150, the threshold voltage of the
10 memory device becomes positive and the memory device performs the same operation as that of an ordinary enhancement mode device. That is, during the reading operation in which a positive potential of approximately 2 volts is applied to the program gate 111, the memory
15 device becomes nonconductive.

Meanwhile, to erase the memory device of Figure 3 or Figure 4, a positive potential of V_{pp} is applied to the erase drain 121 while the program gate 111 is
20 grounded. Then, electrons are tunneled into the erase drain 121 and the floating gate 150 is charged positively. Hence, the memory device operates as a depletion mode device and becomes conductive at the times of reading operation.

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The program gate 111, the erase drain 121 and the drain 131 of the FLOTOX type nonvolatile memory element are connected to the lines 110, 120 and 130, respectively, while the source 140 is grounded.

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Figure 7 is a circuit diagram of a part of Figure 2, showing a known high voltage pump circuit.

The high voltage pump circuit comprises a MOS
35 transistor 214 of enhancement type (referred to as "E

type" hereinafter) whose drain 210 is coupled to a positive potential of V_{pp} produced from a high voltage generating circuit (not shown) and whose source is connected to a node 222 and whose gate is coupled to an output node 220. A driver transistor is formed of an E type MOS transistor 218 whose gate and drain are coupled to the node 222, and whose source is connected to the node 220. A coupling MOS capacitor 216 has one electrode 212 coupled to receive a clock pulse ϕ , i.e., square pulse of peak to peak 5 volts generated from a pulse generator (not illustrated), and another electrode connected to the node 222.

When the output node 220 is floating at logic high level (+5 volts), the transfer transistor 214 for charging the clocked capacitor 216 turns on. Then the MOS capacitor 216 pumps charge into the output node 220 through the transistor 218 in response to clock pulses. Since the output node 220 is floating in this case, the voltage thereof rises to a high potential V_{pp} (+ 20 volts).

When the output node 220 is at a logic low level (ground level), the transfer transistor 214 turns off. Therefore, although clock pulse ϕ is applied to the MOS capacitor 216 and a little charge is transferred to the output node 220, the output node 220 will keep at a logic low level, because it is grounded.

Turning to Figure 2, each output node 220 of high voltage pump circuits 200, 300 and 400 is connected to conductor lines 33, 120, and 34 respectively. Conductor lines 31, 32, 33, 34, 35, 36, 110, 120 and 130 may be lines made of polysilicon or metal. Between the supply voltage source of V_{cc} (+ 5 volts) and the line 34, an E

type MOS transistor 64 and a D type MOS transistor 65 of which source-drain paths are connected in series are inserted. The gate of the transistor 65 is connected to the line 34 and a pulse signal CP, which goes high at the time of address program, which will be described later, is applied to the gate of the transistor 64.

Between the line 34 and the ground source, the drain-source path of an E type MOS transistor 66 is connected and a reset pulse signal RS, which goes to high at the time of reset program which will be described later, is applied to the gate of the transistor 66. Therefore, during the time of address program, the line 34 will go high (+ 5 volts) by the conduction of driving transistors 64 and 65 and then will go to a high potential voltage (+ 20 volts) by the operation of the high voltage pump circuit 400.

On the other hand, between the supply voltage source Vcc (+5 volts) and the ground source, there is connected in series the drain-source paths of a D type MOS transistor 67 whose gate is grounded, an E type MOS transistor 68 whose gate is coupled to the pulse signal $\overline{CP}$ (complement of CP), an E type MOS transistor 69 whose gate is coupled to the same signal $\overline{CP}$ as that of the transistor 68, and a D type MOS transistor 70 whose gate is grounded. The connection node 71 of the transistor 68 and 69 is coupled to the line 34. The circuit formed of transistors 67 to 70 is a voltage reference generator, where the signal $\overline{CP}$ is a logical high state, which supplies $V_{cc}/2$ (+ 2.5 volts) to lines 34 and 110 during the reading operation which will be described later. Such application of voltage $V_{cc}/2$ to the line 110 makes the FLOTOX type nonvolatile memory element 100 of depletion mode at the time of a reading operation have

better conductivity.

The line 34 is connected to the line 110 via a drain-source path of a D type MOS transistor 90. The gate of the transistor 90 is coupled to the line 33. Between the supply voltage source Vcc and the line 33, an E type MOS transistor 44 and a D type MOS transistor 45 are connected in series, as indicated. The gate of the transistor 44 is connected to the line 31 on which an address signal Ak delivered from an address buffer (not shown) is supplied and the gate of the transistor 45 is connected to the line 33. Between the line 33 and the ground source, E type transistors 46 and 47 are connected in parallel. The gate of the transistor 46 is coupled to a pulse signal $\overline{PR}$ and the gate of the transistor 47 is connected to the line 32, on which an address signal $\overline{Ak}$, i.e. complement of the address signal Ak, is supplied. Therefore, at a logic low level of the signal $\overline{PR}$, if the address signal Ak is high ($\overline{Ak}$ is low), the line 33 will be at high potential Vpp by the conduction of transistors 44 and 45 and then by the operation of the high voltage pump circuit 200. Meanwhile, if the address signal $\overline{Ak}$ is high (Ak is low), the line 33 will be in a logic low level by the ON state of the transistor 47.

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At the end terminal of the line 120 connected to the erase drain 121 of Figure 4 there is connected the output node 56 of an inverter which is formed of E type MOS transistors 54 and 55 connected in series between the supply source Vcc and the ground source and which operates as an inverter by a reset signal RS and its complement $\overline{RS}$. Therefore, with the high level of the reset signal RS at the time of reset program, the line 120 goes to a high potential Vpp by the operation of the inverter and the high voltage pump circuit 300.

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Between the supply voltage source Vcc and the line 130 connected to the drain 131 of the nonvolatile memory element 100, a D type MOS transistor 81 whose gate is coupled to a node 38 and a D type MOS transistor 82 whose gate is grounded, are connected in series.

The line 35 coupled to the node 38 is connected to the drain of an E type MOS transistor 83 and the drain of the transistor 83 is connected to gates of E type transistors 85 and 87. The signal PR having a logic high level at the time of address program is applied to the gate of the transistor 83 whose source is grounded, and the transistor 83 turns on at that time. The transistor 83 and a load transistor of D type 84 connected in series at a node 39 form an inverter. The output node 39 of the inverter is connected to the gate of an E type MOS transistor 86 via a line 36. Each drain-source path of transistors 86 and 87 is connected in series between line 31 and 32 via a node 37, as indicated.

The node 37 is connected to the gate of an E type MOS transistor 88 whose source is grounded and a drain line 89 of the transistor 88 is the output line coupled to the redundant row line 3.

A circuit comprising transistors 81 to 88 operates during the reading operation as a sensing circuit for determining whether or not the redundant row line will be selected according to the programmed state of the nonvolatile memory element 100. That is, if the nonvolatile memory element 100 is programmed as a depletion mode element and the row address signal Ak on the line 31 is at a logic low level, the potential of the

node 38 will be low (ground) by the conduction of the element 100 and by the signal PR provided as a logic low level during the reading operation. Then, the transistors 85 and 87 become OFF and the transistor 86 becomes ON. Therefore, the node 37 becomes logic low and the redundant row line 3 connected to the line 89 becomes logic high so as to select the redundant memory cell.

However, if the row address signal Ak had logic high level at that time, the node 37 would be at a logic high level and the redundant row line 3 logic low level and, as a result, redundant memory cells connected to the redundant row line 3 would not be selected but normal memory cells connected to the normal row line 4 would be selected.

On the other hand, if the nonvolatile memory element 100 was programmed as an enhancement mode element, the node 38 would be at a logic high level by the nonconduction of the element 100. Therefore, if the complementary row address signal $\overline{Ak}$ has a logic low level, the redundant row line 3 will be selected by the conduction of the transistor 87.

The mode of operation will now be described in detail, with reference to Figures 1 and 2.

Programming steps of the row address program devices RAPD0 to RAPDi+1 for the substitution of good cells for defective cells can be divided into two steps: a reset program (first program mode) and an address program (second program mode).

The reset program is performed at the same time on all of the row address program devices RAPD0 to

RAPDi+1 after a test of the memory array, and programs all nonvolatile memory elements so as to operate in depletion mode. The reset program is begun by setting only the reset signal RS of program control signals RS, CP and PR at a logic high level. Then, transistors 46, 54 and 66 are rendered conductive. Hence, lines 33, 34, and 110 are discharged into logic low levels and the line 120 is charged to a high potential V_{pp} by the operation of the high voltage pump circuit 300 as described above. As a result, all nonvolatile memory elements in row address program devices RAPD0 to RAPDi+1 are held as depletion mode elements due to the high potential V_{pp} applied to the erase drain 121 and the ground potential applied to the program gate 111.

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After the completion of the above mentioned reset program step, an address program step for substituting redundant memory cells is performed. The address program step is to program the row address program devices RAPD0 to RAPDi+1 so as to select the redundant row line by causing the address bit pattern selecting the normal row line to input to the above devices. The address program is divided into two cases; one is the case that the row address signal A_k is low, and the other is the case that the row address signal A_k is high.

In any case, program control signals PR and CP are set at logic high levels and the reset signal RS is set at a logic low level. Therefore, the line 120 will become logic low by the conduction of the transistor 55 and the line 34 will be charged to a high potential V_{pp} by the conduction of transistors 64 and 65, and by the operation of the high voltage pump circuit 400.

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At this time, if a row address signal A_k on the

line 31 has a logic low level (complementary signal $\overline{Ak}$ of the signal Ak has a logic high level), the transistor 44 will become OFF and the transistor 47 will become ON. Then, the line 33 will be discharged to the ground state.

5 Therefore, the isolation transistor 90 transfers only a part of the high potential V_{pp} (+ 20 volts) on the line 110. As a result, the line 110 will provide a potential of approximately 3 volts on the program gate 111. Accordingly, since this potential can not provide an

10 electric field of sufficient magnitude to cause the memory element 100 to change the program state, the memory element 100 will be maintained in the same depletion mode as that of the above mentioned reset programming step.

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If a row address signal Ak on the line 31 has a logic high level, the transistor 44 and 45 will become conductive, and then the line 33 will have a high potential V_{pp} by the operation of the high voltage pump

20 circuit 200. Therefore, the potential on the line 110 will become a high potential V_{pp} by the conduction of the transistor 90. As a result, the nonvolatile memory element 100 will be changed into an enhancement mode element.

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Once the above mentioned program steps are completely finished, at the time of reading operation, the redundant row decoder 10 must operate so as to select the redundant row line 3 in place of the defective normal

30 row line 4. Such a reading operation is performed by the sensing circuit formed of transistors 81 to 88. At this time, signals CP, RS and PR are all in logic low levels, that is, in normal state. Therefore, lines 110 and 120 are both at logic low levels. If the nonvolatile memory

35 element 100 is programmed in depletion mode, the node 38

will be at a logic low level, and then the transistor 86 will turn on, while the transistor 87 is OFF. Hence, the logic low level of the address signal A_k appears at the node 37 and the transistor 88 becomes OFF, and then the
5 redundant row line is selected. If the nonvolatile memory element 100 is programmed as an enhancement mode, the transistor 86 will be OFF, while the transistor 87 is ON. Therefore, the redundant row line is selected by the logic low level of the address signal A_k .

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Therefore, if the memory cells connected to the normal row line 4 are free of defects, either one of the output signals of the row address program devices $RAPD_i$ and $RAPD_{i+1}$ will be at logic low level due to the above
15 mentioned reset program. Hence, the redundant row line 3 maintains a logic low level so as not to be selected.

If the memory cells on the normal row line 4 are defective, one or more row address program devices of
20 which input row address signal A_k has a logic low level will be programmed as depletion modes, while row address program devices of which input row address signal A_k has a logic high level will be programmed as enhancement modes.

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The programming is such that, when the respective address signal is applied to the row address programming devices, the output signals of none of them will be at logic low level. Hence, the redundant row line 3 floats
30 to logic high level, due to the supply voltage V_{CC} conducted through the transistor 1, so that the redundant row line 3 is selected and the normal low line 4 is deselected.

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Although the above description gives an example

of using one FLOTOX type nonvolatile memory element, if the element is defective, the redundancy plan will be unsuccessful. To solve this mentioned problem, a four cell FLOTOX type nonvolatile memory element connected as a bridge type can be used in block 100 of Figure 2.

Referring to Figure 5, program gates of FLOTOX type nonvolatile memory elements 202 to 205 are all coupled to a program gate terminal 211, and erase drains of the elements 202 to 205 are all connected to an erase drain terminal 221. Drains of the elements 202 and 203 are both coupled to a drain terminal 231. Sources of the elements 202 and 203 are all connected together with drains of the elements 204 and 205. Sources of the elements 204 and 205 are both grounded and the program gate terminal 211, the erase drain terminal 221 and the drain terminal 231 are connected to the lines 110, 120 and 130, respectively. The four cell FLOTOX type nonvolatile memory element performs the same operation as that of the FLOTOX type nonvolatile memory element shown in Figures 3 and 4.

The four cell FLOTOX type nonvolatile memory element shown in Figure 5 cannot work, if at least two of the four elements 202 to 205 are defective. Therefore, the probability, PT, that the four cell FLOTOX type nonvolatile memory element is defective can be given by the following equation.

$$PT = 2P^2 (1-P^2) + 4P^3 (1-P) + P^4 + 2P^2$$

wherein P is the probability that a one-cell FLOTOX nonvolatile memory element illustrated in Figures 3 and 4 produces a defect during the manufacturing process.

Generally, since the value of P is a small value of approximately 10^{-5} , the reliability of the four cell element shown in Figure 5 will increase by the order of 10^{-5} rather than by the reliability of one cell element illustrated in Figures 3 and 4.

Figure 6 shows a redundancy circuit diagram substituting a plurality of redundant row lines for a plurality of normal row lines. In Figure 6, each of a plurality of redundant row decoders 10A to 10I has the same structure as that of the redundant row decoder 10 illustrated in Figure 1 and normal decoders 20A to 20I are known NOR gate decoders.

Now, if we assume that normal memory cells on the normal row line 4A had defects, and row address program devices RAPDoA to RAPDi+1A were programmed so as to repair the bad cells by the address program, and row address signals for selecting the normal memory cells on the line 4A were delivered to the semiconductor chip, the signal on the redundant row line 3A would become a logic high level. Then, the output signal of a NAND gate formed of a NOR gate 5 and an inverter 6, which inputs signal on redundant row lines 3A to 3I, will be at a logic high level. Therefore, all output signals of the normal row decoders 20A to 20I connected to the output of the NAND gate will become logic low levels so as not to select the normal memory cells on the normal row lines 4A to 4I.

If all memory cells of the normal memory array are free of defect, by the reset program as mentioned above, all redundant row lines 3A to 3I will be at a logic low level so as not to select redundant memory cells.

While the above describes a preferred embodiment of the present invention, it will be apparent to those skilled in the art that the invention may be modified in numerous ways and may assume embodiments other than specifically set out and described above. For example, the input signals of the additional address program device can be complementary signals of the input signals of another one of the other address program devices.

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CLAIMS:

1. A semiconductor memory device comprising:
 - 5 a plurality of normal memory cells;
a plurality of redundant memory cells for the replacement of any defective ones of said normal memory cells;
 - 10 a normal decoder connected to receive a plurality of address signals and operative to address normal memory cells identified by said address signals; and
 - 15 a redundant decoder connected to receive said address signals and operative to output a redundant signal upon a redundant line in dependence upon said address signals, the redundant decoder comprising a plurality of first program devices connected in parallel
 - 20 between a reference potential and said redundant line and operative to output selectively said reference potential in dependence upon said address signals; and a second additional program device connected in parallel with said first program devices between said reference potential
 - 25 and said redundant line and operative to output selectively said reference potential, said second program device being connected to receive an input signal which is complementary to that of a selected one of said first program devices; the arrangement being such that, when
 - 30 the memory is addressed, then if none of said normal memory cells is defective, one of said one selected first program device and said second program device outputs said reference potential and, if at least one of said normal memory cells is defective, none of said first
 - 35 program devices and said second program device outputs



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said reference potential, the presence or absence of said reference potential at the output of said first and second program devices determining the presence or absence of said redundant signal upon said redundant
5 line, and the redundant signal being operative to enable or inhibit addressing of either the normal memory cells or the redundant memory cells accordingly.

2. A semiconductor memory device according to Claim
10 1, wherein said normal detector is connected to receive and respond to said redundant signal, and each of said first program devices is connected to receive a respective one of said address signals and its complement.

15 3. A semiconductor memory device according to Claim 2, wherein said second program device is connected to receive, in an inverse connection, the true and complementary address signals of said selected one of
20 said first program devices.

4. A semiconductor memory device according to Claim 1, 2 or 3, wherein said reference potential is ground.

25 5. A semiconductor memory device according to any of Claims 1 to 4, wherein each program device comprises a non-volatile memory element capable of assuming first and second program states.

30 6. A semiconductor memory device according to Claim 5, wherein each program device comprises:
a true address signal line;
a complementary address signal line;
a nonvolatile memory element having a program
35 gate terminal, erase drain terminal, a drain terminal and



source terminal which is grounded;

a first means, connected to said program gate terminal through an isolation transistor, for producing a high potential in a second program mode, a low potential
5 in a first program mode, and supplying a predetermined potential to said program gate terminal so that said memory element has better conduction during reading operation;

a second means, connected to said erase drain
10 terminal, for producing a high potential in said first program mode;

a third means, connected between said true address signal line and an input terminal of said isolation transistor, and between said complementary
15 address signal line and the input terminal of said isolation transistor, for supplying a sufficiently high potential to said input terminal that the high potential produced at the first means in said second program mode transfers to said program gate terminal, when said true
20 address signal is true, thereby causing a change of program state of said memory element as programmed in said first program mode, and producing a low potential to said input terminal, during said second program mode when said true address signal is complementary, thereby
25 causing no change of program state of said memory element as programmed in said first program mode; and

a sensing means, connected between said drain terminal and said true address signal line and said complementary address signal line, for grounding the
30 output line connected to said redundant line when said true address signal is true, and floating said output line when said true address signal is complementary.

7. A semiconductor memory device according to Claim
35 5 or 6, wherein said nonvolatile memory element comprises



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a plurality of nonvolatile memory devices of which program gates and erase drains are connected together with a program gate terminal and an erase drain terminal respectively, and of which drains of said devices
5 connected in parallel are connected to a drain terminal and of which source-drain junction points of said devices connected in series are connected together and of which other sources are grounded or connected to reference potential.

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8. A semiconductor memory device according to Claim 5, 6 or 7, wherein the or each said nonvolatile memory device is a FLOTOX type nonvolatile memory device.

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9. A semiconductor memory device according to Claim 6 or to Claim 6 together with Claim 7 or 8, wherein each of said first, second and third means comprises a high voltage pump circuit.

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10. A semiconductor memory device, substantially as hereinbefore described with reference to the accompanying drawings.

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