ABSTRACT OF THE DISCLOSURE

A memory device includes cell transistors on active regions defined by a device isolation layer on a substrate such that each cell transistor has a buried cell gate and a junction portion adjacent to and at least partially distal to the substrate in relation to the buried cell gate, an insulation pattern on the substrate and covering the cell transistors and the device isolation layer, and a bit line structure on the insulation pattern and connected to the junction portion. The bit line structure includes a buffer pattern on the pattern and having a thermal oxide pattern, a conductive line on the buffer pattern, and a contact extending from the conductive line to the junction portion through the buffer pattern and the insulation pattern.

FIG. 1