Description

The present invention relates to a frequency detector for detecting a signal which has been frequency-modulated by a digital signal and, more particularly, to a frequency detector suitable for an integrated circuit.

Implementations heretofore proposed for accomplishing a frequency detector in an integrated circuit configuration include a so-called direct conversion system. An advantage attainable with the direct conversion system is that it directly converts a received carrier wave to a baseband signal so as to allow filtering and other processings to be performed in the baseband. Signal processing in the baseband may be implemented by a well known method which relies on differentiation and multiplication. Although the differentiation and multiplication scheme advantageously demodulates even a signal which has been modulated by an analog signal great difficulty is experienced in realizing a circuit for practicing the method due to the need for gain control and balance of the circuitry particular thereto.

Concerning prior art constructions of the kind concerned, a reference may be made in U.S. Patent 4,322,851 (Vance) which shows in Fig. 4 a decoding logic circuit arrangement for an FSK (frequency shift keyed) receiver. The arrangement comprises two inverters, four NOR gates, two SR flip-flops, four D flip-flops, and two resistors. The problem with such an arrangement is that as many as 140 transistors are necessary in total in order to implement the circuit elements mentioned above, particularly all the gate elements, rendering the overall circuit bulky and, therefore, unsuitable for an integrated circuit. Meanwhile, U.K. Patent Application GB 2 106 359 A (Standard Telephones and Cables Limited) shows in Fig. 11a a demodulator construction furnished with an analog circuit section which includes a switch, resistors, a low pass filter and other elements. While the analog circuit section of the illustrated demodulator may be removed to produce a demodulated digital signal, spike noise is apt to appear in the output of the demodulator because of a delay difference between two baseband signals applied to an output, that is, an exclusive OR circuit.

Summary of the invention

It is therefore an object of the present invention to provide a frequency detector for the detection of a signal frequency-modulated by a digital signal which can be readily implemented by an integrated circuit.

It is another object of the present invention to provide a generally improved frequency detector.

A frequency detector for detecting a signal frequency-modulated by a digital signal of the present invention comprises a local oscillator device having a frequency substantially equal to a center frequency of the modulated signal, a frequency conversion device to which the modulated signal is inputted, for outputting 2N (N being a positive integer) baseband signals which are different in phase from each other, a digitizer for digitizing the 2N baseband signals to generate 2N digital signals, an Exclusive-OR gate supplied with the 2N digital signals, a signal provided by the Exclusive-OR means being assumed to be a first signal and, when the 2N digital signals are arranged in a modulo 180° order in phase, alternate ones of the signals being assumed to belong to a first signal group and the rest of the signals to a second signal group, a first pulse generator for generating a pulse every time a state of any of the signals in the first signal group is changed, a second pulse generator for generating a pulse every time a state of any of the signals in the second signal group is changed, a signal selector connected to the Exclusive-OR gate, the first pulse generator and the second pulse generator for selecting one of binary logical states if the state of the first signal is logical "1" at a time when the first pulse generator generates an output pulse or if the state of the first signal is logical "0" at a time when the second pulse generator generates an output pulse, and selecting the other of the logical states if the state of the first signal is logical "0" at a time when the first pulse generator generates an output pulse or if the state of the first signal is logical "1" at a time when the second pulse generator generates an output pulse, a signal developed from an output signal of the signal selector being provided as a detection output signal.

In accordance with the present invention, a frequency detector detects a signal which has been frequency-modulated by a digital signal. Digital logical elements are used for most of the sections which constitute a network for frequency detection and all of them operate in the baseband. Such a construction is readily attainable in an integrated circuit.

The above and other objects, features and advantages of the present invention will become apparent from the following detailed description taken with the accompanying drawings.

Brief description of the drawings

Fig. 1 is a block diagram of a frequency detector embodying the present invention;

Fig. 2 is a block diagram of a delayed pulse generator circuit applicable to the frequency detector shown in Fig. 1;

Fig. 3 shows waveforms of signals which appear in various portions of the frequency detector of Fig. 1;

Fig. 4 is a block diagram of a frequency detector in accordance with another embodiment of the present invention; and

Fig. 5 shows waveforms of signals which appear in various portions of the frequency detector of Fig. 4.

Description of the preferred embodiments

While the frequency detector of the present invention is susceptible of numerous physical

embodiments depending upon the environment and requirements of use, substantial numbers of the herein shown and described embodiments have been made, tested and used, and all have performed in an eminently satisfactory manner.

Referring to Fig. 1 of the drawings, a frequency detector of the present invention is shown and generally designated by the reference numeral 10. A received carrier wave which has undergone frequency modulation by a mark or space digital signal is applied to an input terminal 12. A local oscillator 14 produces an output whose frequency is substantially equal to the center frequency of the input carrier wave. The oscillator output is applied on one hand to a mixer 18 via a 90° phase shifter 16 and on the other hand to another mixer 20 so that the mixers 18 and 20, using the local oscillation signals which are different in phase by 90°, frequency-convert the input carrier wave to the baseband signal. The mixer 18 is connected to a low-pass filter (LPF) 22 and the mixer 20 to a low-pass filter (LPF) 24. Each of the LPF's 22 and 24 functions to pick up only a baseband signal in a desired channel and to band-limit the noise. The baseband signals output from the low-pass filters 22 and 24 respectively are applied to digitizers 26 and 28 which then produce digital signals Q and I. Since the phase difference between the input modulated signal and the local oscillation signal differs by 90° from the mixer 18 to the mixer 20, the signals I and Q are also different in phase by 90° from each other. Exemplary waveforms of the signals I and Q are shown in Fig. 3, in which the solid lines shows a case wherein the modulation signal is the mark and the phantom lines a case wherein the modulation signal is the space.

The signals I and Q are routed to an Exclusive-OR (Ex-OR) gate 30 which produces a signal IQ as shown in Fig. 3. At the same time, the signals I and Q are applied to delayed pulse generators 32 and 34, respectively. The delayed pulse generators 32 and 34 generate respectively pulse signals DI and DQ each of which is delayed by a time ΔT relative to a state transition time of the associated signal I or Q. If the output signal IQ of the Ex-OR gate 30 is (logical) "1", the pulse signal DI propagates through an AND gate 36 and an OR gate 38 to a set-reset flip-flop 40 to set it and, if the signal IQ is "0" and, therefore, an output of an inverter 42 is "1", the pulse signal DI passes through an AND gate 44 and an OR gate 46 to the flip-flop 40 to reset it.

Meanwhile, the pulse signal DQ, if the signal IQ is "1", passes through an AND gate 48 and an OR gate 46 to reset the set-reset flip-flop 40 and, if the signal IQ is "0" and, therefore, the output of the inverter 42 is "1", it propagates through an AND gate 50 and the OR gate 38 to the flip-flop 40 to set it. In this construction, as will be seen from Fig. 3, the flip-flop 40 is set if the modulation signal is a mark and reset if it is a space, a detection output appearing at an output terminal 52 of the flip-flop 40. In Fig. 1, a section 54 enclosed by a phantom line constitute a logic circuit.

The delayed pulse generators 32 and 34 may each be implemented by an arrangement shown in Fig. 2. As well known in the art, where the signal I or Q applied to an input terminal 200 is applied to an Ex-OR gate 204 directly on one hand and via a delay circuit 202 on the other hand, it is possible to generate a pulse signal at a transition point of the input signal. In the particular construction shown in Fig. 2, the pulse signal output from the Ex-OR 204 is further applied to a delay circuit 206 so that a signal DI (DQ) appears at an output terminal 208 with a delay of ΔT relative to the transition point of the signal I (Q). The purpose of the delay set up by the delay circuit 206 is to stabilize the operation by avoiding the neighborhood of the transition point of the signal IQ. Such a purpose, therefore, may also be served by inserting the delay circuit 206 in the signal IQ side. In that case, since only the sign of the detection output will be inverted, another inverter may be installed or the set and reset inputs to the flip-flop 40 may be replaced with each other.

In accordance with the embodiment described above, the phase difference between the signals I and Q is not limited to 90° and is open to choice if it is not zero. This will readily be understood by, for example, drawing such waveforms as those shown in Fig. 3. Further, the phase difference may be applied to the modulated carrier wave which is fed to the two mixers 22 and 24, instead of the output signals of the mixers 22 and 24.

Referring to Fig. 4, a frequency detector 60 in accordance with another embodiment of the present invention is shown. The operation of the frequency detector 60 will be described with reference also made to Fig. 5. The frequency modulated carrier wave is applied to an input terminal 62 of the frequency detector 60. A local oscillator 64 generates a signal whose frequency is substantially equal to the center frequency of the input modulated carrier wave. The output of the local oscillator 64 is applied to a phase splitter 66 to be thereby provided with phase differences of 0°, 45°, 90° and 135°. The four outputs of the splitter 66 respectively are fed to four mixers 68, 70, 72 and 74 as local oscillation signals, each of the mixers frequency-converting the input modulated carrier wave to the baseband signal on the basis of the associated local oscillation signal. The outputs of the mixers 68, 70, 72 and 74 respectively are passed through low pass filters 76, 78, 80 and 82 and, then, through digitizers 84, 86, 88 and 90. Let the outputs of the digitizers 84, 86, 88 and 90 be I_1, Q_1, I_2 and Q_2, respectively. These signals are different in phase from each other as shown in Fig. 5 by way of example. In Fig. 5, solid lines are associated with the mark and phantom lines with the space.

The signals I_1, Q_1, I_2 and Q_2 are commonly applied to an Ex-OR gate 92 the output IQ of which is shown in Fig. 5. The signals I_1 and Q_1 are also applied to an Ex-OR gate 94 and the signals I_2 and Q_2 to an Ex-OR gate 96 with the result that signals I_1Q_1 and I_2Q_2 are provided. The signals I_1Q_1 and I_2Q_2 respectively are applied to delayed pulse generators 98 and 100 which then produce

pulse signals DI_1Q_1 and DI_2Q_2 respectively. The pulse signals DI_1Q_1 and DI_2Q_2 are delivered to a logic circuit 102 together with the signal IQ, so that a detection output appears at an output terminal 104. In Fig. 4, the logic circuit 102 is identical with the logic circuit 54 of Fig. 1. In Figs. 4 and 5, regarding the signal DI_1Q_1 as a signal DI and the signal DI_2Q_2 as a signal DQ, it will be seen that the relationship between the signals DI and DQ and the signal IQ is the same as in the first embodiment and, hence, a detection output is produced at the output terminal 104.

While the second embodiment shown in Figs. 4 and 5 is somewhat intricate in construction compared to the first embodiment, it is advantageously applicable to a modulated carrier wave whose phase transition rate per data repetition period is low, i.e., a modulated carrier wave with a smaller modulation index.

The detection described above is achievable even if the number of the baseband signals is increased to 2N, as will be understood by analogy from the operation of the second embodiment. Also, it will be easily confirmed that such an operation is accomplished even with unequal differences between the phases of the baseband signals. Considering the fact that the logical "1" and "0" of the signal IQ alternate with each other every time one of the numerous baseband signals changes its state, what is required for adequate operation is, assuming baseband signals arranged in order of phase, to identify a state of the signal IQ every time the state of one of alternate signals selected out of all the arranged signals is changed. Care should be taken in so arranging the phases of the signals so that those signals with phases larger than 180° are arranged after subtracting 180° from their actual phases, i.e., in a modulo 180° order. This will readily be understood by drawing signal waveforms.

In summary, it will be seen that the present invention provides a frequency detector which can be implemented by an integrated circuit because all the circuit elements after mixers operate in a baseband and because the section after digitizers is implemented by a digital circuit. In addition, the circuitry succeeding the baseband circuit may be realized by once digitizing the signals and, then, performing the signal processing in accordance with the present invention by use of a microprocessor.

Claims

1. A frequency detector for detecting a signal frequency-modulated by a digital signal, comprising:

local oscillator means (14) having a frequency substantially equal to a center frequency of the modulated signal;

frequency conversion means (16—20) to which the modulated signal is inputted for outputting 2N (N being a positive integer) baseband signals which are different in phase from each other;

digitizer means (26, 28) for digitizing the 2N baseband signals to generate 2N digital signals;

Exclusive-OR means (30) supplied with the 2N digital signals;

a signal (IQ) provided by said Exclusive-OR means (30) being assumed to be a first signal and, when the 2N digital signals are arranged in a modulo 180° order in phase, alternate ones of the signals being assumed to belong to a first signal group ($I_3I_1Q_1$) and the rest of the signals to a second signal group (Q; I_2 Q_2),

first pulse generator means (32; 98)' for generating a pulse every time a state of any of the signals in the first signal group is changed;

second pulse generator means (34; 100) for generating a pulse every time a state of any of the signals in the second signal group is changed;

signal selector means (54; 102) connected to said Exclusive-OR means, said first pulse generator means (32; 98) and said second pulse generator means (34; 100) for selecting one of binary logical states if the state of the first signal (IQ) is logical "1" at a time when the first pulse generator means (32; 98) generates an output pulse or if the state of the first signal (IQ) is logical "0" at a time when the second pulse generator means (34; 100) generates an output pulse, and selecting the other of the logical states if the state of the first signal (IQ) is logical "0" at a time when the first pulse generator means (32; 98) generates an output pulse or if the state of the first signal (IQ) is logical "1" at a time when the second pulse generator means (34; 100) generates an output pulse;

a signal developed from an output signal of the signal selector means being provided as a detection output signal.

2. A frequency detector as claimed in claim 1, further comprising means for branching an output of the local oscillator means into 2N signals and applying predetermined phase differences to the branched signals.

3. A frequency detector as claimed in claim 2, wherein N is one, the predetermined phase differences being commonly 90°.

4. A frequency detector as claimed in claim 2, wherein N is two, the predetermined phase differences being 0°, 45°, 90° and 135°.

5. A frequency detector as claimed in any of claims 1 to 4, further comprising means for separating particular one of the baseband signals only.

6. A frequency detector as claimed in claim 5, wherein said means comprises a low pass filter.

7. A frequency detector as claimed in any of claims 1 to 6, wherein the frequency conversion means comprises mixer means.

8. A frequency detector as claimed in any of claims 1 to 7, wherein each of the first and second pulse generator means is constructed to generate the pulse before the time of change in the state of the first signal.

9. A frequency detector as claimed in any of claims 1 to 7, wherein each of the first and

pulse signals DI_1Q_1 and DI_2Q_2 respectively. The pulse signals DI_1Q_1 and DI_2Q_2 are delivered to a logic circuit 102 together with the signal IQ, so that a detection output appears at an output terminal 104. In Fig. 4, the logic circuit 102 is identical with the logic circuit 54 of Fig. 1. In Figs. 4 and 5, regarding the signal DI_1Q_1 as a signal DI and the signal DI_2Q_2 as a signal DQ, it will be seen that the relationship between the signals DI and DQ and the signal IQ is the same as in the first embodiment and, hence, a detection output is produced at the output terminal 104.

While the second embodiment shown in Figs. 4 and 5 is somewhat intricate in construction compared to the first embodiment, it is advantageously applicable to a modulated carrier wave whose phase transition rate per data repetition period is low, i.e., a modulated carrier wave with a smaller modulation index.

The detection described above is achievable even if the number of the baseband signals is increased to 2N, as will be understood by analogy from the operation of the second embodiment. Also, it will be easily confirmed that such an operation is accomplished even with unequal differences between the phases of the baseband signals. Considering the fact that the logical "1" and "0" of the signal IQ alternate with each other every time one of the numerous baseband signals changes its state, what is required for adequate operation is, assuming baseband signals arranged in order of phase, to identify a state of the signal IQ every time the state of one of alternate signals selected out of all the arranged signals is changed. Care should be taken in so arranging the phases of the signals so that those signals with phases larger than 180° are arranged after subtracting 180° from their actual phases, i.e., in a modulo 180° order. This will readily be understood by drawing signal waveforms.

In summary, it will be seen that the present invention provides a frequency detector which can be implemented by an integrated circuit because all the circuit elements after mixers operate in a baseband and because the section after digitizers is implemented by a digital circuit. In addition, the circuitry succeeding the baseband circuit may be realized by once digitizing the signals and, then, performing the signal processing in accordance with the present invention by use of a microprocessor.

Claims

1. A frequency detector for detecting a signal frequency-modulated by a digital signal, comprising:

local oscillator means (14) having a frequency substantially equal to a center frequency of the modulated signal;

frequency conversion means (16—20) to which the modulated signal is inputted for outputting 2N (N being a positive integer) baseband signals which are different in phase from each other;

digitizer means (26, 28) for digitizing the 2N baseband signals to generate 2N digital signals;

Exclusive-OR means (30) supplied with the 2N digital signals;

a signal (IQ) provided by said Exclusive-OR means (30) being assumed to be a first signal and, when the 2N digital signals are arranged in a modulo 180° order in phase, alternate ones of the signals being assumed to belong to a first signal group ($I_3I_1Q_1$) and the rest of the signals to a second signal group (Q; I_2 Q_2),

first pulse generator means (32; 98)' for generating a pulse every time a state of any of the signals in the first signal group is changed;

second pulse generator means (34; 100) for generating a pulse every time a state of any of the signals in the second signal group is changed;

signal selector means (54; 102) connected to said Exclusive-OR means, said first pulse generator means (32; 98) and said second pulse generator means (34; 100) for selecting one of binary logical states if the state of the first signal (IQ) is logical "1" at a time when the first pulse generator means (32; 98) generates an output pulse or if the state of the first signal (IQ) is logical "0" at a time when the second pulse generator means (34; 100) generates an output pulse, and selecting the other of the logical states if the state of the first signal (IQ) is logical "0" at a time when the first pulse generator means (32; 98) generates an output pulse or if the state of the first signal (IQ) is logical "1" at a time when the second pulse generator means (34; 100) generates an output pulse;

a signal developed from an output signal of the signal selector means being provided as a detection output signal.

2. A frequency detector as claimed in claim 1, further comprising means for branching an output of the local oscillator means into 2N signals and applying predetermined phase differences to the branched signals.

3. A frequency detector as claimed in claim 2, wherein N is one, the predetermined phase differences being commonly 90°.

4. A frequency detector as claimed in claim 2, wherein N is two, the predetermined phase differences being 0°, 45°, 90° and 135°.

5. A frequency detector as claimed in any of claims 1 to 4, further comprising means for separating particular one of the baseband signals only.

6. A frequency detector as claimed in claim 5, wherein said means comprises a low pass filter.

7. A frequency detector as claimed in any of claims 1 to 6, wherein the frequency conversion means comprises mixer means.

8. A frequency detector as claimed in any of claims 1 to 7, wherein each of the first and second pulse generator means is constructed to generate the pulse before the time of change in the state of the first signal.

9. A frequency detector as claimed in any of claims 1 to 7, wherein each of the first and

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second pulse generator means is constructed to generate the pulse after the time of change in the state of the first signal.

10. A frequency detector as claimed in any of claims 1 to 9, wherein the signal selector means comprises a digital circuit.

Patentansprüche

1. Frequenzdetektor zum Detektieren eines Signals, das durch ein Digitalsignal frequenzmoduliert worden ist, mit

einem lokalen Oszillator (14) dessen Frequenz im wesentlichen gleich einer Mitelfrequenz des modulierten Signals ist,

einem Frequenzkonverter (16—20), dem das modulierte Signal zugeführt wird, um 2N (N=eine positive ganze Zahl) Basisbandsignale abzugeben, die sich in ihrer Phase voneinander unterscheiden,

einem Digitalisierer (26, 28) zum Digitalisieren der 2N Basisbandsignale und Erzeugen von 2N Digitalsignalen,

eine Exklusiv-ODER-Einrichtung (30), der die 2N Digitalsignale zugeführt werden,

einem von der Exklusiv-ODER-Einrichtung (30) abgegebenen signal (IQ), das als ein erstes Signal angesehen wird, und, wenn die 2N Digitalsignale in einer Modulo-180°-Phasenordnung angeordnet sind, Alternativsignalen, die als Signale angesehen werden, die zu einer ersten Signalgruppe (I; I_1 Q_1) gehören, während die übrigen Signale zu einer zweiten Signalgruppe (Q; I_2 Q_2) gehören,

einem ersten Impulsgenerator (32; 98) zum Erzeugen eines Impulses jedesmal dann, wenn sich ein Zustand eines der Signale in der ersten Signalgruppe andert,

einem zweiten Impulsgenerator (34; 100) zum Erzeugen eines Impulses jedesmal dann, wenn sich ein Zustand eines der Signale in der zweiten Signalgruppe andert,

einem Signalselektor (54; 102), der mit der Exklusiv-ODER-Einrichtung, dem ersten Impulgenerator (32; 98) und dem zweiten Impulsgenerator (34; 100) verbunden ist, um einen der binaren Logikzustände auszuwählen, wenn der Zustand des ersten Signals (IQ) logisch "1" ist, wenn der erste Impulsgenerator (32; 98) einen Ausgangsimpuls erzeugt, oder wenn der Zustand des ersten Signals (IQ) logisch "0" ist, wenn der zweite Impulsgenerator (34; 100) einen Ausgangsimpuls erzeugt, und Selektieren des anderen Logikzustandes, wenn der Zustand des ersten Signals (IQ) logisch "0" ist, wenn der erste Impulsgenerator (32; 98) einen Ausgangsimpuls erzeugt, oder wenn der Zustand des ersten Signals (IQ) logisch "1" ist, wenn der zweite Impulsgenerator (34; 100) einen Ausgangsimpuls erzeugt,

wobei ein aus einem Ausgangssignal des Signalselektors abgeleitetes Signal als Detektionsausgangssignal abgegeben wird.

2. Frequenzdetektor nach Anspruch 1 mit einer Einrichtung zum Verzweigen eines Ausgangssignals des lokalen Oszillators in 2N Signale und Zuordnen vorgegebener Phasendifferenzen zu den verzweigten Signalen.

3. Frequenzdetektor nach Anspruch 2, dadurch gekennzeichnet, daß N=1 und daß die vorgegebenen Phasendifferenzen jeweils 90° betragen.

4. Frequenzdetektor nach Anspruch 2, dadurch gekennzeichnet, daß N=2 und daß die vorgegebenen Phasendifferenzen 0°, 45°, 90° und 135° betragen.

5. Frequenzdetektor nach einem der Ansprüche 1 bis 4, gekennzeichnet durch eine Einrichtung zum Separieren lediglich eines bestimmten Signale aus den Basisbandsignalen.

6. Frequenzdetektor nach Anspruch 5, dadurch gekennzeichnet, daß die Einrichtung einen Tiefpassfilter aufweist.

7. Frequenzdetektor nach einem der Ansprüche 1 bis 6, dadurch gekennzeichnet, daß der Frequenzkonverter einen Mischer aufweist.

8. Frequenzdetektor nach einem der Ansprüche 1 bis 7, dadurch gekennzeichnet, daß sowohl der erste als auch der zweite Impulsgenerator so ausgebildet sind, daß sie den Impuls erzeugen bevor sich der Zustand des ersten Signals ändert.

9. Frequenzdetektor nach einem der Ansprüche 1 bis 7, dadurch gekennzeichnet, daß sowohl der erste als auch der zweite Impulsgenerator so ausgebildet sind, daß sie den Impuls erzeugen, nachdem sich der Zustand des ersten Signals geändert hat.

10. Frequenzdetektor nach einem der Ansprüche 1 bis 9, dadurch gekennzeichnet, daß der Signalselektor einen Digitalschaltkreis aufweist.

Revendications

1. Détecteur de fréquence pour détecter un signal modulé en fréquence par un signal numérique, comprenant:

un moyen d'oscillateur local (14) ayant une fréquence sensiblement égale à une fréquence centrale du signal modulé;

un moyen de conversion de fréquence (16—20) dans lequel le signal modulé est entré afin de sortir 2N (N étant un nombre entier positif) signaux en bande de base qui sont différents en phase les uns des autres;

un moyen de numérisation (26, 28) pour numériser les 2N signaux en bande de base pour produire 2N signaux numériques;

un moyen OU Exclusif (30) alimenté avec les 2N signaux numériques;

un signal (IQ) fourni par le moyen OU Exclusif (30) étant supposé être un premier signal et, lorsque les 2N signaux numériques sont disposés dans un ordre de phase modulo 180°, des signaux alternés parmi les signaux étant supposés appartenir à un premier groupe de signaux (I; I_1 Q_1) et le reste des signaux à un second groupe de signaux (Q; I_2 Q_2);

un premier moyen de générateur d'impulsions (32; 98) pour produire une impulsion chaque fois que l'état de l'un quelconque des signaux du premier groupe de signaux est changé;

un second moyen de générateur d'impulsions (34; 100) pour produire une impulsion chaque fois que l'état de l'un quelconque des signaux du

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second groupe de signaux est changé;

un moyen de sélecteur de signal (54; 102) connecté au moyen OU Exclusif, au premier moyen de générateur d'impulsions (32; 98) et au second moyen de générateur d'impulsions (34; 100) pour choisir l'un des états logiques binaires si l'état du premier signal (IQ) est le niveau logique "1" à l'instant où le premier moyen de générateur d'impulsions (32; 98) produit une impulsion de sortie ou si l'état du premier signal (IQ) est le niveau logique "0" à l'instant où le second moyen de générateur d'impulsions (34; 100) produit une impulsion de sortie, et pour choisir l'autre des états logiques si l'état du premier signal (IQ) est le niveau logique "0" à l'instant où le premier moyen de générateur d'impulsions (32; 98) produit une impulsion de sortie ou si l'état du premier signal (IQ) est le niveau logique "1" à l'instant où le second moyen de générateur d'impulsions (34; 100) produit une impulsion de sortie;

un signal développé à partir d'un signal de sortie du moyen de sélecteur de signal étant fourni comme signal de détection de sortie.

2. Détecteur de fréquence selon la revendication 1, comprenant en outre un moyen pour ramifier une sortie du moyen d'oscillateur local en 2N signaux et appliquer des différences de phase prédéterminées aux signaux ramifiés.

3. Détecteur de fréquence selon la revendication 2, dans lequel N est un, les différences de phase prédéterminées étant généralement 90°.

4. Détecteur de fréquence selon la revendication 2, dans lequel N est deux, les différences de phase prédéterminées étant 0°, 45°, 90° et 135°.

5. Détecteur de fréquence selon l'une quelconque des revendications 1 à 4, comprenant en outre un moyen pour séparer seulement un signal particulier des signaux en bande de base.

6. Détecteur de fréquence selon la revendication 5, dans lequel le moyen comprend un filtre passe-bas.

7. Détecteur de fréquence selon l'une quelconque des revendications 1 à 6, dans lequel le moyen de conversion de fréquence comprend un moyen de mélangeur.

8. Détecteur de fréquence selon l'une quelconque des revendications 1 à 7, dans lequel chacun des premier et second moyens de générateur d'impulsions est construit pour produire l'impulsion avant l'instant du changement de l'état du premier signal.

9. Détecteur de fréquence selon l'une quelconque des revendications 1 à 7, dans lequel chacun des premier et second moyens de générateur d'impulsions est construit pour produire l'impulsion après l'instant du changement de l'état du premier signal.

10. Détecteur de fréquence selon l'une quelconque des revendications 1 à 9, dans lequel le moyen de sélecteur de signal comprend un circuit numérique.

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