CLAIMS

WHAT IS CLAIMED IS:

1. An interface device between a plurality of memory devices and a memory controller, the interface device comprising:

processing circuitry configured to

provide a plurality of controller channels for communicating with the memory controller;

provide a plurality of memory channels for communicating with the plurality of memory devices;

connect each of the plurality of controller channels to at least one of the plurality of memory channels in a first mode; and

disconnect at least one of the plurality of controller channels from the plurality of memory channels in a second mode,

wherein in the second mode, a connected controller channel of the plurality of controller channels is configured to output at least one of a retiming signal or a clock signal.

2. The interface device of claim 1, wherein the processing circuitry is configured to be set to the first mode or the second mode based on a first signal received from outside of the interface device.

3. The interface device of claim 2, further comprising at least one dedicated pin exposed to the outside of the interface device and configured to receive the first signal.

4. The interface device of claim 2 or claim 3,

wherein the processing circuitry comprises a register configured to be set based on the first signal,

wherein the first signal is received through at least one of the plurality of controller channels.

5. The interface device of any one of claims 1 to 4, wherein

the plurality of controller channels includes a first controller channel and a second

controller channel,

the plurality of memory channels include a first memory channel, a second memory channel, a third memory channel, and a fourth memory channel, and

the processing circuitry is configured to connect the first controller channel to the first and second memory channels and to connect the second controller channel to the third and fourth memory channels, in the first mode, and to connect the first controller channel to the first, second, third, and fourth memory channels and disconnect the second controller channel from the first, second, third, and fourth memory channels, in the second mode.

6. The interface device of any one of claims 1 to 4, wherein

the plurality of controller channels include a first controller channel and a second controller channel,

the plurality of memory channels include a first memory channel and a second memory channel, and

the processing circuitry is configured to respectively connect the first and second controller channels to the first and second memory channels, in the first mode, and to connect the first controller channel to the first and second memory channels and disconnect the second controller channel from the first and second memory channels, in the second mode.

7. The interface device of any one of claims 1 to 6, wherein the processing circuitry is configured to mirror data lines included in each of the plurality of controller channels based on a second signal received from outside of the interface device.

8. The interface device of any one of claims 1 to 7, wherein the processing circuitry includes

a first plurality of buffers respectively corresponding to the plurality of controller channels, and a second plurality of buffers respectively corresponding to the plurality of memory channels.

9. The interface device of any one of claims 1 to 8, wherein the plurality of controller channels and the plurality of memory channels are based on a same protocol.

10. A memory package comprising:

a plurality of memory devices; and

at least one interface device between the plurality of memory devices and a memory controller, the at least one interface device being configured to provide a plurality of controller channels for communicating with the memory controller and a plurality of memory channels for communicating with the plurality of memory devices,

wherein the at least one interface device is configured to, in a first mode, connect each of the plurality of controller channels to at least one of the plurality of memory channels, and in a second mode, disconnect at least one of the plurality of controller channels from the plurality of memory channels, and

wherein the at least one interface device is configured to mirror data lines included in each of the plurality of controller channels based on a second signal received from outside of the memory package.

11. The memory package of claim 10, wherein the at least one interface device is configured to be set to the first mode or the second mode based on a first signal received from outside of the memory package.

12. The memory package of claim 10 or claim 11, wherein

the at least one interface device is configured to provide first and second controller channels, and first, second, third, and fourth memory channels, and

in the first mode, to connect the first controller channel to the first and second memory channels and connect the second controller channel to the third and fourth memory channels, and

in the second mode, to connect the first controller channel to the first, second, third, and fourth memory channels and disconnect the second controller channel from the first, second, third, and fourth memory channels.

13. The memory package of any one of claims 10 to 12, further comprising

a printed circuit board; and

spacers mounted on an upper surface of the printed circuit board,

wherein the at least one interface device is mounted on the upper surface of the printed circuit board between the spacers, and

the plurality of memory devices are stacked on the spacers and the at least one interface device.

14. A memory system comprising:

a memory controller configured to provide a host channel for communicating with a host; and

a first memory package comprising a plurality of memory devices and an interface device, the interface device configured to set a number of controller channels based on a first signal received from outside of the first memory package, the controller channels being for communicating with the memory controller,

wherein the memory controller and the plurality of memory devices are configured to communicate with each other through at least one controller channel enabled by the interface device,

wherein the memory controller is configured to provide the first signal to the first memory package through the at least one controller channel enabled by the interface device, and

the interface device comprises a register to be set based on the first signal.

15. The memory system of claim 14, further comprising:

a printed circuit board on which the memory controller and the first memory package are mounted,

wherein the first memory package further comprises at least one dedicated pin contacting a pad of the printed circuit board, the at least one dedicated pin configured to receive the first signal.

16. The memory system of claim 15, wherein the printed circuit board comprises a pattern configured to pull-up and pull-down the at least one dedicated pin.

17. The memory system of claim 15, wherein

the printed circuit board comprises at least one pattern for connecting the memory controller to the at least one dedicated pin, and

the memory controller is configured to provide the first signal through the at least one pattern.

18. The memory system of any one of claims 14 to 17, wherein the first memory package comprises at least one pin corresponding to a disabled controller channel and disconnected from the memory controller.

19. The memory system of claim 14, further comprising:

a printed circuit board, the first memory package mounted on an upper surface of the printed circuit board; and

a second memory package commonly connected to a first controller channel with the first memory package, the second memory package mounted on a lower surface of the printed circuit board,

wherein the interface device of the first memory package is configured to mirror data lines included in each of the set controller channels based on a second signal received from the outside.