

PATENT SPECIFICATION

(11) 1344871

- (21) Application No. 20493/71 (22) Filed 19 April 1971
(31) Convention Application No. 12262 (32) Filed 18 Feb. 1970 in
(33) United States of America (US)
(44) Complete Specification published 23 Jan. 1974
(51) International Classification G11C 17/00
(52) Index at acceptance
G4A 10EX 17B4
H1K 211 217 422 511 514 515 52Y 541 543 54Y 551
552 555 55Y 563 566 581 583 596 599



(54) IMPROVEMENTS IN OR RELATING TO READ ONLY MEMORY CIRCUITS

(71) We, HEWLETT-PACKARD COMPANY, a corporation organised and existing under the laws of the State of California, United States of America, of 1501 Page Mill Road, Palo Alto, California 94304, United States of America, do hereby declare the invention for which we pray that a Patent may be granted to us and the method by which it is to be performed, to be particularly described in and by the following statement:—

This invention is concerned with improvements in or relating to coincident select read only memories.

Read only memories (ROM) are being used increasingly in a variety of applications including character generation, logic control, code conversion, arithmetic logic, and the like. One form of ROM structure is disclosed in U.S. Patent Specification no. 3381279. This ROM system is constructed using four individual circuit boards, one for a memory array, one for pulse drivers, one for switching circuits, and an additional one for sense amplifier circuitry. There are over 100 interconnections between the core memory circuit board and the other boards, and the cycle time of operation for this memory is over 100 nanoseconds. The increased utilization of ROM circuits requires a faster access time, a smaller package size, and a lower cost.

The present invention provides a bipolar read only memory comprising a first plurality of address lines, an orthogonally-oriented second plurality of address lines, a first plurality of transistors arranged in a plurality of orthogonally oriented rows and columns, each of said first plurality of transistors having a base, a collector and an emitter, the bases of the transistors in each row of said first plurality of transistors being coupled in common to a different one of said first plurality of address lines, the collectors of said first plurality of transistors being connected in common to a source of supply voltage, the emitters of selected transistors in

each column of said first plurality of transistors being coupled in common to a different one of said second plurality of address lines, first address means coupled to said first plurality of address lines for energizing a selected one of said first plurality of address lines, second address means coupled to said second plurality of address lines for selecting one or more but less than all of said second plurality of address lines, output means including a second plurality of transistors for detecting the presence or absence of current through each of said first plurality of transistors addressed by said selected one of said first plurality of address lines and said selected one or more of said second plurality of address lines, each of said second plurality of transistors being coupled to a different one of said second plurality of address lines.

Preferably in a memory as set forth in the last preceding paragraph the bases of the transistors in each row of said first plurality of transistors comprise a common base diffusion stripe and the emitters of the transistors in each row of said first plurality of transistors comprise separate emitter diffusion regions spaced apart along the base diffusion stripe of that row.

Preferably in a memory as set forth in the last preceding paragraph said second plurality of address lines comprises a plurality of metal lines, each of said metal lines extending over and being insulated from the emitter diffusion regions of the transistors in a different column of said first plurality of transistors and being connected to selected ones of these emitter diffusion regions by connections extending through openings in the insulation between the metal lines and the emitter diffusion regions.

Preferably in a memory as set forth in the last preceding paragraph but two said first plurality of transistors is formed in an isolation well of a semiconductor chip, said isolation well serves as a common collector for said first plurality of transistors, the bases of the transistors in each row of said first

plurality of transistors comprise a separate common base diffusion stripe extending across said isolation well in one direction, the emitters of the transistors in each row of said first plurality of transistors comprise separate emitter diffusion regions spaced apart along the base diffusion stripe of that row, said first plurality of address lines comprises said base diffusion stripes, and said second plurality of address lines comprises spaced-apart metal lines extending across said isolation well orthogonal to said base diffusion stripes, each of said metal lines extending over and being insulated from the emitter diffusion regions of the transistors in a different column of said first plurality of transistors and being connected to selected ones of these emitter diffusion regions by connections extending through openings in the insulation between the metal lines and the emitter diffusion regions at selected points where the metal lines overlie the emitter diffusion regions.

Preferably in a memory as set forth in the last preceding paragraph but three or in the last preceding paragraph said first address means comprises a first address decoder circuit having a plurality of outputs, said second address means comprises a second address decoder circuit having a plurality of outputs, and said output means comprises one or more output circuits coupled by said second plurality of transistors to said second plurality of address lines.

Preferably in a memory as set forth in the last preceding paragraph each of said second plurality of transistors has a base, a collector, and an emitter, the base of each of said second plurality of transistors being coupled to a different output of said second address decoder circuit, the collector of each of said second plurality of transistors being coupled to a different one of said second plurality of address lines, and the emitters of said second plurality of transistors being coupled in common to an output circuit. Alternatively said second plurality of transistors is arranged in a plurality of grains and each of said second plurality of transistors has a base, a collector, and an emitter, the bases of said second plurality of transistors being coupled in common to a source of reference voltage, the collectors of the transistors in each group of said second plurality of transistors being coupled in common to a different output circuit, the emitter of each of said second plurality of transistors being coupled to a different one of said second plurality of address lines, and the emitter of each transistor in each group of said second plurality of transistors also being coupled to a different output of said second address decoder circuit.

Preferably in a memory as set forth in the last preceding paragraph but five, or the last

preceding paragraph but two or the last preceding paragraph but one said first address means comprises a plurality of AND circuits, each of said AND circuits including a plurality of inputs, an output coupled to one of said first and second plurality of address lines, an input transistor having a base coupled to said output, a collector coupled to a source of supply voltage, and a plurality of separate emitters coupled to said inputs, and an output emitter follower transistor having a collector coupled to a source of supply voltage, a base coupled to the collector of said input transistor, and an emitter coupled to said output.

Preferably in a memory as set forth in the last preceding paragraph but six, or the last preceding paragraph but three, or the last preceding paragraph but two includes a plurality of inverter circuits, each of said inverter circuits including an input, an output coupled to one of said first and second address means, first and second transistors, each of said first and second transistors having a base, a collector, and an emitter, the base of said first transistor being coupled by a first circuit to said input, the collector of said first transistor being coupled in common with the emitter of said second transistor to said output, the emitter of said first transistor being coupled to a source of reference voltage, the collector of said second transistor being coupled to a source of supply voltage, and control means coupled to said input and to the base of said second transistor, said control means being responsive to a change in state of an input signal applied to said input for turning said second transistor off before said first transistor is turned on.

Preferably in a memory as set forth in the last preceding paragraph said control means comprises a third transistor having a base, a collector, and an emitter, the base of said third transistor being coupled by a second circuit to said input, the collector of said third transistor being coupled to the base of said second transistor, the emitter of said third transistor being coupled to a source of reference voltage, said second circuit and said third transistor operating to turn said second transistor off before said first circuit operates to turn said first transistor on and operating to turn said second transistor on after said first circuit operates to turn said first transistor off.

Two examples of the present invention will now be hereinafter described with reference to the accompanying drawings, in which:

Figure 1 is a block diagram of a logic organization of one form of read only memory (ROM) made in accordance with the present invention;

Figure 2 (i.e. Figures 2A, 2B and 2C) is a schematic diagram showing the ROM of Figure 1 in more detail;

Figure 3A is a plan view of a portion of

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the memory array showing the intersection of the metal lines and the base stripes;

Figures 3B, C and D are cross section views of the portion of the memory array taken through section lines B—B, C—C and D—D, respectively, in Figure 3A;

Figure 4 is a block diagram of another form of ROM providing a plurality of formats; and

Figure 5 (i.e. Figures 5A and 5B) is a schematic diagram of a portion of the ROM of Figure 4 showing the bit detector circuitry.

Referring now to Figure 1, the integrated circuit read only memory comprises five Y and five X input buffer-inverter circuits 11 and 12 respectively, address decoders 13 and 14, a memory cell array 15, bit detectors 16 and an output driver 17. The input buffer-inverter circuits 11 and 12 generate true and

complement output signals Y and $\bar{Y}$ and X and $\bar{X}$, respectively, for each of the five input signals to each circuit. The ten output signals from each of the input buffers 11 and 12 are fed into the associated address decoders 13 and 14, respectively, each of which comprises thirty-two multi-input AND gates.

The address decoders 13 and 14 allow access to any desired coincidence location in the 32×32 memory cell array. The thirty-two bit detectors 16 sense the state of the addressed memory cell array 15 and feed this information to the output driver 17 which may, for example, provide signal amplification, quantization, and level restoration. Bit organization with a linear select array in an ROM of 1024×1 format would require 1024 address decoders; the coincident select array reduces the number of address decoders to 64.

In optimizing the construction of a high speed integrated circuit ROM there are a number of design criteria to be considered. Four of the major criteria are the minimization of the circuit power dissipation, signal propagation delay, circuit area, and the pad or output interconnection count. Minimizing the power dissipation and the signal propagation delay are conflicting criteria, the well-known power/delay trade-off. For example, reduction of RC time constants by reduction of resistance results in increased power consumption. In the present integrated circuit ROM, emitter followers are utilized to achieve a fast switching action and good capacitive driving capability without incurring excessive power consumption. Power switching techniques may be utilized in the address decoders to obtain power reduction without degrading the speed. Minimization of active and passive device area while retaining adequate current handling capability leads to reduced capacitances and higher speeds. Schottky diodes may be used to reduce stor-

age time and therefore to improve high speed performance. Thus, a combination of selected circuit, component and processing techniques are employed to minimize power dissipation and propagation delay times in the ROM.

The third criterion, that of minimizing circuit area, not only serves to reduce fabrication costs but also leads to improved high speed performance, due to reduced capacitances at the switching nodes. In the ROM reduced circuit area has been achieved by the straightforward shrinkage of component area, consistent with known integrated circuit masking and diffusion tolerances, and also by careful logic organization and circuit design optimized for minimum area. The use of a coincident select structure rather than some other non-coincident select structure results in a considerable reduction in the number of addressed decoders and thus in the circuit area. In addition, the collectors of the memory cell array circuit described hereinafter are designed to occupy a single common-collector isolation, hence reducing the necessary area to about 1 square mil per cell. Also, the bit pattern for the memory cell array is specified by programmable (selectively positionable) contact openings in the silicon dioxide insulation layer, rather than by using a programmable metal mask. In this manner, when the metal line conductors are laid down, connection is made to the desired emitters through the contact openings in the insulation layer. This interconnection method alone reduces the size of the memory cell array by close to one half.

The fourth criterion, that of minimizing pad interconnection count, is met in an ROM array by fabrication of the complete ROM array on one chip. Although on-chip address inversion and decoding is in direct conflict with considerations of minimum power and minimum circuit area, the advantages of the fully on-chip fabrication justify any extra power and circuit area that may result. For example, with on-chip decoding, the ROM is much easier to test since there are considerably fewer pads to probe. In addition, the complete chip may be mounted on standard 16 dual in-line packages, as opposed to the prior approaches involving multi-chip assembly on complex multi-layer substrates, thus reducing packaging costs and minimizing the complexity of package-to-package interconnections.

The ROM results in the use of a minimum circuit area and an optimum power/delay product figure of merit. In the embodiments shown in this application a total bit capacity of 1024 bits per chip is shown, with bit $\times$ word format flexibility including 4×256 , 2×512 , and 1×1024 . Since these formats require 8, 9 and 10 inputs and 4, 2 and 1 outputs, respectively, then, together with power supply, ground, and chip select lines, the ROM chips

are easily assembled on 14 or 16 lead dual in-line packages.

Referring now to Figure 2, there is shown a complete ROM circuit fabricated on a single semiconductor chip 112×112 mils square. The circuit components include NPN transistors and diffused resistors. If desired, Schottky diodes may be utilized in parallel with the base-collector junctions for reduced storage time and therefore increased speed. Each input buffer circuit 11 and 12 comprises two output transistors T1 and T2 providing an output at their emitter-collector connection. The input resistor ratios R1:R2 and R3:R4 are chosen so that the transistor T3 coupled to the base of T1 turns on before transistor T2, and hence the base of transistor T1 goes to low voltage before T2 turns on, thus minimizing supply current spikes which can occur with active load output stages. The use of an active load transistor T1 results in a low output impedance in both the high and low logic states giving high fanout and capacitive driving capability. The resistors in the input inverter have the following values (in ohms): R1, 2K, R2, 2.6K; R3, 1.6K; R4, 1.5K, and R10, 2.8K. With signal propagation delays of about 5 nanoseconds and average power dissipation of about 10 milliwatts, this circuit provides high speed, and low power performance in a small area (only two collector isolation areas). In conjunction with the high input impedance buffers, a high performance input buffer-inverter is realized in about 100 square mils of area.

The address decoder 13 provides high performance with circuit simplicity. Both the true and complement address signals Y and

Y are fed via metal connecting lines to the emitters 18 of associated multiple emitter transistors such as T4. Programmable contact openings in the insulation layer allow the emitters 18 to make connection with either true or complement signals from the address inputs to generate the appropriate function at the decoder output. The emitter follower T5 in each AND circuit provides a low output impedance without requiring resistor R5 (3.8K) to be of low value, resulting in fast switching action for the AND gate with reduced power dissipation. In operation, both T4 and T5 operate in an active region, thus minimizing delay and storage time effects. Since the collector-base junction of T4 is reverse-biased, the inverse current gain effect which results in undesirable interactions between multiple emitter inputs is eliminated in this arrangement. If desired, further power reduction may be accomplished by driving the upper node of the resistor R5 from an input line rather than connecting it to the supply line Vs. In this manner the power dissipation in the address decoder may be halved,

assuming a 50% duty cycle on the input line.

This address decoder circuit will provide propagation delays of about 5 nanoseconds at a 4 milliwatts power dissipation, with the circuit layout occupying about 40 square mils in area.

The memory cell comprises 1024 NPN transistors T6 arranged in an orthogonal emitter-follower array fabricated in one isolation well, the thirty-two horizontal conducting address lines being formed by base-diffused stripes 19 in one direction and the thirty-two vertical conducting address lines being formed by metal lines 21 in the other direction, thus requiring single layer metal technology in the integrated circuit fabrication. The emitters 22 are diffused into the base stripes 19 at every intersection of a metal line 21 and the bit pattern is specified by programmable emitter contact openings through which the metal lines 21 are connected via contacts 21' to an associated emitter 22 rather than by programmable metal connections.

A plan view (Figure 3A) and cross sectional views (Figure 3B to 3D) show one corner of a single isolation well including the P-type substrate 23, the epitaxially grown N-type layer 24, the P-type diffusion isolation area 25, the U-type diffusion base stripes 19, the N+ (i.e. heavily N-type semiconductor material) type emitter 22, the silicon dioxide insulation layer 26, the metal layer input lines 27 connecting the address decoder outputs to the base stripes 19, and the metal lines 21. To increase the speed of operation and minimize voltage drop, low resistance N+ diffusion stripes 20 coupled to the input lines 27 extend along each base stripe 19 and are periodically shorted to the base stripe by metal surface contacts 26', serving to reduce the IR (i.e. voltage) drop and the distributed RC time constant along the length of the higher resistance base. By employing a plurality of cross-under N+ diffusion stripes 25' and 25'' to make connection with the metal lines 21 via contacts 25''' extending through the insulation layer 26, the need for two layer metal fabrication techniques is avoided. One group of cross-under diffusion stripes 25' connects with the metal lines 21 on one half the array. The other group of cross-under diffusion stripes 25'' connects with the metal lines on the other half of the array (N-type stripes 25' and 25'' are diffused into P-type regions 25a).

Certain of the metal lines 21 connect with the emitters 22 via connecting portions 21' through openings in the insulation layer 26. The single diffusion area of the common collector 24 for all of the transistors T6 in the array is connected to the supply voltage Vs. Since the entire array of 1024 bits is encompassed in a single collector isolation

area and the programmable emitter contact openings technique is utilized, a high density memory cell array is provided which occupies about one square mil per cell.

- 5 In operation, for a 32×32 memory cell array 15, the row select address decoders 13 hold 31 out of the 32 base stripes 19 at a low voltage; the selected base stripe 19 goes to high voltage and forward-biases the base-emitter memory cells, i.e. unidirectional conducting devices, T6 in that particular selected row. Bit detection is accomplished by sensing the presence or absence of current in the appropriate emitter 22. The column select address decoders 14 hold 31 of the 32 bases of the bit select transistors T7 at a low voltage; the selected base goes to high voltage, turning on the associated bit select transistor T7. The presence or absence of bit current I_C in the associated metal line 21, dependent on whether or not a contact 21' exists between an associated emitter 22 and line 21, is summed with the base current I_B of the transistor T7 to give two distinct current levels of $(I_B + I_C)$ or I_B on the common emitter output line 28. Since 31 of 32 of the bit select transistors T7 are held off and current flows in only one of the 32 columns of the memory cell array, power dissipation is minimized.

- 30 The output driver 17 coupled to the output line 28 of the bit detectors T7 includes a circuit similar to that in the input inverter circuit. The input resistor values are chosen so that the threshold values of the input current I_{in-th} (where the output changes state) is given by

$$I_B < I_{in-th} < (I_B + I_C).$$

- 40 The presence or absence of an emitter contact opening at the address location in the memory cell array will result in a low or high voltage logic level at the output of the output driver 17.

- 45 The input resistor ratios R6:R7 and R8:R9 are chosen to minimize supply current spikes during the turn-on and turn-off. The output transistor configuration results in a low output impedance both in the low and the high output modes so that the effect of output loading on output rise and fall times is minimized. Additional chip section circuitry can force the output to a high impedance condition, so that the ROM outputs can be wired together to expand word capacity above that of the individual ROM package. The resistors in the output driver have the following values (in ohms): R6, 460; R7, 1K; R8, 260; R9, 320; R11, 1K; R12, 4K; R13, 800; R14, 4.2K; and R15, 560.

A variety of circuit ROM's may be fabricated in accordance with the present invention. Simple changes in the metal mask

allows various formats including 4×256 , 2×512 , and 1×1024 to be fabricated in a chip area of about 12,000 square mils. Outputs may be specified to both sink and drive considerable output current, so that both current sinking logic types (TTL, DTL) and current sourcing logic types (RTL, CTL) can be driven from the ROM outputs.

Referring now to Figures 4 and 5, there is shown another form of read only memory made in accordance with the present invention and providing a flexible words $\times$ bits format of 1×1024 , 2×512 , and 4×256 . In this system there are four bit detectors, each including eight transistors T8 having their collectors 33 connected in common to one of the four outputs 34, 35, 36 and 37 of the bit detectors. Each emitter 38 of the eight transistors T8 in a bit detector is connected through a resistor R10' to a separate one of the eight outputs from the X-line decoders. The bases 39 of each transistor T8 are connected in common to a reference voltage V_{REF} .

The outputs from the bit detectors are coupled to separate ones of the four output drivers 41, which also receive an enabling input from the Z-line decoders 42.

In operation, when one of the eight X-decoder transistors T9 is turned on, ground is connected to the lower ends of four resistors R10' associated with that particular transistor T9. Where contacts 21' exist between the emitters 22 of any of the four associated transistors T6 in the high voltage base 19 and the metal lines 21, the base voltage of those transistors T6 is higher than the reference voltage V_{REF} on the bases of the associated transistors T8 and current will flow through T6. No current will flow through the associated transistors T8 to the output lines 34—37.

On the other hand, where there is no contact 21' between the emitters 22 associated with the high voltage base stripe 19 and the metal line 21, current will flow from the supply voltage in the output drivers 41 along the associated output lines 34—37 through T8, R10, and T9. Therefore, the presence or absence of contacts 21' will determine whether or not current flows in the associated one of the output leads 34—37 to the output drivers 41.

WHAT WE CLAIM IS:—

1. A bipolar read only memory comprising a first plurality of address lines, an orthogonally-oriented second plurality of address lines, a first plurality of transistors arranged in a plurality of orthogonally oriented rows and columns, each of said first plurality of transistors having a base, a collector and an emitter, the bases of the transistors in each row of said first plurality of transistors being coupled in common to a different one of said



area and the programmable emitter contact openings technique is utilized, a high density memory cell array is provided which occupies about one square mil per cell.

5 In operation, for a 32×32 memory cell array 15, the row select address decoders 13 hold 31 out of the 32 base stripes 19 at a low voltage; the selected base stripe 19 goes to high voltage and forward-biases the base-emitter memory cells, i.e. unidirectional conducting devices, T6 in that particular selected row. Bit detection is accomplished by sensing the presence or absence of current in the appropriate emitter 22. The column select address decoders 14 hold 31 of the 32 bases of the bit select transistors T7 at a low voltage; the selected base goes to high voltage, turning on the associated bit select transistor T7. The presence or absence of bit current I_C in the associated metal line 21, dependent on whether or not a contact 21' exists between an associated emitter 22 and line 21, is summed with the base current I_B of the transistor T7 to give two distinct current levels of $(I_B + I_C)$ or I_B on the common emitter output line 28. Since 31 of 32 of the bit select transistors T7 are held off and current flows in only one of the 32 columns of the memory cell array, power dissipation is minimized.

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$$I_B < I_{in-th} < (I_B + I_C).$$

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allows various formats including 4×256 , 2×512 , and 1×1024 to be fabricated in a chip area of about 12,000 square mils. Outputs may be specified to both sink and drive considerable output current, so that both current sinking logic types (TTL, DTL) and current sourcing logic types (RTL, CTL) can be driven from the ROM outputs.

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On the other hand, where there is no contact 21' between the emitters 22 associated with the high voltage base stripe 19 and the metal line 21, current will flow from the supply voltage in the output drivers 41 along the associated output lines 34—37 through T8, R10, and T9. Therefore, the presence or absence of contacts 21' will determine whether or not current flows in the associated one of the output leads 34—37 to the output drivers 41.

WHAT WE CLAIM IS:—

1. A bipolar read only memory comprising a first plurality of address lines, an orthogonally-oriented second plurality of address lines, a first plurality of transistors arranged in a plurality of orthogonally oriented rows and columns, each of said first plurality of transistors having a base, a collector and an emitter, the bases of the transistors in each row of said first plurality of transistors being coupled in common to a different one of said



- first plurality of address lines, the collectors of said first plurality of transistors being connected in common to a source of supply voltage, the emitters of selected transistors in each column of said first plurality of transistors being coupled in common to a different one of said second plurality of address lines, first address means coupled to said first plurality of address lines for energizing a selected one of said first plurality of address lines, second address means coupled to said second plurality of address lines for selecting one or more but less than all of said second plurality of address lines, output means including a second plurality of transistors for detecting the presence or absence of current through each of said first plurality of transistors addressed by said selected one of said first plurality of address lines and said selected one or more of said second plurality of address lines, each of said second plurality of transistors being coupled to a different one of said second plurality of address lines.
2. A bipolar read only memory according to claim 1 wherein the bases of the transistors in each row of said first plurality of transistors comprise a common base diffusion stripe and the emitters of the transistors in each row of said first plurality of transistors comprise separate emitter diffusion regions spaced apart along the base diffusion stripe of that row.
3. A bipolar read only memory according to claim 2 wherein said second plurality of address lines comprises a plurality of metal lines, each of said metal lines extending over and being insulated from the emitter diffusion regions of the transistors in a different column of said first plurality of transistors and being connected to selected ones of these emitter diffusion regions by connections extending through openings in the insulation between the metal lines and the emitter diffusion regions.
4. A bipolar read only memory as in claim 1 wherein said first plurality of transistors is formed in an isolation well of a semiconductor chip, said isolation well serves as a common collector for said first plurality of transistors, the bases of the transistors in each row of said first plurality of transistors comprise a separate common base diffusion stripe extending across said isolation well in one direction, the emitters of the transistors in each row of said first plurality of transistors comprise separate emitter diffusion regions spaced apart along the base diffusion stripe of that row, said first plurality of address lines comprises said base diffusion stripes, and said second plurality of address lines comprises spaced-apart metal lines extending across said isolation well orthogonal to said base diffusion stripes, each of said metal lines extending over and being insulated from the emitter diffusion regions of the transistors in a different column of said first plurality of transistors and being connected to selected ones of these emitter diffusion regions by connections extending through openings in the insulation between the metal lines and the emitter diffusion regions at selected points where the metal lines overlie the emitter diffusion regions.
5. A bipolar read only memory according to either one of claims 1 and 4 wherein said first address means comprises a first address decoder circuit having a plurality of outputs, said second address means comprises a second address decoder circuit having a plurality of outputs, and said output means comprises one or more output circuits coupled by said second plurality of transistors to said second plurality of address lines.
6. A bipolar read only memory according to claim 5 wherein each of said second plurality of transistors has a base, a collector, and an emitter, the base of each of said second plurality of transistors being coupled to a different output of said second decoder circuit, the collector of each of said second plurality of transistors being coupled to a different one of said second plurality of address lines, and the emitters of said second plurality of transistors being coupled in common to an output circuit.
7. A bipolar read only memory according to claim 5 wherein said second plurality of transistors is arranged in a plurality of groups and each of said second plurality of transistors has a base, a collector, and an emitter, the bases of said second plurality of transistors being coupled in common to a source of reference voltage, the collectors of the transistors in each group of said second plurality of transistors being coupled in common to a different output circuit, the emitter of each of said second plurality of transistors being coupled to a different one of said second plurality of address lines, and the emitter of each transistor in each group of said second plurality of transistors also being coupled to a different output of said second address decoder circuit.
8. A bipolar read only memory according to any one of claims 1, 4 and 5 wherein said first address means comprises a plurality of AND circuits, each of said AND circuits including a plurality of inputs, an output coupled to one of said first and second plurality of address lines, an input transistor having a base coupled to said output, a collector coupled to a source of supply voltage, and a plurality of separate emitters coupled to said inputs, and an output emitter follower transistor having a collector coupled to a source of supply voltage, a base coupled to the collector of said input transistor, and an emitter coupled to said output.
9. A bipolar read only memory according to any one of claims 1, 4 and 5 including a

- plurality of inverter circuits, each of said inverter circuits including an input, an output coupled to one of said first and second address means, first and second transistors, each of said first and second transistors having a base, a collector, and an emitter, the base of said first transistor being coupled by a first circuit to said input, the collector of said first transistor being coupled in common with the emitter of said second transistor to said output, the emitter of said first transistor being coupled to a source of reference voltage, the collector of said second transistor being coupled to a source of supply voltage, and control means coupled to said input and to the base of said second transistor, said control means being responsive to a change in state of an input signal applied to said input for turning said second transistor off before said first transistor is turned on.
10. A bipolar read only memory according to claim 9 wherein said control means comprises a third transistor having a base, a collector, and an emitter, the base of said third transistor being coupled by a second circuit to said input, the collector of said third transistor being coupled to the base of said second transistor, the emitter of said third transistor being coupled to a source of reference voltage, said second circuit and said third transistor operating to turn said second transistor off before said first circuit operates to turn said first transistor on and operating to turn said second transistor on after said first circuit operates to turn said first transistor off.
11. A bipolar read only memory according to claim 1 substantially as hereinbefore described with reference to the accompanying drawings.
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Printed for Her Majesty's Stationery Office, by the Courier Press, Leamington Spa, 1974.
Published by The Patent Office, 25 Southampton Buildings, London, WC2A 1AY, from which copies may be obtained.



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