Cross-Coupled Transistor Layouts in Restricted Gate Level Layout Architecture

ABSTRACT

A first P channel transistor and a first N channel transistor are defined by first and second gate electrodes, respectively. The second gate electrode is electrically connected to the first gate electrode. A second P channel transistor and a second N channel transistor are defined by third and fourth gate electrodes, respectively. The fourth gate electrode is electrically connected to the third gate electrode. Each of the first P channel transistor, first N channel transistor, second P channel transistor, and second N channel transistor has a respective diffusion terminal electrically connected to a common node. Each of the first, second, third, and fourth gate electrodes is defined to extend along any of a number of parallel oriented gate electrode tracks without physically contacting a gate level feature defined within any gate level feature layout channel associated with a gate electrode track adjacent thereto.

Figure 4