CLAIMS

What is claimed is:

1. A method of forming an integrated circuit, the method comprising:

depositing a first dielectric layer;

depositing a sacrificial masking layer of self-organizing material over the first dielectric layer;

patterning the masking layer, wherein the patterning includes a non-subtractive process that causes the masking layer to self-organize into distinct structures;

patterning the first dielectric layer using the patterned masking layer; and

depositing a metal-insulator-metal (MIM) capacitor over the patterned first dielectric layer.

2. The method of claim 1, wherein the non-subtractive process causes the masking layer to segregate into at least a first phase and a second phase.

3. The method of claim 1, wherein the masking layer comprises at least one of poly(styrene-b-methyl methacrylate), poly(styrene-b-ethylene oxide), poly(styrene-b-lactide), poly(propylene oxide-b-styrene-co-4-vinyl pyridine), poly(styrene-b-4-vinyl pyridine), poly(styrene-b-dimethylsiloxane), poly(styrene-b-methacrylate), poly(methyl methacrylate-b-n-nonyl acrylate), beta-Ti-Cr, polystyrene latex (PSL) spheres, and/or a combination thereof.

4. The method of claim 1, wherein the non-subtractive process includes heating the masking layer to a temperature in the range of about 100–450 °C.

5. The method of claim 1, wherein the non-subtractive process includes exposing the masking layer to a solvent environment including at least one of toluene (C_7H_8), nitrogen (N_2), argon (Ar), and/or helium (He).

6. The method of claim 1, wherein after the non-subtractive process, patterning the masking layer further comprises:

selectively etching away a segregated component material of the masking layer to form a pattern of recesses in the masking layer.

7. The method of claim 6, wherein after the first dielectric layer is patterned using

the patterned masking layer, the method further comprises:

removing the remaining masking layer.

8. The method of claim 1, wherein the masking layer comprises a material which coalesces into isolated islands when heated to a temperature in the range of about 100–450 °C.

9. The method of claim 1, wherein the masking layer comprises at least one of copper (Cu), silver (Ag), silicon (Si), germanium (Ge), platinum (Pt), polystyrene on silicon dioxide (SiO_2), and/or a combination thereof.

10. The method of claim 1, wherein patterning the masking layer does not require any etching.

11. The method of claim 1, wherein the MIM capacitor comprises:

a first conductive layer formed over the first dielectric layer;

a second dielectric layer formed over the first conductive layer; and

a second conductive layer formed over the second dielectric layer.

12. The method of claim 11, wherein at least one of the first conductive layer and/or the second conductive layer comprises at least one of titanium (Ti), titanium nitride (TiN), tantalum (Ta), and/or a combination thereof.

13. The method of claim 11, wherein the second dielectric layer comprises at least one of zirconium dioxide (ZrO_2), tantalum pentoxide (Ta_2O_5), aluminum oxide (Al_2O_3), titanium dioxide (TiO_2), hafnium oxide (HfO_2), lanthanum oxide (La_2O_3), strontium titanate ($SrTiO_3$), and/or a combination thereof.

14. The method of claim 1, wherein before depositing the masking layer over the first dielectric layer, the method further comprises:

depositing a hardmask layer between the first dielectric layer and the masking layer, the hardmask layer comprising at least one of silicon nitride (Si_3N_4), silicon dioxide (SiO_2), silicon oxynitride (SiO_xN_y), a silicon (Si)-rich polymer having a Si concentration greater than or equal to about 20%, titanium nitride (TiN), and/or a combination thereof.

15. The method of claim 1, wherein the patterned first dielectric layer has a substantially corrugated profile and the MIM capacitor is substantially conformal to said profile.

16. The method of claim 1, wherein the patterned first dielectric layer has a substantially corrugated profile including at least one recess having a topography which itself is corrugated.

17. An integrated circuit formed by the method of any of claims 1 through 16.

18. A mobile computing device comprising the integrated circuit of claim 17.

19. A method of forming an integrated circuit, the method comprising:

depositing a first dielectric layer;

depositing a sacrificial layer of block co-polymer material over the first dielectric layer;

treating the layer of block co-polymer material with a non-subtractive process to cause phase separation thereof;

selectively etching the phase-separated layer of block co-polymer material to remove a phase thereof, thereby forming a pattern of recesses therein;

etching to transfer the pattern of recesses into the first dielectric layer;

etching to remove the remaining layer of block co-polymer material; and

depositing a metal-insulator-metal (MIM) capacitor over the patterned first dielectric layer.

20. The method of claim 19, wherein the patterned first dielectric layer has a substantially corrugated profile and the MIM capacitor is substantially conformal to said profile.

21. The method of claim 19, wherein the block co-polymer material comprises at least one of poly(styrene-b-methyl methacrylate), poly(styrene-b-ethylene oxide), poly(styrene-b-lactide), poly(propylene oxide-b-styrene-co-4-vinyl pyridine), poly(styrene-b-4-vinyl pyridine), poly(styrene-b-dimethylsiloxane), poly(styrene-b-methacrylate), poly(methyl methacrylate-b-n-nonyl acrylate), and/or a combination thereof.

22. A method of forming an integrated circuit, the method comprising:

depositing a first dielectric layer;

depositing a sacrificial layer over the first dielectric layer;

treating the sacrificial layer with a non-subtractive process to cause agglomeration thereof, wherein agglomeration of the sacrificial layer results in a pattern of coalesced bodies having recesses there between;

etching to transfer the pattern into the first dielectric layer;

etching to remove the sacrificial layer; and

depositing a metal-insulator-metal (MIM) capacitor over the patterned first dielectric layer.

23. The method of claim 22, wherein agglomeration of the sacrificial layer occurs at a temperature in the range of about 100–450 °C.

24. The method of claim 23, wherein the sacrificial layer comprises at least one of copper (Cu), silver (Ag), silicon (Si), germanium (Ge), platinum (Pt), and/or polystyrene on silicon dioxide (SiO_2).

25. The method of claim 23, wherein the patterned first dielectric layer has a substantially corrugated profile and the MIM capacitor is substantially conformal to said profile.

CLAIMS

What is claimed is:

1. A method of forming an integrated circuit, the method comprising:
depositing a first dielectric layer;

depositing a hardmask layer over the first dielectric layer;

depositing a sacrificial masking layer of self-organizing material over the hardmask layer;

patterning the masking layer, wherein the patterning includes a non-subtractive process that causes the masking layer to self-organize into distinct structures;

patterning the first dielectric layer using the patterned masking layer; and

depositing a metal-insulator-metal (MIM) capacitor over the patterned first dielectric layer.

2. The method of claim 1, wherein the non-subtractive process causes the masking layer to segregate into at least a first component material of a first phase and a second component material of a second phase.

3. The method of claim 1, wherein the masking layer comprises at least one of poly(styrene-b-methyl methacrylate), poly(styrene-b-ethylene oxide), poly(styrene-b-lactide), poly(propylene oxide-b-styrene-co-4-vinyl pyridine), poly(styrene-b-4-vinyl pyridine), poly(styrene-b-dimethylsiloxane), poly(styrene-b-methacrylate), poly(methyl methacrylate-b-n-nonyl acrylate), beta-Ti—Cr, polystyrene latex (PSL) spheres, and a combination thereof.

4. The method of claim 1, wherein the non-subtractive process includes heating the masking layer to a temperature in the range of about 100-450° C.

5. The method of claim 1, wherein the non-subtractive process includes exposing the masking layer to a solvent environment including at least one of toluene (C_7H_8), nitrogen (N_2), argon (Ar), and helium (He).

6. The method of claim 1, wherein after the non-subtractive process, patterning the masking layer further comprises:
selectively etching away a segregated component material of the masking layer to form a pattern of recesses in the masking layer.

7. The method of claim 6, wherein after the first dielectric layer is patterned using the patterned masking layer, the method further comprises:
removing the remaining masking layer.

8. The method of claim 1, wherein the masking layer comprises a material which coalesces into isolated islands when heated to a temperature in the range of about 100-450° C.

9. The method of claim 1, wherein the masking layer comprises at least one of copper (Cu), silver (Ag), silicon (Si), germanium (Ge), platinum (Pt), polystyrene on silicon dioxide (SiO_2), and a combination thereof.

10. The method of claim 1, wherein patterning the masking layer does not require any etching.

11. The method of claim 1, wherein the MIM capacitor comprises:
a first conductive layer formed over the first dielectric layer;

a second dielectric layer formed over the first conductive layer; and

a second conductive layer formed over the second dielectric layer.

12. The method of claim 11, wherein at least one of the first conductive layer and/or the second conductive layer comprises at least one of titanium (Ti), titanium nitride (TiN), tantalum (Ta), and a combination thereof.

13. The method of claim 11, wherein the second dielectric layer comprises at least one of zirconium dioxide (ZrO_2), tantalum pentoxide (Ta_2O_5), aluminum oxide (Al_2O_3), titanium dioxide (TiO_2), hafnium oxide (HfO_2), lanthanum oxide (La_2O_3), strontium titanate ($SrTiO_3$), and a combination thereof.

14. The method of claim 1, wherein after depositing the MIM capacitor over the patterned first dielectric layer, the method further comprises:
depositing a third dielectric layer over the MIM capacitor.

15. The method of claim 14, wherein at least one of the first dielectric layer and the third dielectric layer is a passivation layer.

16. The method of claim 1, wherein the hardmask layer comprises at least one of silicon nitride (Si_3N_4), silicon dioxide (SiO_2), silicon oxynitride (SiO_xN_y), a silicon (Si)-rich polymer having a Si concentration greater than or equal to about 20%, titanium nitride (TiN), and a combination thereof.

17. The method of claim 1, wherein the patterned first dielectric layer has a substantially corrugated profile and the MIM capacitor is substantially conformal to said profile.

18. The method of claim 1, wherein the patterned first dielectric layer has a substantially corrugated profile including at least one recess having a topography which itself is corrugated.

19. An integrated circuit formed by the method of claim 1.

20. A mobile computing device comprising the integrated circuit of claim 19.

21. A method of forming an integrated circuit, the method comprising:
depositing a first dielectric layer;

depositing a sacrificial layer of block co-polymer material over the first dielectric layer;

treating the layer of block co-polymer material with a non-subtractive process to cause phase separation thereof;

selectively etching the phase-separated layer of block co-polymer material to remove a phase thereof, thereby forming a pattern of recesses therein;

etching to transfer the pattern of recesses into the first dielectric layer;

etching to remove the remaining layer of block co-polymer material; and

depositing a metal-insulator-metal (MIM) capacitor over the patterned first dielectric layer.

22. The method of claim 21, wherein the patterned first dielectric layer has a substantially corrugated profile and the MIM capacitor is substantially conformal to said profile.

23. The method of claim 21, wherein the block co-polymer material comprises at least one of poly(styrene-b-methyl methacrylate), poly(styrene-b-ethylene oxide), poly(styrene-b-lactide), poly(propylene oxide-b-styrene-co-4-vinyl pyridine), poly(styrene-b-4-vinyl pyridine), poly(styrene-b-dimethylsiloxane), poly(styrene-b-methacrylate), poly(methyl methacrylate-b-n-nonyl acrylate), and a combination thereof.