# SEMICONDUCTOR DEVICES GROWN IN SPHERICAL CAVITY ARRAYS AND ITS PREPARATION METHOD

## FIELD OF THE INVENTION

The invention relates to the fabrication of semiconductor devices and in particular the fabrication of a plurality of said devices in periodic arrays upon a substrate.

## BACKGROUND

Microcavities have been widely used to fabricate semiconductor lasers, for example, vertical cavity surface emitting lasers (VCSEL), which are key components for information technologies. However, this kind of microcavity confines light in only one dimension, e.g., the vertical dimension. It follows that, it is desirable to confine light in all directions, which should provide higher efficiency for realising low threshold lasers.

A dielectric microsphere, having a diameter comparable to or larger than the wavelength of light, acts as a high-Q (quality factor) optical cavity. The resonant modes are called "whispering gallery modes" (WGMs).

Such microcavity structures can also be used for low-power nonlinear optical switching besides being used in low-threshold lasers.

Another class of nanostructures called "photonic crystals" (PCs), consist of periodically modulated dielectric structures, with high potential to control spontaneous emission and photon transport, and are applicable to more recently developed optical devices. In particular, the formation and characterization of semiconductor two-dimensional (2D) PCs having air/semiconductor interfaces have the advantage of integration to semiconductor optical devices like laser diodes.

Commonly, laser cavities are formed by two facets at two opposite sides of an active medium. However, for compact devices (micro- or nano-scales), these one-dimensional cavities are not efficient enough to provide feedback for lasing.

Alternatively, some dielectric spherical optical cavities have been used in optical devices (resonator) incorporating an active medium (semiconductor materials, semiconductor quantum dots, polymer) to form lasers. But most photonic crystal structures fabricated by growing semiconductor materials have difficulty to make electrically contact.

## SUMMARY OF INVENTION

In a first aspect the invention provides a method for fabricating an array of semiconductor devices comprising the steps of providing a non-metallic substrate;

Placing a layer of spheres on said substrate; reducing diameter of the spheres;

encapsulating the spheres in a matrix of rigid material; finishing an upper surface of said matrix to expose a portion of said spheres; removing the spheres to form an array of cavities within said matrix, and; forming features in said cavities in contact with said substrate so as to form the device.

The present invention uses micro- or nano-spheres as template to obtain micro- or nano-scaled spherical cavities on semiconductor substrates, and then selectively grow nanostructures of semiconductor materials into the spherical cavities. Using this method, light-emitting semiconductors may be epitaxially grown into the spherical cavities. The spherical cavity may provide almost all-directional confinement for light, which efficiently reduces threshold for lasing or enhances light extraction efficiency for light emitting diodes or enhances absorption of light for detectors by making using of photonic crystal effects.

The top surface of the spherical cavity arrays may provide good support for the electrode for making electrical contact with the semiconductor nanostructure arrays when it grows up to the top surface of the spherical cavity arrays.

Preferred embodiments according to the present invention may provide several advantages and unique features. Firstly, the period and size of the spherical cavities may be changed from one hundred nanometers to several micrometers by using different sized sphere template. For different applications, different size or periodicity of the structures may be useful. For example, for active photonic crystal application, the period of the structures may be in the wavelength range

of emitting or receiving light which changes from several hundred nanometers (visible) to several or several ten thousands nanometers (infrared).

The diameter of the spherical cavities may be easily reduced, while keeping the period fixed, by reducing diameters of the spheres after their arrangement. For some applications, for example, photonic crystals, the ratio of diameter of individual structure and periodicity may be a key parameter for controlling optical properties.

Spherical cavities with different materials may be obtained according to their application, for example, spherical metal cavities, which have very high reflectance or spherical polymer cavities.

Chemical vapor deposition (MOCVD for InP, GaAs, GaN based materials), physical vapor deposition (MBE for GaAs, GaN based materials), and emulsion phase epitaxy (for example, low temperature ZnO) may be used to fabricate various kinds nanostructures inside or through the spherical cavities. Those structures may be used in light emitting and receiving devices (detectors, solar cells), which benefited by resonant of spherical cavities or enhancement of photonic crystal structures. The self-alignment of nanowires may also make them suitable for use as field emitting devices.

In a second aspect, the invention provides an array of semiconductor devices fabricated according to a method comprising the steps of providing a non-

metallic substrate; placing a layer of spheres on said substrate; reducing diameter of the spheres; encapsulating the spheres in a matrix of rigid material; finishing an upper surface of said matrix to expose a portion of said spheres; removing the spheres to form an array of cavities within said matrix, and; forming features in said cavities in contact with said substrate so as to form the device.

In a third aspect, the invention provides an array of semiconductor devices comprising a non-metallic substrate, an array of spherical cavities in a matrix of rigid material, said matrix placed on the non-metallic substrate, and features in said cavities in contact with said substrate so as to form the device.

## BRIEF DESCRIPTION OF THE DRAWINGS

It will be convenient to further describe the present invention with respect to the accompanying drawings, which illustrate possible arrangements of the invention. Other arrangements of the invention are possible and consequently the particularity of the accompanying drawings is not to be understood as superseding the generality of the preceding description of the invention.

**Fig. 1 A1** is a top view schematic drawing showing monolayer latex spheres being arranged on a selected substrate, which acts as a template, according to an embodiment of the present invention.

**Fig. 1 A2** is a top view schematic drawing showing the diameter of the spheres of FIG. 1 A1 on the selected substrate being reduced to a predetermined value.

**FIG. 1B** is a cross-sectional view schematic drawing showing formation of a film of selected material, which contains the latex sphere template, according to an embodiment of the present invention.

**FIG. 1C** is a cross-sectional view of a thin layer of the surface of the film of FIG. 1B having been removed so that the top of the latex spheres is exposed.

**FIG. 1D** is a cross-sectional view schematic drawing where the latex spheres of FIG. 1C have been selectively etched off.

**FIG. 1 E1** is a side view schematic drawing of one embodiment of a semiconductor structure grown epitaxially into or through the spherical cavity array of FIG. 1D.

**FIG. 1 E2** is a side view schematic drawing of one embodiment of a semiconductor structure grown epitaxially into or through the spherical cavity array of FIG. 1D.

**FIG. 1 E3** is a side view schematic drawing of one embodiment of a semiconductor structure grown epitaxially into or through the spherical cavity array of FIG. 1D.

**FIG. 2A** is a top view of a SEM image of a $SiO_2$ spherical nanocavity array fabricated according to an embodiment of the present invention.

**FIG. 2B** is a top view of a SEM image of a $SiO_2$ spherical nanocavity array fabricated according to an embodiment of the present invention.

**FIG. 2C** is a tilted view SEM image of the $SiO_2$ spherical nanocavity array fabricated according to an embodiment as shown in Fig. 2B.

**FIG. 3A** is a top view of SEM images of InGaAs/GaAs quantum well nanostructures grown into the $SiO_2$ spherical nanocavity array according to an embodiment of the present invention.

**FIG. 3B** is a top view of a SEM image of InGaAs/GaAs quantum well nanostructure grown into the $SiO_2$ spherical nanocavity array according to an embodiment of the present invention.

**FIG. 3C** is a cross-section view of a SEM image of the InGaAs/GaAs quantum well nanostructures as shown in Fig. 3B.

**FIG. 3D** is a cross-section view of a SEM image of the InGaAs/GaAs quantum well nanostructures as shown in Fig. 3B.

## DETAILED DESCRIPTION

Fig. 1A to 1E outline the process for growing semiconductor nanostructures into 2D ordered spherical silica nanocavities according to an embodiment of the present invention. The process commences with forming a 2D hexagonally close-packed (hcp) colloidal monolayer composed of polystyrene (PS) spheres with diameter of 300 nm by spin coating. GaAs substrates **100** were used in these experiments, which were treated by ozone at 130 $^{0}$C for 5 min. This treatment resulted in a hydrophilic surface of the GaAs substrate, which is useful for arranging the PS spheres. The concentration of the purchased suspension with mean diameter 300 nm was 10% w/w, which was then diluted with deionized (DI) water 1:1 to form a solution.

Mono-layered hcp arrays of the PS spheres **200** were obtained by spin-coating the colloidal suspension at 800 rpm for 60s (Fig. 1 A1). Then, as shown in Fig. 1B, several drops of liquid silica were put onto the whole surface of the wafer having the PS sphere template **200**. The solution quickly infiltrated into the spaces between the PS spheres due to capillary action. The extra materials of the liquid silica were spun off by rotating the wafer at a speed of 5000 rpm for 30 s to form uniform silica film **300**, which contains the PS sphere template **200**. Normally, the thickness of the silica film formed by spin-coating is around 150 nm. However, due to presence of the PS sphere template, the thickness of the silica film formed on the wafer should be approximately the thickness of the film formed on a flat surface plus the diameter of the spheres.

The silica film **300** containing the PS sphere template **200** was further densified by heating in air environment at 250 $^0$C for 15min. Then ICP dry etching using mixed $CF_4$ plus $O_2$ gases was used to etch away a thin layer of the silica film **300** on the top of the PS sphere template **200** to form top openings **310**, which exposes the spheres as shown in Fig 1C. The ICP dry etchings were performed employing these condition: $CF_4$, 20 sccm; $O_2$, 10 sccm; RF power, 100 W; ICP power, 500 W; chamber pressure, 8 mTorr. The PS sphere template **200** was etched off in supersonic bath in toluene solution, then spherical silica nanocavities **400** with circular top openings **310** and bottom openings **320** were formed on the GaAs substrate **100** as shown in Fig. 1D.

The top openings of the silica nanocavities **310** allow reactive gases to diffuse into the nanocavities **400.** Following MOCVD growth, semiconductor nanostructures are deposited on the GaAs surface defined by bottom opening **320** of the silica nanocavities as shown in Fig. 1E.

Shown in Fig. 2A (low magnification) and 2B (high magnification) are typical SEM images of the wafer after the processes shown in Fig. 1A to 1D at the dry etching (Fig. 1C) duration of 5 min. It is clearly seen that honeycomb structures with excellent uniformity are formed. The tilted (45$^0$) top view SEM image as shown in Fig. 2C indicated a relatively smooth top surface of the honeycomb structures. The mean diameter of the openings is about 200nm. The period of

the honeycomb structures is about 315 nm, which is a little larger than that of the PS spheres used as the template (~ 300nm).

Different kinds of semiconductor micro or nanostructures can be grown epitaxially into or through the spherical $SiO_2$ cavities by changing the growth conditions, substrate orientations, growth materials, and growth techniques. For example, vertically aligned pillar structures of GaAs, AlGaAs, InGaAs, or their combinations can be selectively grown into or through the spherical $SiO_2$ nanocavities by MOCVD or MBE on a <111>B GaAs substrate (Fig. 1E2). Nanowires arrays of those materials can be selectively deposited into or through the spherical $SiO_2$ nanocavities by using Au nanoparticle catalysts via vapor-liquid-solid mechanism (as shown in Fig. 1E3).

Pyramidal-like nanostructures (Fig. 1E1) of InGaAs/GaAs quantum structures also can be epitaxially grown into the spherical $SiO_2$ nanocavity arrays by using MOCVD as shown in Fig. 3A to 3D.

A low-pressure horizontal MOCVD system was employed to carry out the growth of InGaAs/GaAs nanostructures into the spherical $SiO_2$ nanocavity arrays. Trimethylgallium (TMGa), trimethylindium (TMIn) were used as group III sources, and TBAs was utilized as the group V sources. The growth temperature of quantum well (s) (QWs) was 600 °C as measured by a thermocouple inserted into the graphite susceptor. The growth chamber pressure was set at 100 mbar. The V/III ratio was 100 and the growth rate was

about 0.1 nm/s. One and two InGaAs QWs with thickness of 5nm separated by a 8nm GaAs barrier layer was grown after 100 nm GaAs buffer layer was grown at 650 $^0$C. Before growth, the wafer with silica spherical cavity arrays was treated at 680 $^0$C for 5 min in $H_2$.

Fig. 3A shows a typical SEM image of the wafer with one InGaAs QW. It is clearly observed that individual nano dot has a flat top surface with six side facets. As deposition of materials was increased, the top surface [<001> facet] disappeared while four large side facets emerged to form pyramidal-like structures as observed in Fig. 3B, which shows the SEM image of the sample with double QWs. In addition, two small side facets posited opposite were also observed. The structural evolution can be explained basically by different facet growth rates of a monocrystalline.

Cross-section view of the structure as shown in Fig. 3B is shown in Fig. 3C and 3D. It is clearly revealed that the nanostructures of InGaAs/GaAs are grown inside the spherical $SiO_2$ nanocavities with good uniformity. The nanostructures with clear facets are also observed. The facets can be identified to be <111> and <110> according their angle relationship. Therefore, the four large facets observed on the top view SEM image as shown in Fig. 3B belong to <110>, while the small two facets opposite each other belong to <111>.

**Claims:**

1. A method for fabricating an array of semiconductor devices comprising the steps of:

providing a non-metallic substrate;

placing a layer of spheres on said substrate;

reducing diameter of the spheres, then;

encapsulating the reduced diameter spheres in a matrix of rigid material;

finishing an upper surface of said matrix to expose a portion of said spheres;

removing the spheres to form an array of cavities within said matrix, and;

forming features in said cavities in contact with said substrate so as to form the device.

2. The method according to claim 1, wherein the encapsulating step comprises the step of electroplating a metal about the spheres to form the matrix.

3. The method according to claim 1, wherein the encapsulating step comprises the steps of introducing a liquid material to immerse the spheres, then solidifying said liquid to form the matrix.

4. The method according to claim 1, wherein the encapsulating step comprises the step of depositing material around the spheres by CVD to form the matrix.

5. The method according to claim 3, wherein said liquid is $SiO_2$.

6. The method according to claim 1, wherein the finishing step comprises etching the upper surface of the matrix.

7. The method according to claim 1, wherein the finishing step comprises polishing the upper surface of the matrix using a CMP process.

8. The method according to claim 1, further comprising the step of etching a bottom surface of the cavities to further expose the substrate.

9. The method according to claim 1, wherein the step of forming features in the cavities includes depositing semiconductor materials using a CVD, or MOCVD, or MBE process.

10. The method according to claim 1, wherein the step of forming features in the cavities includes depositing materials using spin-off process.

11. The method according to claim 1, wherein the reduction of the diameter of the spheres is in the range of 0% to 50% of the diameter.

12. The method according to claim 1, wherein the spheres are of a material having different etching properties to those of the material of the matrix.

13. The method according to claim 1, wherein the spheres are of a material having different etching properties to those of the material of the substrate.