

PATENT SPECIFICATION

DRAWINGS ATTACHED

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COMPLETE SPECIFICATION

Signal Translating System

We, RADIO CORPORATION OF AMERICA, a Corporation organized under the laws of the State of Delaware, United States of America, of 30, Rockefeller Plaza, City and State of New York, United States of America, do hereby declare the invention, for which we pray that a patent may be granted to us, and the method by which it is to be performed, to be particularly described in and by the following statement:—

This invention relates to signal translating systems, and more particularly to signal translating systems which can be economically fabricated using integrated circuit techniques.

As used herein, the term integrated circuit refers to a unitary or monolithic semiconductor device which is the equivalent of a network of interconnected active and passive circuit elements. Various problems have presented themselves in the design of amplifier circuits to be formed in an integrated circuit device. For example, in cascade connected resistance-capacitance amplifiers, the use of coupling capacitors between successive stages may be objectionable in some applications.

For one thing, the coupling capacitor occupies considerable area on the integrated circuit device, even for a relatively small amount of capacitance. The small coupling capacitance limits not only the low frequency response of the amplifier, but also the high frequency response, and therefore the gain at the desired signal frequency. The parasitic shunt capacitance which occurs in integrated circuit capacitor structures may limit the high frequency response of the circuit. In addition to the foregoing, limitations in the processing techniques presently used for forming capacitors are such that the resultant capacitors may be a source of trouble due to shorting between the plates thereof.

In cascade connected direct coupled ampli-

fiers, the direct voltage appearing at the output electrode of one stage comprises the voltage which is applied to the succeeding stage. As a result, complicated biasing networks are used to establish the desired operating point for each of the cascaded stages. In addition, direct current (d-c) feedback must be provided for operating point stabilization. Where substantial gain is to be provided in a single integrated circuit device, the phase shifts within the feedback loop are such as to increase the likelihood of circuit instability.

In accordance with the invention a signal translation stage comprises first and second transistors connected in an emitter-coupled amplifier circuit, a first resistor being connected in a common circuit for the emitter electrodes of said transistors, and a second resistor having substantially twice the resistance value of said first resistor being connected in the collector electrode circuit of said second transistor, a third transistor connected in an emitter-follower configuration to the voltage sources used to supply said emitter-coupled amplifier circuit and a direct current connection between the collector electrode circuit of said second transistor and the base electrode of said third transistor.

The terms resistors, capacitors, transistors, rectifiers, etc., as used herein are intended to apply to the equivalent device as incorporated in or on an integrated circuit device.

In the accompanying drawings:—

FIGURE 1 is a schematic circuit diagram of an amplifier stage embodying the invention;

FIGURE 2 is a schematic circuit diagram of a pair of amplifiers stages connected in cascade;

FIGURES 3a, 3b and 3c are graphs showing the frequency response of the amplifier cir-

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cuit of FIGURE 2 for different conditions in the feedback circuit thereof;

FIGURES 4a and 4b represent circuit elements which may be connected in the feedback circuit of the amplifier shown in FIGURE 2;

FIGURE 5 is a schematic circuit diagram of an angle modulated wave processing channel for television receivers which may be incorporated in an integrated circuit device, and

FIGURE 6 illustrates a modification which may be made to the arrangement described in relation to FIGURE 5.

The schematic circuit diagram of FIGURE 1 shows a direct coupled amplifier stage 10 which may comprise a basic building block for integrated circuits. The amplifier stage 10 includes three transistors 12, 14 and 16 connected to provide an emitter coupled amplifier circuit driving an emitter follower circuit.

The emitter coupled amplifier circuit includes the transistor 12 connected in the common collector configuration, driving the transistor 14 which is connected in the common base configuration. Signals from a source 18, not necessarily included in the integrated circuit device, are applied to the base electrode of the transistor 12.

Coupling between the transistors 12 and 14 is provided by direct-emitter connection and the resistor 20 which is connected in common between the emitter electrodes of the transistors 12 and 14 and the negative terminal 22 of an operating potential supply. The base electrode of transistor 14 is connected to the ground.

A load resistor 24 is connected between the collector electrode of the transistor 14 and a positive terminal 26 of the operating potential supply. Amplified signals developed across the load resistor 24 are directly applied to the base electrode of the transistor 16 which is connected in an emitter follower circuit. Output signals from the stage 10 are developed across the emitter follower load resistor 28.

The operating potential supply source, not shown, comprises a three terminal supply providing symmetrical positive and negative voltages relative to ground. By way of example, the voltages at the terminals 26 and 22 may be plus two volts and minus two volts respectively, with ground as a reference.

In the present example the emitter coupled amplifier circuit is balanced for symmetrical operation by maintaining the base electrodes of the transistors 12 and 14 at substantially the same (ground) potential. Further amplifier stages of the same circuit configuration as the amplifier stage 10 can be directly driven by the amplifier stage 10 if the d-c voltage at the emitter electrode of the transistor 16 is held at ground potential. In such a case the emitter coupled amplifier or limiter of succeeding stages will be balanced since the base

electrodes of the first transistor 12 will be at ground potential. It should be noted at this point that for some circuit applications a deliberate unbalance of succeeding emitter coupled amplifiers may be desirable.

The desired d-c output voltage level is established by setting the quiescent voltage at the collector of the transistor 14 at a voltage exceeding the desired d-c output voltage by an amount equal to the voltage drop (V_{be}) across the base-to-emitter junction of the transistor 16. To provide zero output voltage relative to ground, the voltage at the collector electrode of the transistor 14 is set to about +.65 volts, and the opposing plus-to-minus .65 volts across the base-to-emitter junction of the transistor 16 results in zero volts at the emitter electrode of the transistor 16. Thus succeeding stages may be directly connected in cascade without the necessity for complicated biasing networks.

The circuit can be stabilized against temperature changes and power supply variations by selecting the resistor 24 to be twice as large as the resistor 20. Temperature changes tend to change the voltage V_{be} between the emitter and base of the three transistors. In the transistors 12 and 14, assume that temperature changes cause a change in V_{be} by an amount ΔV_{be} , and that as a result the current of each transistor 12 and 14 changes by an amount Δi .

Then

$$\Delta V_{be} = 2\Delta i R_{20} \quad (1)$$

rearranging

$$\Delta i = \frac{\Delta V_{be}}{2R_{20}} \quad (2) \quad 100$$

in which R_{20} is the resistance of resistor 20. The change in the collector voltage of the transistor 14 is:

$$\Delta V_o = \Delta i R_{24} \quad (3)$$

in which R_{24} is the resistance of resistor 24. Substituting (2) in (3)

$$\Delta V_o = \frac{\Delta V_{be} R_{24}}{2R_{20}} \quad (4)$$

The change in voltage at the emitter electrode of the transistor 16 is $\Delta V_o - \Delta V_{be}$ or

$$\frac{\Delta V_{be} R_{24}}{2R_{20}} - \Delta V_{be} = \Delta V_{be} \left(\frac{R_{24}}{2R_{20}} - 1 \right) \quad 110$$

If $R_{24} = 2R_{20}$, then the net change in voltage at the emitter electrode of the transistor 16 is zero. In other words, if the resistor 24 is made twice as large as the resistor 20, the rise in voltage at the emitter follower output due to its decreasing V_{be} with increasing temperature is compensated by the fall in



voltage at the collector of the transistor 14.

Next, consider the effects of operating potential supply variations. If the voltage at the terminal 26 drops by a voltage Δe_1 (becomes less positive) then the output voltage at the collector of transistor 14 falls a like amount because the current through transistor 14 remains constant. If the voltage at the terminal 22 drops by a voltage Δe_2 (becomes less negative) the emitter current per transistor falls by $\frac{\Delta e_2}{2R_{20}}$, and the collector voltage rises

by $\frac{\Delta e_1 R_{24}}{2R_{20}}$. Thus the net change in voltage at collector of the transistor 14 is $\Delta e_1 - \frac{\Delta e_2 R_{24}}{2R_{20}}$.

Again, if the resistor 24 is made twice the value of the resistor 20, then the net change in voltage at the collector of the transistor 20 is $\Delta e_1 - \Delta e_2$. It is advantageous to derive e_1 and e_2 from a common power source so that e_1 and e_2 will change in the same proportion.

An important fact to be noted here is that the ratios of the resistors 20 and 24 are more important to the maintenance of stability than their absolute values. This is of special significance in integrated circuit fabrication since the two resistors can be formed at the same time and their ratios can be readily maintained whereas the absolute resistance values are a function of the variables in the fabrication processes. Accordingly with a given process procedure, a higher yield of useable circuits can be expected where the ratios of the circuit components are more significant than the absolute values.

The schematic circuit diagram of FIGURE 2 includes a pair of amplifying stages 30 and 32 directly connected in cascade. The stage 32 is the same as that shown in FIGURE 1 and the stage 30 differs from the circuit shown in FIGURE 1 in that a direct current feedback loop has been included to provide operating point stabilization.

The amplifier stage 30 includes a pair of transistors 34 and 36 connected to operate as an emitter coupled amplifier, and a third transistor 38 connected to operate as an emitter follower amplifier. The output signals from the amplifier stage 30 are developed across a load resistor 40. The d-c feedback circuit includes a resistor 42 connected between the emitter electrode of the transistor 38 and the base electrode of the transistor 36. A capacitor 44 connects the base electrode of the transistor 36 to ground.

Base current of the transistor 36 flowing through the resistor 42 tends to establish the base electrode of the transistor 39 at a positive voltage relative to ground. Such a voltage tends to unbalance the emitter

coupled amplifier portion of the stage 32 because the direct voltage at the base electrodes of the transistor 39 and 41 would be different.

To prevent unbalance and preserve symmetrical limiting in the circuit, an offset voltage is developed in the feedback loop. The offset voltage is developed across a resistor 46 connected between the emitter of the transistor 38 and the load resistor 40. The resistor 46 is of a value to develop a voltage equal to the voltage developed across the resistor 42. Since the voltages across the resistors 42 and 46 are in opposition, the base electrode of the transistor 36 is operated at ground potential. At the same time, the d-c output voltage at the junction of the resistor 40 and 46 is at ground potential. Complete balance is thereby obtained.

The capacitor 44 provides maximum feedback voltages at d-c or low frequencies. The frequency response of the amplifier stage of FIGURE 2 is shown in FIGURE 3(a) which is a plot of amplitude A of the output signal against frequency. The drop in gain at low frequencies is due to the low frequency negative feedback, and the drop in gain at high frequencies is due to shunt capacities in the integrated circuit.

Other forms of feedback can be used. For example, if the capacitor 44 is replaced by a resistor as shown in FIGURE 4a, the frequency response becomes relatively flat from d-c to some higher frequency determined by the resistance "level" as shown in FIGURE 3(b). The upper frequency limit has been found to be as high as 100 megacycles per second when collector resistors for the transistors 36 and 41 are of low values such as of the order of 150 ohms. If a selective network, such as the series tuned circuit shown in FIGURE 4b, is used to replace the capacitor 44 the response assumes a band-pass characteristic as shown in FIGURE 3(c). Thus, it can be seen that the shape of the frequency passband characteristic is established by the type of feedback circuit used.

In the circuit of FIGURE 2, the amplifier stage 30 is operated at low power levels and the amplifier stage 32 is operated at higher power levels. To this end, the symmetrical positive and negative voltages applied to the terminals 54 and 56 are smaller in magnitude than the positive and negative voltages applied to the terminals 50 and 52. The high level stage 32 need not be included in the feedback loop since it is automatically balanced by the feedback which precedes it.

The fact that the amplifier stage 32 is not included in the feedback loop reduces the amount of open loop gain enclosed by the feedback loop, and thereby reduces the possibility of oscillation. It should be noted that neither the voltage nor resistance ratios need be maintained in the high level stage 32. The

resistors



emitter follower portion 32 is not substantially affected by unbalance of the emitter coupled portion of the stage, and the emitter of the emitter follower need not be maintained at ground potential.

The schematic circuit diagram of FIGURE 5 shows the use of multiple three transistor amplifier stages in the sound channel of a television receiver. The dotted line rectangle 60 has a pair of contact areas 62 and 64 which are coupled to a source of FM (frequency modulated) waves. As to physical dimensions, the chip 60 may be of the order of 50 mils $\times$ 50 mils, or smaller.

FM signals from a suitable source such as a video detector of a video amplifier of a television receiver are applied to a terminal 66 and coupled through a capacitor 68 to a resonant circuit 70 which is tuned to the 4.5 Mc/s intercarrier beat between the video and sound carriers of a television signal. The resonant circuit 70 and the coupling capacitor 68 in the present example are external to the chip but are coupled thereto through the contact areas 62 and 64. It is noted that the principles of the invention are readily adapted to broadcast FM receivers.

The contact area 62 is directly coupled to a first amplifier stage 72 including three transistors 74, 76 and 78. The first two transistors 74 and 76 are connected to provide an emitter coupled amplifier and the third transistor 78 is connected as an emitter follower as described above.

The amplifier stage 72 is directly coupled to a similar amplifier stage 80 which also includes three transistors 82, 84 and 86. A feedback circuit including a resistor 88 is connected between the emitter electrode of the transistor 86 and the base electrode of the transistor 76. A capacitor 90, which may not be on the integrated circuit chip, connects the base electrode of the transistor 76 to a common circuit for the base electrodes of the transistors 74 and 84.

The capacitor 90 is connected to the integrated circuit chip through a contact area 92. An offset voltage is developed in the feedback circuit across a resistor 94 to oppose and cancel the voltage developed across the feedback resistor 88 as described in connection with FIGURE 2.

Output signals from the stage 80 are developed across a resistor 96 and applied to a high level amplifier stage 100 including three transistors 102, 104 and 106. The emitter follower transistor 106 portion of the stage 100 is connected through a contact area 108 to drive the primary winding of the discriminator transformer 110. The secondary winding of the discriminator transformer is connected through a pair of contact areas 112 and 114 to the remainder of the discriminator circuit 116. The discriminator circuit 116 is balanced to provide a direct output voltage at

the base of the transistor 118 which does not vary with signal level or power supply fluctuations. The demodulated signals applied to the base electrode of the transistor 118 are developed across the resistor 120, and are taken from the semiconductor chip through the contact area 124.

The circuit of FIGURE 5 differs from that of FIGURES 1 and 2 in that the operating potential supply is unbalanced. In other words all of the voltages in the circuit are positive relative to ground. To this end the positive terminal of a d-c supply source which may be subject to some variation is connected to the contact area 130, and grounded negative terminal is connected to the contact area 132. The unregulated voltage between the contact areas 130 and 132 is directly applied to the transistors of the high level amplifier stage 100.

A resistor 138 and six rectifiers 140, 142, 144, 146, 148 and 150, all formed on the integrated circuit chip, are connected in series between the power supply terminals 130 and 132, and provide regulated operating voltages for the amplifier stages 72 and 80. The rectifiers 140-150 are poled to be forward biased by the supply connected across the terminals 130 and 132, and provide a substantially constant voltage drop for relatively wide fluctuations of the supply voltage. The full voltage across the six rectifiers provides the collector voltage supply for the transistors used in the amplifier stages 72 and 80, except for the emitter follower transistor 86. The voltage developed across the rectifiers 140, 142 and 144 is used to provide the base voltage for the transistors 74, 84 and 104.

The voltage regulating system described is not only advantageous in that it is readily incorporated in an integrated circuit chip, but it also provides readily available regulated voltages between the various rectifiers. For example, the base electrode of the transistor 118 is connected through the discriminator transformer to the junction between the rectifiers 144 and 146 and is thus held at about plus two volts above ground. The appropriate biasing potential for the transistor 118 is then provided by returning the emitter electrode through the resistor 122 to a point between the rectifiers 140 and 142. Since the voltage drop per rectifiers is about 0.65 volts, about 1.3 volts is applied between the base and emitter electrodes of the transistor 118, a portion of which is dropped across the resistor 122.

As in the case of the circuit of FIGURE 2, the output amplifier stage 100 is not included within the feedback loop. However, the feedback loop maintains the voltage across the resistor 96 at the same level as the voltage applied to the base of the transistor 104, hence the emitter coupled amplifier portion of the amplifier stage 100 is automatically

balanced. It may be desirable in some applications to hold the voltage across the resistor 96 at a value different from that applied to the base electrode of the transistor 104. By way of example, such an unbalance in the base bias voltages permits a greater collector voltage swing for the transistor 104, and hence a larger amplitude output signal.

The circuit configuration is such that transient or steady state overloads applied to the base electrode of the transistor 74 does not introduce surges in the feedback network or in the output circuit of the amplifier. This is a result of the higher degree of symmetrical limiting obtained in the emitter coupled amplifier and the linearity of the emitter follower. This insensitivity to overload conditions prevents undesirable shifts in the operating point of the amplifier with signal level which would cause a shift in the clipping axis and thereby degrade the limiting performance of the circuit.

The fundamental configuration of each amplifier stage is such that the input circuit has a high input impedance and is free of feedback through the collector-to-base capacitance of the first transistor of each stage. The freedom from Miller-effect feedback also increases the gain and bandwidth of the amplifier, reduces phase shifts of the signal and improves the overall stability. The circuit of FIGURE 5 provides outstanding performance as an amplifier-limiter. A dynamic range of over 70 db has been obtained because the absence of rectification and other non-linear effects in each of the amplifier stages prevents the operating point from shifting even under extreme overload conditions.

The absence of coupling capacitors between the various amplifier stages provides advantages both to the topology of the resultant integrated circuit, and in the integrated circuit performance. As mentioned above, coupling capacitors take up a large area on the integrated circuit. In addition, the coupling capacitors add parasitic capacitance which reduces the bandwidth of the circuit.

In high gain amplifier and limiter circuits which are required to handle large signals with a large percentage of amplitude modulation, greater regulation of the power supply voltage is required. The internal resistance of the rectifiers 140-150 of FIGURE 5 is sufficiently high so that changes in the load current drawn by the transistors of the amplifier stages 72 and 80 may produce changes in the voltages applied to these transistors. The two emitter coupled portions (transistors 74 and 76 and transistors 82 and 84) are essentially constant current, and amplitude modulation does not materially affect the current drawn by these stages. However, the emitter follower transistors 78 and 86 draw current as a function of the amplitude modulation. These current changes operating

against the internal resistance of these rectifiers may adversely affect the operation of the system. Accordingly, as shown in FIGURE 5, the transistor 86 collector, which operates at higher signal level than the transistor 78, is not supplied by the rectifier divider 140-150, but is returned to the operating potential terminal 130.

A lower impedance voltage supply may be provided on the integrated circuit chip as shown in FIGURE 6. A pair of transistors 160 and 162, connected as emitter followers provide the desired impedance transformation. An additional rectifier 143 is provided to offset the emitter-to-base drop of the transistors 160 and 162. Operating potential for the collector electrodes of transistors 74, 76, 78, 82, 84 and 86 is provided at the emitter electrode terminal 164 of the transistor 160. The intermediate potential derived between the rectifiers 144 and 146 of FIGURE 6 is available at the emitter electrode terminal 166 of transistor 162. The terminal 168 of FIGURE 6 is adapted to be connected to the transistor 118 through the resistor 122.

The emitter followers present a lower impedance than the rectifiers 140-150, and hence variations in load current due to amplitude modulation produce a much smaller change in supply voltage. As a result, with the circuit of FIGURE 6, the collector electrode of the transistor 86 may be returned to the regulated supply terminal 164, with appropriate adjustment of the emitter load resistor value of that transistor.

The integrated circuit including the biasing chain of rectifiers is described and claimed in Specification 25028/68 (Serial No. 1,127,802) divided from this Application.

WHAT WE CLAIM IS:—

1. A signal translating stage comprising first and second transistors connected in an emitter-coupled amplifier circuit, a first resistor being connected in a common circuit for the emitter electrodes of said transistors, and a second resistor having substantially twice the resistance value of said first resistor being connected in the collector electrode circuit of said second transistor, a third transistor connected in an emitter-follower configuration to the voltage sources used to supply said emitter-coupled amplifier circuit, and a direct current connection between the collector electrode circuit of said second transistor and the base electrode of said third transistor.

2. A circuit arrangement comprising a signal translating stage in accordance with claim 1 connected in cascade with one or more like stages and including a direct-current feedback connection from the emitter-follower of a succeeding stage to the emitter-coupled amplifier of a preceding stage.

3. A circuit arrangement in accordance

balanced.⁴ It may be desirable in some applications to hold the voltage across the resistor 96 at a value different from that applied to the base electrode of the transistor 104. By way of example, such an unbalance in the base bias voltages permits a greater collector voltage swing for the transistor 104, and hence a larger amplitude output signal.

The circuit configuration is such that transient or steady state overloads applied to the base electrode of the transistor 74 does not introduce surges in the feedback network or in the output circuit of the amplifier. This is a result of the higher degree of symmetrical limiting obtained in the emitter coupled amplifier and the linearity of the emitter follower. This insensitivity to overload conditions prevents undesirable shifts in the operating point of the amplifier with signal level which would cause a shift in the clipping axis and thereby degrade the limiting performance of the circuit.

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against the internal resistance of these rectifiers may adversely affect the operation of the system. Accordingly, as shown in FIGURE 5, the transistor 86 collector, which operates at higher signal level than the transistor 78, is not supplied by the rectifier divider 140-150, but is returned to the operating potential terminal 130.

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WHAT WE CLAIM IS:—

1. A signal translating stage comprising first and second transistors connected in an emitter-coupled amplifier circuit, a first resistor being connected in a common circuit for the emitter electrodes of said transistors, and a second resistor having substantially twice the resistance value of said first resistor being connected in the collector electrode circuit of said second transistor, a third transistor connected in an emitter-follower configuration to the voltage sources used to supply said emitter-coupled amplifier circuit, and a direct current connection between the collector electrode circuit of said second transistor and the base electrode of said third transistor.

2. A circuit arrangement comprising a signal translating stage in accordance with claim 1 connected in cascade with one or more like stages and including a direct-current feedback connection from the emitter-follower of a succeeding stage to the emitter-coupled amplifier of a preceding stage.

3. A circuit arrangement in accordance

with claim 2 wherein said feedback connection includes a third resistor.

5 4. A circuit arrangement in accordance with claim 3 including means for developing in said feedback path an offset voltage substantially equal in magnitude but opposite in polarity to the voltage developed across said third resistor.

10 5. A circuit arrangement in accordance with claim 4 wherein the means for developing said offset voltage includes a fourth resistor which is connected to the emitter of the emitter-follower transistor.

15 6. A circuit arrangement in accordance with claim 5 comprising first and second terminals adapted to be connected to an operating potential supply source, and a third terminal adapted to be connected to a potential source intermediate the potentials to be maintained at said first and second terminals, said first resistor in each said stage being connected between the emitter electrodes of said first and second transistors and said first terminal, said second resistor in each said stage being connected between the collector of said second transistor and said second terminal, and the collectors of said first and third transistors in each said stage being directly connected to said second terminal, said fourth and a fifth resistor being connected in series between the emitter of said third transistor in said succeeding stage and said

first terminal, said third resistor being connected between the emitter of said third transistor and the base electrode of the second transistor in said preceding stage, said fourth resistor having a value such that the voltage developed thereacross is equal to that developed across said third resistor, an impedance connected between said second transistor base electrode and said third terminal and a signal output circuit connected to the junction of said fourth and fifth resistors.

7. A circuit arrangement in accordance with claim 6 wherein said impedance comprises a capacitor, a resistor or a series-resonant circuit.

8. A circuit arrangement in accordance with any one of the preceding claims wherein all said transistors and said resistors constitute elements of one and the same integrated circuit device.

9. A signal translating stage substantially as described with reference to Figures 1, 2 or 2 and 4 of the drawings.

10. A signal translating circuit arrangement substantially as described with reference to Figure 5 or Figures 5 and 6 of the drawings.

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