CLAIMS

1. A chip module including:

an integrated-circuit (IC) chip,

a first substrate layer made at least partly of a flexible material and with a first hole,

a second substrate layer made at least partly of an adhesive material and with a second hole,

a third substrate layer made at least partly of an electrically conductive material,

a fourth substrate layer made at least partly of an adhesive material and with a third hole, and

a fifth substrate layer with a fourth hole,

wherein said second substrate layer is sandwiched between and fixedly engaged with said first substrate layer and said third substrate layer,

wherein said first hole of said first substrate layer and said second hole of said second substrate layer are aligned with each other to form a first cavity,

wherein at least a first part of said IC chip is received within said first cavity, and

wherein said chip module is in the shape of a prism, a cylinder, or an elliptical cylinder.

2. The chip module of Claim 1, wherein said third substrate layer is made at least partly of copper.

3. The chip module of Claim 1 or 2, wherein said third substrate layer includes at least one slit engaged with a leg of said IC chip to electrically connect said IC chip with said third substrate layer.

4. The chip module of any of the preceding claims, wherein said first hole and said second hole are of the substantially the same size and shape.

5. The chip module of any of the preceding claims, wherein said first substrate layer is made of polyimide (PI), polyethylene terephthalate (PET), and/or a glass-reinforced epoxy laminate material.

6. The chip module of Claim 1, wherein said third hole and said fourth hole are aligned with each other to form a second cavity, and wherein at least a second part of said IC chip is received within said second cavity.

7. The chip module of Claim 6, wherein said third hole and said fourth hole are of the substantially the same size and shape.

8. The chip module of any one of the preceding claims, wherein said fifth substrate layer is made of or electro-plated with an electrically conductive material.

9. The chip module of any one of the preceding claims, wherein two opposite major surfaces of said chip module are planar, of the same shape and parallel to each other.

10. A chip module card inlay including at least one chip module according to any one of Claims 1 to 9.

11. The chip module card inlay of Claim 10, wherein said chip module is received within a fifth hole of a sixth substrate layer.

12. The chip module card inlay of Claim 11, wherein said sixth substrate layer is sandwiched between and fixedly engaged with a seventh substrate layer and an eighth substrate layer.

13. The chip module card inlay of any one of Claims 10 to 12, wherein said chip module is electrically connected with at least one conductive wire.

14. A method of forming a chip module including:

providing a first substrate layer made at least partly of a flexible material and with a plurality of first holes,

providing a second substrate layer made at least partly of an adhesive material and with a plurality of second holes,

providing a third substrate layer made at least partly of an electrically conductive material,

aligning said first holes of said first substrate layer with said second holes of said second substrate layer to form a plurality of first cavities,

sandwiching said second substrate layer between said first substrate layer and said third substrate layer,

fixedly engaging said first substrate layer, said second substrate layer and said third substrate layer to form a first layered structure,

fixedly engaging at least a first part of an integrated-circuit (IC) chip within one of said first cavities of said first layered structure,

providing a fourth substrate layer made at least partly of an adhesive material and with a plurality of third holes and a fifth substrate layer with a plurality of fourth holes,

fixedly engaging said fourth adhesive substrate layer and said fifth substrate layer with said first layered structure to form a second layered structure,

cutting out at least one chip module from said second layered structure fixedly engaged with said IC chip, and

wherein said chip module is in the shape of a prism, a cylinder, or an elliptical cylinder.

15. The method of Claim 14, wherein said third substrate layer is made at least partly of copper.

16. The method of Claim 14 or 15, including engaging a leg of said IC chip with at least one slit of said third substrate layer to electrically connect said IC chip with said third substrate layer.

17. The method of any one of Claims 14 to 16, wherein said first holes and said second holes are of the substantially the same size and shape.

18. The method of any one of Claims 14 to 17, further including filling at least a part of a space between said first part of said IC chip and said first cavity with an adhesive.

19. The method of any one of Claims 14 to 18, wherein said first substrate layer is made of polyimide (PI), polyethylene terephthalate (PET), and/or a glass-reinforced epoxy laminate material.

20. The method of Claim 19, further including aligning said third holes of said fourth adhesive substrate layer with said fourth holes of said fifth substrate layer to form a

plurality of second cavities, and positioning at least a second part of said IC chip within one of said second cavities.

21. The method of Claim 20, wherein said third holes and said fourth holes are of the substantially the same size and shape.

22. The method of any one of Claims 19 to 21, wherein said fifth substrate layer is made of or electro-plated with an electrically conductive material.

23. The method of any one of Claims 14 to 22, wherein two opposite major surfaces of said chip module are planar, of the same shape and parallel to each other.

24. A method of forming a chip module card inlay including forming at least one chip module according to a method according to any one of Claims 14 to 23.

25. The method of Claim 24, including positioning said chip module within a fifth hole of a sixth substrate layer.

26. The method of Claim 25, including sandwiching said sixth substrate layer between a seventh substrate layer and an eighth substrate layer, and fixedly engaging said sixth substrate layer, said seventh substrate layer and said eighth substrate layer with one another.

27. The method of any one of Claims 24 to 26, including electrically connecting said chip module with at least one conductive wire.