

S P E C I F I C A T I O N

TITLE OF THE INVENTION

5 Semiconductor Device and Process for
 Manufacturing the Same

BACKGROUND OF THE INVENTION

 The present invention relates to a semiconductor
10 device and a process for manufacturing it and, more
 particularly, to a technique which is effective if
 applied for switching the functions and word
 structures of a memory module including a plurality of
 semiconductor devices.

15 According to our investigations, the memory
 module to be used as an extended memory in a personal
 computer or a work station is constructed by mounting
 on a module wiring substrate a memory or the DRAM
 (dynamic random access memory) semiconductor device,
20 as made of the SOJ (small outline package) type resin-
 sealed package, for example.

 In order that the memory module may have
 specifications conforming to the device to be used,
 there is mounted on the aforementioned module wiring
25 substrate the memory in which the functions are

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switched in the refresh cycle such as a refreshing operation cycle or a reading mode such as FAST PAGE or EDO (extended data out).

5 The switching of these functions of the memory is executed by connecting a predetermined electrode in a semiconductor chip through a bonding wire with a supply voltage V_{CC} or a ground potential V_{SS} or no connection terminal (NC) in the bonding step for packaging.

10 As another method for switching the aforementioned memory functions, moreover, there is known either the memory for selecting a predetermined reading mode in dependence upon a predetermined signal fed from the outside of the memory, as disclosed in
15 Japanese Patent Laid-Open No. 75494/1984, or the memory for designating a bit length mode programmably on the basis of a predetermined signal, as disclosed in Japanese Patent Laid-Open No. 59682/1986. On the other hand, the memory module is disclosed in Japanese
20 Patent Laid-Open No. 334112/1994.

Incidentally, the memory extended system of this kind is disclosed in detail, for example, on pp. 114 to 126 of "Semiconductor MOS Memory and Its Use", as issued on August 30, 1990 by Nikkan Kogyo Shinbunsha
25 and edited by Yasoji Suzuki. This publication

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describes the circuit construction and operations of a memory extending DRAM board.

SUMMARY OF THE INVENTION

5 Incidentally, it has been found by us that the aforementioned memory module has the following problem.

 The memory, as used in a memory module to be used as the extended memory of a personal computer or the
10 like, has a variety of function switching operations. However, the memory module, as mounted as a complete product on the module wiring substrate, cannot switch the functions. Thus, the memory modules are assembled for the individual functions, and there arises a
15 problem that the degree of freedom for the production is degraded.

 An object of the present invention is to provide a memory module, in which the individual functions and word structures can be arbitrarily switched outside of
20 the package, and a process for manufacturing the memory module.

 The aforementioned and other objects and novel features of the present invention will become apparent from the following description to be made with
25 reference to the accompanying drawings.

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The summaries of the representatives of the invention to be disclosed herein will be briefly described in the following.

A memory module according to the present invention comprises at least one semiconductor device including function switching external terminals for selecting a function in dependence upon the state of a function switching signal; and a printed-wiring substrate with the semiconductor device mounted thereon and including function switching means for selecting an arbitrary function switching signal to be inputted to the function switching external terminals.

According to the present invention, moreover, the function switching means includes a first node formed on the printed-wiring substrate and electrically connected with the function switching external terminal of the semiconductor device, as mounted on the printed-wiring substrate; a second node formed on the printed-wiring substrate and connected with a supply voltage; and a third node formed on the printed-wiring substrate and connected with a reference voltage, and the function switching means is means for switching the function switching signals altogether, as inputted to the function switching external terminals, with or without conducting means

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provided between the first node and the second node or the third node.

According to the present invention, moreover, the function switching means is arranged at or in the vicinity of a corner portion of the printed-wiring substrate.

According to the present invention, moreover, the function of the semiconductor device to be switched by the function switching means includes a reading mode.

According to the present invention, moreover, the function of the semiconductor device to be switched by the function switching means includes a refresh cycle.

According to the present invention, moreover, the function of the semiconductor device to be switched by the function switching means includes a reading mode and a refresh cycle.

According to the present invention, moreover, the semiconductor device further includes word structure switching external terminals for selecting a word structure in dependence upon the state of a word structure switching signal, and the printed-wiring substrate further includes a word structure setting circuit for inputting a preset word structure switching signal to the word structure switching external terminals.

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According to the present invention, a memory module comprises at least one semiconductor device including word structure switching external terminals for selecting a word structure in dependence upon the state of a word structure switching signal; and a
5 dedicated printed-wiring substrate with the semiconductor device mounted thereon and including dedicated lines corresponding to the switched word structure of the semiconductor device.

10 According to the present invention, moreover, the memory module further comprises word structure switching means mounted on the dedicated printed-wiring substrate for selecting an arbitrary word structure switching signal to be inputted to the word
15 structure switching external terminals.

According to the present invention, moreover, the word structure switching means includes a word structure setting circuit wired on the dedicated printed-wiring substrate and adapted to be switched to
20 a predetermined word structure by mounting the semiconductor device so that a predetermined word structure switching signal is inputted to the word structure switching external terminals.

According to the present invention, moreover, the
25 word structure switching means includes a fourth node

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formed on the dedicated printed-wiring substrate and electrically connected with the word structure switching external terminal of the semiconductor device, as mounted on the dedicated printed-wiring
5 substrate; a fifth node formed on the dedicated printed-wiring substrate and connected with a supply voltage; and a sixth node formed on the dedicated printed-wiring substrate and connected with a reference voltage, and the word structure switching
10 means is means for switching the word structure switching signals altogether, as inputted to the word structure switching external terminals, with or without conducting means provided between the fourth node and the fifth node or the sixth node.

15 According to the present invention, moreover, the semiconductor device further includes function switching external terminals for selecting a function in dependence upon the state of a function switching signal, and the dedicated printed-wiring substrate
20 further includes function switching means for selecting an arbitrary function switching signal to be inputted to the function switching external terminals.

According to the present invention, moreover, the function switching means includes a first node (or
25 electrode) formed on the dedicated printed-wiring



substrate and electrically connected with the function
switching external terminal of the semiconductor
device, as mounted on the dedicated printed-wiring
substrate; a second node (or electrode) formed on the
5 dedicated printed-wiring substrate and connected with
a supply voltage; and a third node (or electrode)
formed on the dedicated printed-wiring substrate and
connected with a reference voltage (or ground
potential), and the function switching means is means
10 for switching the function switching signals
altogether, as inputted to the function switching
external terminals, with or without conducting means
provided between the first node and the second node or
the third node.

15 According to the present invention, moreover, the
function of the semiconductor device to be switched by
the function switching means includes a reading mode.

 According to the present invention, moreover, the
function of the semiconductor device to be switched by
20 the function switching means includes a refresh cycle.

 According to the present invention, moreover, the
function of the semiconductor device to be switched by
the function switching means includes a reading mode
and a refresh cycle.

25 According to the present invention, moreover, the

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function switching means includes a function setting circuit wired on the dedicated printed-wiring substrate and adapted to be switched to a predetermined function by mounting the semiconductor device so that a predetermined function switching signal is inputted to the function switching external terminals.

According to the present invention, a process for manufacturing a memory module comprises the step of preparing a semiconductor device for selecting a predetermined word structure on the basis of a word structure switching signal, as inputted to word structure switching external terminals, and a plurality of kinds of dedicated printed-wiring substrates corresponding to a plurality of word structures, and selecting one of the dedicated printed-wiring substrates, as corresponding to a demanded word structure of the semiconductor device, from the plurality of kinds of dedicated printed-wiring substrates; and the step of mounting the semiconductor device on the selected one of the dedicated printed-wiring substrates.

According to the present invention, moreover, a process for manufacturing a memory module comprises the step of preparing a semiconductor device for

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switching a word structure on the basis of a word structure switching signal, as inputted to word structure switching external terminals, and for selecting a function on the basis of a function switching signal, as inputted to function switching external terminals, function switching means for selecting an arbitrary function switching signal, as inputted to the function switching external terminals, with or without conducting means provided, and a plurality of kinds of dedicated printed-wiring substrates corresponding to a plurality of word structures, and selecting one of the dedicated printed-wiring substrates, as corresponding to a demanded word structure of the semiconductor device, from the plurality of kinds of dedicated printed-wiring substrates; the step of mounting the semiconductor device on the selected one of the dedicated printed-wiring substrates; and the step of switching an arbitrary function selectively, with or without the conducting means provided.

According to the present invention, moreover, a process for manufacturing a memory module comprises the step of preparing a semiconductor device for selecting a predetermined word structure on the basis of a word structure switching signal, as inputted to

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word structure switching external terminals, and for switching a predetermined function on the basis of a function switching signal, as inputted to function switching external terminals, and a plurality of kinds of dedicated printed-wiring substrates corresponding to the switching operations of a plurality of word structures and a plurality of functions, and selecting one of the dedicated printed-wiring substrates, as corresponding to a demanded word structure of the semiconductor device and the switching operation of the function, from the plurality of kinds of dedicated printed-wiring substrates; and the step of mounting the semiconductor device on the selected one of the dedicated printed-wiring substrates.

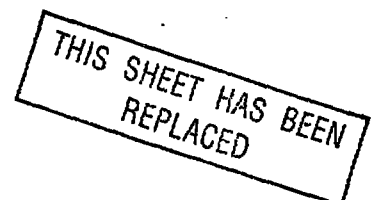
As described above, it is possible to improve the efficiency in the product development of the semiconductor device and to facilitate the product management thereby to reduce the cost.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is an explanatory diagram showing a construction of an essential portion of a memory according to Mode 1 of Embodiment of the present invention;

Fig. 2 is a pin arrangement diagram of the memory

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according to Mode 1 of Embodiment of the present invention;

Fig. 3 is an explanatory diagram showing internal connections of the memory according to Mode 1 of Embodiment of the present invention;

Fig. 4 is an explanatory table showing the mode switching operations of the memory according to Mode 1 of Embodiment of the present invention;

Fig. 5 is a connection diagram of one embodiment of a memory module, in which are mounted the memories according to the present invention;

Fig. 6 is a wiring diagram showing a module wiring substrate in which is mounted the memory according to Mode 1 of Embodiment of the present invention;

Fig. 7 is a mounting diagram of the module wiring substrate in which is mounted the memory according to Mode 1 of Embodiment of the present invention;

Fig. 8 is an explanatory diagram showing a mounting example of a jumper for switching the functions of the memory according to Mode 1 of Embodiment of the present invention;

Fig. 9 is a block diagram showing the memory module according to Mode 1 of Embodiment of the present invention;

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Fig. 10 is a mounting diagram showing the module mounting substrate in which is mounted a memory according to another mode of embodiment of the present invention;

5 Figs. 11A to 11E are standards diagrams of the module wiring substrate according to another mode of embodiment of the present invention;

Fig. 12 is a block diagram showing the memory module according to another mode of embodiment of the present invention;

Fig. 13 is a pin arrangement diagram of a memory according to Mode 2 of Embodiment of the present invention;

Fig. 14 is a connection diagram of another embodiment of the memory module in which are mounted memories according to the present invention;

Fig. 15 is a connection diagram of another embodiment of the memory module in which are mounted memories according to the present invention;

20 Fig. 16 is a connection diagram of another embodiment of the memory module in which are mounted memories according to the present invention;

Fig. 17 is a pin arrangement diagram showing a memory according to another mode of embodiment of the present invention; and

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Fig. 18 is an explanatory diagram showing the internal connections of a memory according to another mode of embodiment of the present invention.

5 DESCRIPTION OF THE PREFERRED EMBODIMENTS

In the present Mode 1 of Embodiment, a memory 1, as made of a TCP (tape carrier package) type DRAM semiconductor device or a kind of surface mount package, has the bonding pads BP or electrodes which
10 are arranged at the central portion of a semiconductor chip 2.

On the other hand, the memory 1 is given such a structure that the aforementioned semiconductor chip 2 is mounted on the tape carriers which are prepared by
15 forming the wiring lines 4 of copper foil as leads repeatedly over the upper face of a film of polyimide.

Moreover, the bonding pads BP, as arranged on the semiconductor chip 2, are individually electrically connected with inner leads 4a, as formed in the tape
20 carriers, at the leading end portions of the wiring lines 4. Still moreover, the inner leads 4a are extended to form outer leads 4b to be electrically connected with external connection electrodes such as lands, as formed on the later-described module wiring
25 substrate.

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On the other hand, the semiconductor chip 2 and the inner leads 4a are sealed with an epoxy resin, for example, to form a package, and the individual leads, as protruding from the package, are bent generally in a crank shape.

Next, the memory 1 is constructed to include twenty eight pins in total, as shown in Fig. 2. Of these, the 2nd and 27th pins, as connected with bonding pads BP1 and BP0 for switching the functions, have outer leads acting as function switching pins (or function switching external terminals) FP1 and FP0.

On the other hand, the memory 1 is equipped with bonding pads BP3 and BP2 for switching the word structure so that the word structure is arbitrarily switched depending upon the states of signals to be inputted to the bonding pads BP3 and BP2.

In Fig. 2, moreover, there are provided data input/output pins IO0 to IO3, a pin WE for designating whether the access is to read or write, address input pins A0 to A11, pins RAS and CAS for row and column selecting signals, a pin OE for a signal to control the states of a data output signal and a data input/output signal at a reading time, a pin Vcc for a supply voltage Vcc, and a pin Vss for a ground potential (or earth potential) or the reference

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potential.

Next, the internal connection structure in the memory 1 will be specifically described with reference to Fig. 3.

5 First of all, the memory 1 is shown to have the arrangement of only: the function switching bonding pads BP1 and BP0 or the electrodes, as electrically connected with the function switching pins FP1 and FP0 of the 2nd and 27th pins, and the bonding pads BP3 and
10 BP2 for switching the word structure, of the bonding pads BP formed on the semiconductor chip 2; and the wiring lines 4 for the supply voltage Vcc of the 1st and 14th pins, and the wiring lines 4 for the ground potential of the 15th and 28th pins.

15 Here in the memory 1, the function means the reading mode which is constructed to include a refresh cycle or the cycle for a refreshing operation, and FAST PAGE and EDO.

As shown in Fig. 4, moreover, the memory 1 can
20 switch the refresh cycle, the reading modes of FAST PAGE AND EDO, and three kinds of word structures of 4 M x 1 bit, 1 M x 4 bits and 512 K x 8 bits.

On the other hand, these function switching operations in the memory 1 are executed by inputting
25 the supply voltage Vcc, the ground potential Vss or

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the function switching signal, as selected from the no connections, to the connection destinations of the function switching bonding pads BP1 and BP0, as arranged in the predetermined positions of the semiconductor chip 2 shown in Fig. 3, that is, the pins FP0 and FP1 for switching the functions of the 2nd and 27th pins, and by combining those function switching signals in the aforementioned manner, as shown in Fig. 4.

Moreover, the connection destinations of the word structure switching bonding pads BP3 and BP2 are predetermined by the wiring lines 4a, as formed on the tape carriers. In the memory 1 of the present Mode of Embodiment, as shown in Fig. 2, the bonding pads BP3 and BP2 have no connection.

In the word structure of the memory 1, therefore, the bonding pads BP3 and BP2 have no connection (as indicated by 'OPEN' in Fig. 4), as shown in Fig. 4, so that the word structure of 4 K x 4 bits is automatically selected.

On the other hand, if the function switching signal to be inputted to the function switching pin FP0 is OPEN (in Fig. 4) and if the function switching signal to be inputted to the function switching pin FP1 is exemplified by the supply voltage Vcc, the

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memory 1 is selected for the function in which the refresh cycle is 2 K and in which the reading mode is FAST PAGE.

With reference to Fig. 5, here will be described
5 a method of switching the function of the memory 1 and the word structure. Moreover, Fig. 5 does not explain the actual mounting arrangement but schematically shows the connection state of the memory 1 in a memory module MM.

10 First of all, in the memory module MM of Fig. 5, a module wiring substrate (or printed-wiring substrate) 5 for mounting the memory 1 is equipped with function switching means KK1 for arbitrarily
15 switching the function switching signal to be inputted to the function switching pin FP0 of the memory 1, and function switching means KK2 for arbitrarily switching the function switching signal to be inputted to the function switching pin FP1 of the memory 1.

On the other hand, the function switching signal
20 is selected from any of the no connection, the supply voltage Vcc and the ground potential Vss.

Moreover, the function switching pins FP0 and FP1 of all the memories 1, as mounted on the module wiring substrate 5, are so wired by a wiring pattern HP that
25 they are connected with the function switching means



KK1 and KK2, respectively.

By these function switching means KK1 and Kk2, moreover, the aforementioned function switching signals can be arbitrarily switched and inputted as a whole to all the mounted memories 1 so that the functions, as constructed to include the reading mode and the refresh cycle as shown in Fig. 4, can be switched and arbitrarily set.

With reference to Figs. 6 and 7, here will be specifically described the memory module which is actually provided with the aforementioned function switching means KK1 and KK2 for switching the functions.

First of all, the memory module is constructed by mounting the TCP type memories 1 (as shown in Fig. 2) or a surface mounting package to make a predetermined memory structure. In this memory module, the module wiring substrate 5 for mounting the memories 1 has a front surface 5a and a back surface 5b, on which a predetermined number of memories 1 are mounted in the longitudinal direction of the module wiring substrate 5. The memories 1, as mounted on the surfaces 5a and 5b of the module wiring substrate 5, are stacked in two stages to make a stacked structure.

On the surfaces 5a and 5b of the module wiring

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substrate 5, moreover, there are formed the lands which are so electrically connected with predetermined destinations that the memories 1 and the various chip parts necessary for the memory module may be mounted.

5 In the vicinity of the corner portion of one longer side of the back surface 5b of the module wiring substrate 5, on the other hand, there are provided: a land (or a first node) L1 for mounting a later-described conducting chip for switching the
10 state of the function switching signal to the function switching pin FP0 (as shown in Fig. 2), as disposed in the memory 1, a land (or a second node) L2, a land (or a third node) L3, a land (or a first node) L4 for mounting a conducting chip for switching the state of
15 the function switching signal to the function switching pin FP1 (as shown in Fig. 2), a land (or a second node) L5, and a land (or a third node) L6.

At the other longer side of the surfaces 5a and 5b of the module wiring substrate 5, moreover, there
20 are provided a predetermined number of module I/O terminals MT which are arranged in the longitudinal direction of the module wiring substrate 5.

On the surfaces 5a and 5b of the module wiring substrate 5, moreover, there are formed the wiring
25 patterns, by which the individual lands and module I/O



terminals MT are individually electrically connected with the predetermined connection destinations.

The land L1 is electrically connected by a predetermined wiring pattern with the land, at which
5 are overlapped the function switching pins FP0 of all the mounted memories 1, and the land L2 is electrically connected through the wiring pattern with the supply voltage Vcc whereas the land L3 is electrically connected through the wiring pattern with
10 the ground potential Vss.

The later-described conducting chip is mounted or not between the land L1 and the land L2 or between the land L1 and the land L3 so that it may be inputted as the function switching signal to the memory 1 to
15 effect the function switching operations selectively all at once.

The function switching means KK1 is constructed to include those lands L1 to L3 and the conducting chips.

20 The land L4 of the module wiring substrate 5 is electrically connected by a predetermined wiring pattern with the land, at which are overlapped the function switching pins FP1 of all the memories 1 to be mounted, and the land L5 is electrically connected
25 with the supply voltage Vcc through the wiring pattern

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whereas the land L6 is electrically connected with the ground potential Vss through the wiring pattern.

The later-described conducting chip is mounted or not between the land L4 and the land L5 or between the land L4 and the land L6 so that it may be inputted as the function switching signal to the memory 1 to effect the function switching operations selectively all at once.

The function switching means KK2 is constructed to include those lands L4 to L6 and the conducting chips.

The lands L1 to L3 and L4 to L6 of the module wiring substrate 5 for mounting the conducting chips are formed in the vicinity of the corner portion of one longer side, where the module I/O terminals MT are not disposed, so that the conducting chips can be easily mounted/demounted even for the memory module MM which is sealed by the metal case.

By mounting the memories 1 and the chip parts in the module wiring substrate 5, as shown in Fig. 7, moreover, there is constructed the memory module MM called 8-byte DIMM (dual inline memory module).

Here in Fig. 7, the memories 1 are switched such that the word structure is set in advance to $4\text{ M} \times 4$ bits and such that the switching of the functions is

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so selected by the function switching signal inputted to the function switching pins FP0 and FP1 as to set the refresh cycle to 2 K cycle and the reading mode to FAST PAGE.

5 When the refresh cycle is set to 2 K cycle and the reading mode is set to FAST PAGE, as described above, it is found from Fig. 4 that the function switching signal to be inputted to the function switching pin FP0 may be non-connected whereas the
10 function switching signal to be inputted to the function switching pin FP1 may be selected to the supply voltage Vcc.

As a result, the function switching pin FP0 is open so that the conducting chips or the chip parts
15 such as jumpers or resistors are not mounted on the lands L1 to L3 to bring the function switching pins FP0 of all the memories 1, as mounted on the module wiring substrate 5, altogether into open state.

Since the supply voltage Vcc is inputted to the
20 function switching pin FP1, on the other hand, a conducting chip (or conducting means) JC or a chip part such as a jumper or resistor is mounted between the land L4 and the land L5, as connected with the supply voltage Vcc, so that the supply voltage Vcc is
25 inputted to the function switching pins FP1 of all the

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memories 1, as mounted on the module wiring substrate
5.

Thus, when the supply voltage V_{CC} is to be fed to
the function switching pins FP1 of all the memories 1
5 (as shown in Fig. 2), as shown in Fig. 8, it is
sufficient to mount the conducting chip JC between the
land L4 and the land L5 of the module wiring substrate
5 (as shown in Fig. 6).

Here, the connection state in this memory module
10 MM is shown in a block diagram of Fig. 9. As shown in
Fig. 9, the function switching signals to be inputted
to the function switching pins FP1 and FP0 of all the
memories 1 are selectively switched altogether by the
function switching means KK1 and KK2.

15 Next, there is shown in Fig. 10 a mounting
example of the case in which the memory module MM is
made of the SODIMM (small outlet dual inline memory
module).

In this case, too, a predetermined number of TCP
20 type memories 1 are mounted individually on the
surfaces 5a and 5b of the module wiring substrate 5 to
construct the predetermined memory structure so that
the memories 1 make the stacked structure in which
they are mounted in two stages.

25 In the vicinity of the corner portion of one



longer side of the front surface 5a of the module wiring substrate 5, on the other hand, as in the aforementioned 8-byte DIMM memory module, there are disposed the lands L1, L3, L4 and L5 for mounting the
5 later-described conducting chips for switching the states of the function switching signals to the function switching pins FP0 and FP1, as mounted in the memory 1.

Moreover, the land L1 is electrically connected
10 by a predetermined wiring pattern with the land in which are overlapped the function switching pins FP0 of all the mounted memories 1, and the land L3 is electrically connected through the wiring pattern with the ground potential Vss.

15 On the other hand, the land L4 is electrically connected by a predetermined pattern with the land in which are overlapped the function switching pins FP1 of all the mounted memories 1, and the land L5 is electrically connected through a wiring pattern with
20 the supply voltage Vcc.

Moreover, the conducting chip is mounted or not between the land L1 and the land L3 or between the land L4 and the land L5 so that the function switching signal is inputted to the memory 1 to effect the
25 function switching operations selectively altogether.

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Moreover, the lands L1 and L3 or the lands L4 and L5 of the module wiring substrate 5 for mounting the conducting chips or the chip parts such as the jumpers or resistors are formed in the vicinity of the corner portion of one longer side, where the module I/O terminals MT are not disposed, as shown in Fig. 10, and the conducting chips can be easily mounted/demounted even from the memory module which is sealed by the metal case.

10 On the other hand, the module wiring substrate 5 to be used in the memory module made of the SODIMM is formed according to the standards, as shown in Figs. 11A, 11B, 11C, 11D and 11E.

Moreover, the connection state in the memory module MM is shown in a block diagram in Fig. 12.

As shown in Fig. 12, the function switching signals to be inputted to the function switching pins FP1 of all the memories 1 are selectively switched altogether to either the supply voltage Vcc or the non-connection by the function switching means KK1, and the function switching signals to be inputted to the function switching pins FP0 of all the memories 1 are selectively switched altogether to the ground potential Vss or no connection by the function switching means KK2.

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As a result, when the input of the function switching pin FP0 is open (as indicated by 'OFF' in Fig. 12), the reading mode is the FAST PAGE. When the input of the function switching pin FP0 is at the ground potential Vss (as indicated by 'ON' in Fig. 12), the reading mode is the EDO mode.

On the other hand, when the input of the function switching pin FP1 is open, the refresh cycle is 4 K cycle. When the input of the function switching pin FP1 is at the supply voltage Vcc (as indicated by 'ON' in Fig. 12), the refresh cycle is 2 K cycle.

With the reading mode being the EDO and the refresh cycle being 4 K cycle, for example, the input of the function switching pin FP0 is at the ground potential Vss, and the input of the function switching pin FP1 may be open. As shown in Fig. 10, therefore, the conducting chip JC may be mounted between the land L1 and the land L3 but may be omitted between the lands L4 and L5.

Here, the function switching signal is selectively switched to either the supply voltage Vcc or no connection, or the ground potential Vss or no connection by the function switching means KK1 and KK2. However, these function switching means KK1 and KK2 are made to select the supply voltage Vcc, the



ground potential Vss or no connection so that those function switching signals can be combined to switch the functions in the memory 1.

- As a result, the following effects can be
- 5 achieved according the present Mode 1 of Embodiment.
- (1) The functions of all the mounted memories 1 can be switched and set altogether by the function switching means KK1 and KK2 so that the functions of the memory module MM can be easily switched for a
- 10 short time period.
- (2) The assembly specifications of the memory module MM can be made common to improve the developing efficiency of products and facilitate the product management.
- 15 (3) By providing the function switching means KK1 and KK2 at the corner portion or in its vicinity of the module wiring substrate 5, the functions of the memories 1 even in the memory module, as completed as a product, can be easily switched for a short time
- 20 period to improve the degree of freedom for the productivity drastically.

Fig. 13 is a pin arrangement diagram of a memory according to Mode 2 of Embodiment of the present invention, and Figs. 14, 15 and 16 are explanatory

25 diagrams showing the memory module in which are

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mounted the memories according to the present invention.

In the present Mode 2 of Embodiment, a memory 1a is made of a TCP type DRAM semiconductor device or a kind of surface mounting package. As shown in Fig. 13, the memory 1a is constructed to include a total number 36 of pins. Of these, the 2nd and 35th pins, as connected with the function switching bonding pads BP1 and BP0, are provided with outer leads as the function switching pins FP1 and FP0 so that an arbitrary function is switched depending upon the state of the function switching signal inputted.

On the other hand, the memory 1a is equipped as word structure switching pins (or word structure switching external terminals) FP3 and FP2 with the outer leads of the 17th and 20th pins, as connected with the bonding pads BP3 and BP2 for switching the word structure, so that an arbitrary word structure is switched depending upon the state of the word structure switching signal to be inputted to the pins FP3 and FP2.

Moreover, there are provided data input/output pins IO0 to IO7, a pin WE for designating whether the access is to read or write, address input pins A0 to A11, pins RAS and CAS for row and column selecting



signals, a pin OE for a signal to control the states
of a data output signal and a data input/output signal
at a reading time, a pin Vcc for the supply voltage
Vcc, and a pin Vss for a ground potential or the
5 reference potential.

The internal connection structure in the memory
1a is specifically described below.

First of all, as shown in Fig. 4, for example,
the memory 1a can arbitrarily switch the functions to
10 switch the refresh cycle or the cycle of the
refreshing operation and the reading mode of FAST PAGE
and EDO, on the basis of the function switching
signals to be inputted to the function switching pins
FP1 and FP0, and can switch three kinds of word
15 structures of 4 M $\times$ 1 bit, 1 M $\times$ 4 bits and 512 K $\times$ 8
bits on the basis of the word structure switching
signals to be inputted to the word structure switching
pins FP3 and FP2.

The functions of the memory 1a are switched by
20 inputting the signals, as selected from the function
switching signals such as the supply voltage Vcc, the
ground potential Vss or no connection to the pins FP1
and FP0 for switching the functions of the 2nd and
35th pins, as shown in Fig. 13, and by combining those
25 signals, as shown in Fig. 4.

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The word structure of the memory 1a is likewise switched by inputting the signals, as selected from the word structure switching signals such as the supply voltage Vcc, the ground potential Vss or no connection, to the word structure switching pins FP3 and FP2 of the 17th and 20th pins for switching the word structure, and by combining those signals, as shown in Fig. 4.

With reference to Figs. 14, 15, 16 and 17, here will be described the method of switching the functions and the word structure of the memory 1a. On the other hand, Figs. 14, 15, 16 and 17 show not the actual mounting structure but schematically the connection state of the memories 1a in the memory module.

First of all, as shown in Fig. 14, the substrate to be used for mounting the memories 1a is exemplified by a dedicated module wiring substrate (or a dedicated printed-wiring substrate) 6 which is wired in advance to correspond to a predetermined word structure.

On the module wiring substrate 6, on the other hand, there are mounted the memories 1a which are equipped with the function switching pins FP1 and FP0 and the word structure switching pins FP3 and FP2.

On the module wiring substrate 6, moreover, there

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is wired a wiring pattern (or a word structure setting line) HP1 for inputting a predetermined word switching signal of no connection, the supply voltage Vcc or the ground potential Vss to the word structure switching pins FP3 and FP2 of the memories 1a so that a
5 predetermined word structure may be set.

On the other hand, the module wiring substrate 6 is equipped with the function switching means KK1 for arbitrarily switching the function switching signal,
10 as selected from no connection, the supply voltage Vcc or the ground potential Vss to be inputted to the function switching pins FP0 of the memories 1a, and the function switching means KK2 for arbitrarily switching the function switching signal, as likewise
15 selected from any of no connection, the supply voltage Vcc or the ground potential Vss to be inputted to the function switching pins FP1 of the memories 1a.

Moreover, The function switching pins FP0 and FP1 of all the memories 1a, as mounted on the module
20 wiring substrate 6, are so wired by the wiring pattern HP that they may be connected with the function switching means KK1 and KK2, respectively.

As a result, the aforementioned function switching signals can be arbitrarily switched by those
25 function switching means KK1 and KK2 to switch and set

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arbitrarily the functions including of the reading
mods and the refresh cycles, as shown in Fig. 4.

As a result, the functions of the memories 1a can
be arbitrarily switched and set by the function .

5 switching means KK1 and KK2 even before or after the
memories 1a are mounted.

Next, in order that an arbitrary word structure
may be set on the dedicated module wiring substrate 6
mounting the memories 1 thereon, as shown in Fig. 15,
10 there are provided word structure switching means WK1
and WK2 for switching any of no connection, the supply
voltage Vcc or the ground potential Vss arbitrarily as
the word structure switching signal to the word
structure switching pins FP3 and FP2 of the memories
15 1a.

On the module wiring substrate 6, on the other
hand, there are likewise provided the function
switching means KK1 and KK2 for switching the
aforementioned function switching signal arbitrarily
20 to the function switching pins FP0 and FP1 of the
memories 1a.

Moreover, the function switching pins FP0 and FP1
of all the memories 1a, as mounted on the module
wiring substrate 6, are so wired by the wiring pattern
25 HP that they may be connected with the function



switching means KK1 and KK2, respectively, and the word structure switching pins FP2 and FP3 of all the memories 1a are so wired by the wiring pattern HP that they may be connected with the word structure

5 switching means WK1 and WK2, respectively.

As a result, the function switching signals are arbitrarily switched by those function switching means KK1 and Kk2 to arbitrarily switch and set the functions including the reading modes and the refresh
10 cycles, as shown in Fig. 4.

The word structure switching signals are so switched by the word structure switching means WK1 and WK2 that the memories 1a may be switched and set to the word structure corresponding to the module wiring
15 substrate 6.

As a result, the functions and the word structures of the memories 1a can be arbitrarily switched and set by the function switching means KK1 and KK2 and the word structure switching means WK1 and
20 WK2 even before or after the memories 1a are mounted.

Only the word structure switching means for switching the word structures may be provided on the module wiring substrate, and the functions may be switched by wiring the wiring pattern, in which a
25 predetermined function switching signal is inputted to

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the function switching pins of the memories, as mounted for the predetermined function to be switched and set, so that the functions may be arbitrarily set by switching the word structures.

5 In this case, too, the dedicated module wiring substrate, as corresponding to the word structures and functions to be switched and set, is prepared to mount the memories thereon.

10 Next, on the dedicated module wiring substrate 6 having the memories 1a mounted thereon, as shown in Fig. 16, there are formed the wiring pattern HP1, which is so wired that the preset word structure switching signal may be inputted to the word structure switching pins FP3 and FP2, and a wiring pattern (or a
15 function setting line) HP2 which is so wired that the preset function switching signal may be inputted to the function switching pins FP1 and FP0.

20 The functions and the word structures of the memories 1a are automatically switched and set by selecting the dedicated module wiring substrate 6, for which the predetermined function and word structure are switched and set in advance, and by mounting the memories 1a on the selected module wiring substrate 6.

25 The aforementioned function switching means KK1 is constructed to include conducting chips for

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selecting the state of the function switching signal to the function switching pin FP0 (as shown in Fig. 13), as mounted on the memories 1a, and mounting lands for mounting the conducting chips.

5 These mounting lands include: function lands electrically connected by a predetermined wiring pattern with the lands, at which are overlapped the function switching pin FP0; power lands electrically connected through the wiring pattern with the supply
10 voltage Vcc; and ground lands electrically connected through the wiring pattern with the ground potential Vss.

 Likewise, the aforementioned function switching means KK2 is also constructed to include conducting
15 chips for switching the state of the function switching signal to the function switching pin FP1 (as shown in Fig. 13), as mounted on the memories 1a, and mounting lands for mounting the conducting chips.

 These mounting lands include: function lands
20 electrically connected by a predetermined wiring pattern with the lands, at which are overlapped the function switching pin FP1; power lands electrically connected through the wiring pattern with the supply voltage Vcc; and ground lands electrically connected
25 through the wiring pattern with the ground potential



Vss.

With or without the conducting chips provided between the function lands and the power lands or between the function lands and the ground lands, any of the supply voltage Vcc, the ground potential Vss and no connection may be arbitrarily selected and inputted as the function switching signal to the memories 1a to effect the function switching operations selectively altogether.

10 Next, the aforementioned word structure switching means WK1 include conducting chips (or conducting means) for switching the state of the function switching signal to the word structure switching pins FP2 (as shown in Fig. 13), as mounted on the memories 1a, and mounting lands for mounting the conducting chips thereon.

These mounting lands include: word lands (or fourth nodes) electrically connected by a predetermined wiring pattern with the lands, at which are overlapped the word structure switching pins FP2; power lands (or fifth nodes) electrically connected through the wiring pattern with the supply voltage Vcc; and ground lands (or sixth nodes) electrically connected through the wiring pattern with the ground potential Vss.

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The word structure switching means WK2 is constructed to include conducting chips for switching the state of the function switching signal to the word structure switching pins FP3 (as shown in Fig. 13), as
5 mounted on the memories 1a, and mounting lands for mounting the conducting chips thereon.

These mounting lands include: word lands electrically connected by a predetermined wiring pattern with the lands, at which are overlapped the
10 word structure switching pins FP3; power lands electrically connected through the wiring pattern with the supply voltage Vcc; and ground lands electrically connected through the wiring pattern with the ground potential Vss.

15 With or without the conducting chips provided between the word lands and the power lands or between the word lands and the ground lands, any of the supply voltage Vcc, the ground potential Vss and the non-connection may be arbitrarily selected and inputted as
20 the function switching signal to the memories 1a to effect the word switching operations selectively altogether.

The mounting lands for mounting the aforementioned conducting chips are arranged in the
25 vicinity of the corner portion of the module wiring

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substrate 6 so that they can be easily mounted/
demounted even from the memory module which is
shielded by the metal case.

As a result, the following effects can be
5 achieved according the present Mode 2 of Embodiment.

(1) The functions and word structures of all the
mounted memories 1a can be switched altogether by the
function switching means KK1 and KK2 and the word
structure switching means WK1 and WK2 so that the
10 functions of the memory module MM can be easily
switched for a short time period.

(2) Thanks to the aforementioned effect (1), the
specifications of the film to be used for the memories
1a can be made common to reduce the cost and improve
15 the productivity.

(3) The assembly specifications of the memory module
MM can be made common to improve the developing
efficiency of products and facilitate the product
management.

20 (4) By providing the function switching means KK1 and
KK2 and the word structure switching means WK1 and WK2
at the corner portion or in its vicinity of the module
wiring substrate 6, the functions of the memories 1a
even in the memory module, as completed as a product,
25 can be easily switched for a short time period.



The present Mode 2 of Embodiment has been described on the TCP type memories 1a. Despite of this description, however, the memory module may be constructed by using either the memories having BGA
5 (ball grid array) structure such as the CSP (chip size package) type made of a package having an external diameter substantially equal to that of the semiconductor chip or the memories having the LOC (lead on chip) structure of the SOJ (small outline
10 j-leaded Package) type.

In a CSP type memory 1b, for example, predetermined pins are assigned as the function switching pins FP1 and FP0 for switching the functions and the word structure switching pins FP3 and FP2 for
15 switching the word structures, as shown in Fig. 17.

On the module wiring substrate having those memories 1b mounted thereon, on the other hand, there are also provided the function switching means and the word structure switching means so that the functions
20 and the word structures can be arbitrarily switched by inputting the function switching signals to the function switching pins FP1 and FP0 and the word structure switching signals to the word structure switching pins FP3 and FP2.

25 Next, in the SOJ type memory 1c, for example, the

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predetermined pins are assigned as the function switching pins FP1 and FP0 for switching the functions and the word structure switching pins FP3 and FP2 for switching the word structures. These function
5 switching pins FP1 and FP0 and word structure switching pins FP3 and FP2 are electrically connected bonding wires W with the bonding pads, as mounted on the semiconductor chips 2, such as the predetermined function switching pads BP1 and BP0 and the word
10 structure switching pads BP3 and BP2, respectively.

On the module wiring substrate for mounting the memories 1c, on the other hand, there are also mounted the function switching means and the word structure switching means so that the functions and the word
15 structures can be arbitrarily switched by inputting the function switching signals to the function switching pins FP1 and FP0 and the word structure switching signals to the word structure switching pins FP3 and FP2.

20 Although our invention has been specifically described on the basis of its modes of embodiment, it should not be limited to the aforementioned modes of embodiment but can naturally be modified in various manners without departing from the gist thereof.

25 In the foregoing Modes 1 and 2 of Embodiment, for

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example, the function switching signals and the word structure switching signals are fed altogether by the function switching means and the word structure switching means to all the memories that are mounted
5 on the memory module. Despite of this fact, however, the function switching signals and the word structure switching signals need not be fed altogether to all the memories mounted on the memory module, but the function switching means and the word structure
10 switching means may be provided for every two or three memories.

In the foregoing Modes 1 and 2 of Embodiment, on the other hand, the connection destinations are switched by selectively mounting/demounting the
15 conducting chips or the chip parts such as the jumpers or resistors. However, the function switching signals to be inputted to the function switching pins of the memories and the word structure switching signals to be inputted to the word structure switching pins may
20 be selected and switched to the module wiring substrate by using the semiconductor device such as the EEPROM (electrically erasable programmable read only memory).

In this modification, the predetermined pins of
25 the EEPROM are electrically connected by a wiring



pattern with the function switching pins of the individual memories which are mounted on the module wiring substrate.

To the EEPROM, there is inputted in advance a
5 program for giving predetermined functions to the individual memories so that the EEPROM switches the functions and the word structures of the memories by setting on the basis of the program the electric levels of predetermined pins, as connected with the
10 function switching pins and the word structure switching pins, to any of the supply voltage, the ground voltage or no connection.

In the foregoing Modes 1 and 2 of Embodiment, moreover, when the function switching pins and the
15 word structure switching pins are open, the conducting chips, as connected with the function switching pins, are not mounted. However, this non-connection state may be effected by cutting the non-connected function switching pins and word structure switching pins from
20 the package end portions at the lead cutting step and disconnecting them from the lands for mounting the memories.

In the foregoing Modes 1 and 2 of Embodiment, on the other hand, the operations to switch the functions
25 of the memories are effected by the reading modes



including the refresh cycles and the FAST PAGE and EDO. However, the various switching operations such as the DRAM operation modes or the synchronous DRAM operation modes may be effected from the outside by
5 the function switching means.

Effects of the Invention

The effects to be obtained from the representatives of the invention, as disclosed herein, will be briefly described in the following.

10 (1) According to the present invention, the assembly specifications of the memory module can be made common to make it unnecessary to manage the semiconductor device for the individual functions.

(2) In the present invention, on the other hand, the
15 functions of the semiconductor device can be arbitrarily switched even after the memory module is completed, so that the specifications of the printed-wiring substrate can be unified to cope with the change in the specifications flexibly.

20 (3) In the present invention, moreover, the functions of the semiconductor device can be easily switched at a low cost by selectively mounting/demounting the conducting means such as the jumpers or resistors.

(4) In the present invention, moreover, thanks to the
25 aforementioned effects (1) to (3), it is possible to

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drastically improve the product developing efficiency
and the productivity of the semiconductor device and
to facilitate the product management.

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WE CLAIM:

1. A memory module comprising:
at least one semiconductor device including
5 function switching external terminals for selecting a
function in dependence upon the state of a function
switching signal; and
a printed-wiring substrate with said
semiconductor device mounted thereon and including
10 function switching means for selecting an arbitrary
function switching signal to be inputted to said
function switching external terminals.
2. A memory module according to claim 1,
15 wherein said function switching means includes:
a first node formed on said printed-wiring
substrate and electrically connected with the function
switching external terminal of said semiconductor
device, as mounted on said printed-wiring substrate;
20 a second node formed on said printed-wiring
substrate and connected with a supply voltage; and
a third node formed on said printed-wiring
substrate and connected with a reference voltage, and
wherein said function switching means is means
25 for switching the function switching signals

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altogether, as inputted to said function switching external terminals, with or without conducting means provided between said first node and said second node or between said first node and said third node.

5

3. A memory module according to claim 1,
wherein said function switching means is arranged at or in the vicinity of a corner portion of said printed-wiring substrate.

10

4. A memory module according to claim 1,
wherein the function of said semiconductor device to be switched by said function switching means includes a reading mode.

15

5. A memory module according to claim 1,
wherein the function of said semiconductor device to be switched by said function switching means includes a refresh cycle.

20

6. A memory module according to claim 1,
wherein the function of said semiconductor device to be switched by said function switching means includes a reading mode and a refresh cycle.

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7. A memory module according to claim 1,
wherein said semiconductor device further
includes word structure switching external terminals
for selecting a word structure in dependence upon the
5 state of a word structure switching signal, and
wherein said printed-wiring substrate further
includes word structure setting lines for inputting a
preset word structure switching signal to said word
structure switching external terminals.

10

8. A memory module comprising:

at least one semiconductor device including word
structure switching external terminals for selecting a
word structure in dependence upon the state of a word
15 structure switching signal; and

a dedicated printed-wiring substrate with said
semiconductor device mounted thereon and including
dedicated lines corresponding to the switched word
structure of said semiconductor device.

20

9. A memory module according to claim 8, further
comprising: word structure switching means mounted on
said dedicated printed-wiring substrate for selecting
an arbitrary word structure switching signal to be
25 inputted to said word structure switching external

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terminals.

10. A memory module according to claim 9,

wherein said word structure switching means

5 includes word structure setting lines wired on said
dedicated printed-wiring substrate and adapted to be
switched to a predetermined word structure by mounting
said semiconductor device so that a predetermined word
structure switching signal is inputted to said word
10 structure switching external terminals.

11. A memory module according to claim 9,

wherein said word structure switching means

includes:

15 a fourth node formed on said dedicated printed-
wiring substrate and electrically connected with the
word structure switching external terminal of said
semiconductor device, as mounted on said dedicated
printed-wiring substrate;

20 a fifth node formed on said dedicated printed-
wiring substrate and connected with a supply voltage;
and

a sixth node formed on said dedicated printed-
wiring substrate and connected with a reference
25 voltage, and

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wherein said word structure switching means is means for switching the word structure switching signals altogether, as inputted to said word structure switching external terminals, with or without
5 conducting means provided between said fourth node and said fifth node or between said fourth node and said sixth node.

12. A memory module according to claim 8,
10 wherein said semiconductor device further includes function switching external terminals for selecting a function in dependence upon the state of a function switching signal, and

wherein said dedicated printed-wiring substrate
15 further includes function switching means for selecting an arbitrary function switching signal to be inputted to said function switching external terminals.

20 13. A memory module according to claim 12, wherein said function switching means includes:
a first node formed on said dedicated printed-wiring substrate and electrically connected with the function switching external terminal of said
25 semiconductor device, as mounted on said dedicated





printed-wiring substrate;

a second node formed on said dedicated printed-wiring substrate and connected with a supply voltage;
and

5 a third node formed on said dedicated printed-wiring substrate and connected with a reference voltage, and

wherein said function switching means is means for switching the function switching signals
10 altogether, as inputted to said function switching external terminals, with or without conducting means provided between said first node and said second node or between said first node and said third node.

15 14. A memory module according to claim 12,

wherein the function of said semiconductor device to be switched by said function switching means includes a reading mode.

20 15. A memory module according to claim 12,

wherein the function of said semiconductor device to be switched by said function switching means includes a refresh cycle.

25 16. A memory module according to claim 12,

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wherein the function of said semiconductor device to be switched by said function switching means includes a reading mode and a refresh cycle.

5 17. A memory module according to claim 12,

wherein said function switching means includes function setting lines wired on said dedicated printed-wiring substrate and adapted to be switched to a predetermined function by mounting said at least one
10 semiconductor device so that a predetermined function switching signal is inputted to said function switching external terminals.

18. A process for manufacturing a memory module,
15 comprising:

the step of preparing a semiconductor device for switching a predetermined word structure on the basis of a word structure switching signal, as inputted to word structure switching external terminals, and a
20 plurality of kinds of dedicated printed-wiring substrates corresponding to a plurality of word structures, and selecting one of said dedicated printed-wiring substrates, as corresponding to a demanded word structure of said semiconductor device,
25 from said plurality of kinds of dedicated printed-





wiring substrates; and

the step of mounting said semiconductor device on the selected one of said dedicated printed-wiring substrates.

5

19. A process for manufacturing a memory module, comprising:

the step of preparing a semiconductor device for selecting a word structure on the basis of a word structure switching signal, as inputted to word structure switching external terminals, and for selecting a function on the basis of a function switching signal, as inputted to function switching external terminals, function switching means for selecting an arbitrary function switching signal, as inputted to said function switching external terminals by mounting conducting means or not, and a plurality of kinds of dedicated printed-wiring substrates corresponding to a plurality of word structures, and selecting one of said dedicated printed-wiring substrates, as corresponding to a demanded word structure of said semiconductor device, from said plurality of kinds of dedicated printed-wiring substrates;

25 the step of mounting said semiconductor device on





the selected one of said dedicated printed-wiring
substrates; and

the step of selecting an arbitrary function
selectively, with or without said conducting means
5 provided.

20. A process for manufacturing a memory module,
comprising:

the step of preparing a semiconductor device for
10 selecting a predetermined word structure on the basis
of a word structure switching signal, as inputted to
word structure switching external terminals, and for
selecting a predetermined function on the basis of a
function switching signal, as inputted to function
15 switching external terminals, and a plurality of kinds
of dedicated printed-wiring substrates corresponding
to the switching operations of a plurality of word
structures and a plurality of functions, and selecting
one of said dedicated printed-wiring substrates, as
20 corresponding to a demanded word structure of said
semiconductor device and the switching operation of
the function, from said plurality of kinds of
dedicated printed-wiring substrates; and

the step of mounting said semiconductor device on
25 the selected one of said dedicated printed-wiring

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substrates.

21. A memory module comprising:
- 5 a wiring substrate having arranged lines;
- a semiconductor device; and
- a function switching circuit,
- wherein said semiconductor device includes
- function switching terminals for selecting an internal
- function and mounted on said wiring substrate, and
- 10 wherein said function switching circuit is
- electrically connected with the function switching
- terminals of said semiconductor device and is arranged
- on said wiring substrate.
- 15 22. A memory module according to claim 21,
- wherein said function switching circuit includes
- a first electrode, a second electrode and a third
- electrode,
- wherein said first electrode is electrically
- 20 connected with said function switching terminal,
- wherein said second electrode is at a supply
- voltage,
- wherein said third electrode is at ground
- potential, and
- 25 wherein the function of said semiconductor device

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is switched by rendering said first electrode and said second electrode, or said first electrode and said third electrode conductive or inconductive.

- 5 23. A memory module according to claim 22, further comprising: a conducting element for rendering the first electrode and the second electrode, or the first electrode and the third electrode of said function switching circuit conductive.

10

24. A memory module according to claim 22, wherein the function of said semiconductor device to be switched by said function switching circuit includes a reading mode.

15

25. A memory module according to claim 22, wherein the function of said semiconductor device to be switched by said function switching circuit includes a refresh cycle.

20

26. A memory module comprising:
a wiring substrate having arranged lines;
a semiconductor device;
a function switching circuit; and
25 word structure setting lines,

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wherein said semiconductor device includes
function switching terminals for switching an internal
function and mounted on said wiring substrate, and
word structure switching terminals for selecting a
5 word structure, and

wherein said function switching circuit is
electrically connected with the function switching
terminals of said semiconductor device and is arranged
on said wiring substrate.
10

27. A memory module according to claim 26,

wherein said function switching circuit includes
a first electrode, a second electrode and a third
electrode,

15 wherein said first electrode is electrically
connected with said function switching terminal,

wherein said second electrode is at a supply
voltage,

wherein said third electrode is at ground
20 potential, and

wherein the function of said semiconductor device
is switched by rendering said first electrode and said
second electrode, or said first electrode and said
third electrode conductive or inconductive.

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28. A memory module according to claim 27, further
comprising: a conducting element for rendering the
first electrode and the second electrode, or the first
electrode and the third electrode of said function
5 switching circuit conductive.

29. A memory module according to claim 27,,
wherein the function of said semiconductor device
to be switched by said function switching circuit
10 includes a reading mode.

30. A memory module according to claim 27,
wherein the function of said semiconductor device
to be switched by said function switching circuit
15 includes a refresh cycle.

31. A memory module comprising:
a wiring substrate having interconnections;
a semiconductor device;
20 a function switching circuit; and
word structure switching lines,
wherein said semiconductor device includes
function switching terminals for selecting an internal
function and mounted on said wiring substrate, and
25 word structure switching terminals for selecting a

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word structure,

wherein said function switching circuit is
connected with the function switching terminals of
said semiconductor device and is arranged on said
5 wiring substrate, and

wherein said word structure switching circuit is
electrically connected with said word structure
switching terminals and arranged on said wiring
substrate.

10

32. A memory module according to claim 31,

wherein said function switching circuit includes
a first electrode, a second electrode and a third
electrode,

15 wherein said first electrode is electrically
connected with said function switching terminal,

wherein said second electrode is at a supply
voltage,

wherein said third electrode is at ground
20 potential, and

wherein the function of said semiconductor device
is switched by making on breaking the connection
between said first electrode and said second electrode
or said third electrode.

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33. A memory module according to claim 32,
wherein said word structure switching circuit
includes a fourth electrode, a fifth electrode and a
sixth electrode,

5 wherein said fourth electrode is electrically
connected with said word structure switching terminal,
wherein said fifth electrode is at a supply
voltage,

wherein said sixth electrode is at ground
10 potential, and

wherein the word structure of said semiconductor
device is switched by making or breaking the
connection between said fourth electrode and said
fifth electrode or said sixth electrode.

15

34. A memory module according to claim 33,
wherein the function of said semiconductor device
to be switched by said function switching circuit
includes a reading mode.

20

35. A memory module according to claim 33,
wherein the function of said semiconductor device
to be switched by said function switching circuit
includes a refresh cycle.

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36. A memory module according to claim 33, wherein
the electrical connection between the first electrode
and the second electrode or the third electrode of
said function switching circuit is made through a
5 conducting element.

37. A memory module according to claim 36, wherein
the electrical connection between the fourth electrode
and the fifth electrode or the sixth electrode of said
10 word structure switching circuit is made through a
conducting element.

38. A memory module comprising:
a wiring substrate having interconnections;
15 a semiconductor device;
a function setting circuit; and
a word structure setting circuit,
wherein said semiconductor device includes
function switching terminals for selecting a function
20 and mounted on said wiring substrate, and word
structure switching terminals for selecting a word
structure,

wherein said function setting circuit is
connected with the function switching terminals of
25 said semiconductor device and is arranged on said

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wiring substrate, and

wherein said word structure setting circuit is
electrically connected with said word structure
switching terminals and arranged on said wiring
5 substrate.

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ABSTRACT OF THE DISCLOSURE

A memory module MM, in which a module wiring substrate 5 is equipped with function switching means KK1 and KK2 for arbitrarily switching function switching signals to be inputted to function switching pins FP0 and FP1 of memories 1. By these function switching means KK1 and KK2, moreover, the function switching signals are arbitrarily switched from any of no connection, a supply voltage Vcc and a ground potential Vss. These signals are inputted altogether to all the mounted memories 1 to switch and arbitrarily set functions including reading modes and refresh cycles.

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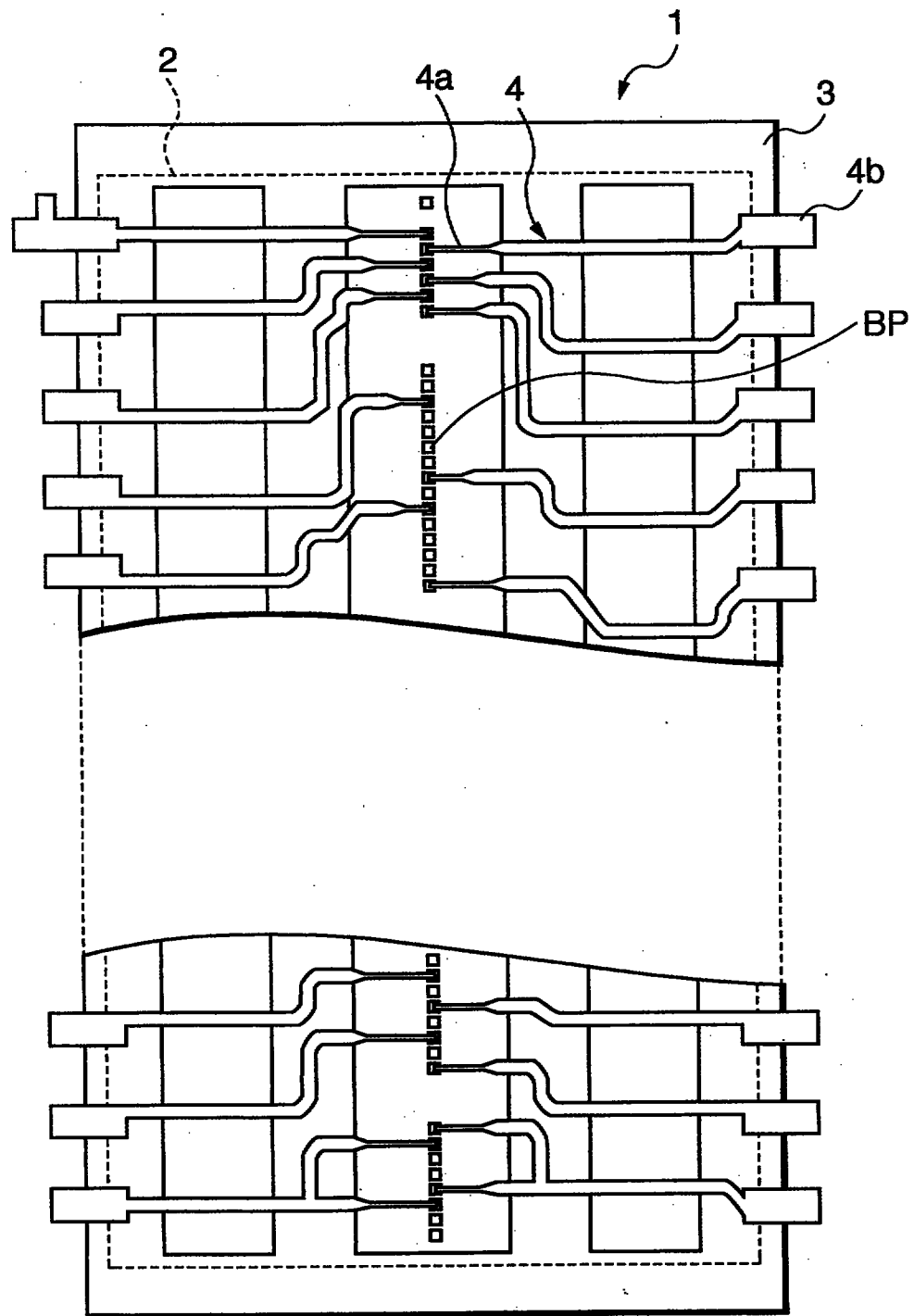
FIG. 1

FIG. 2

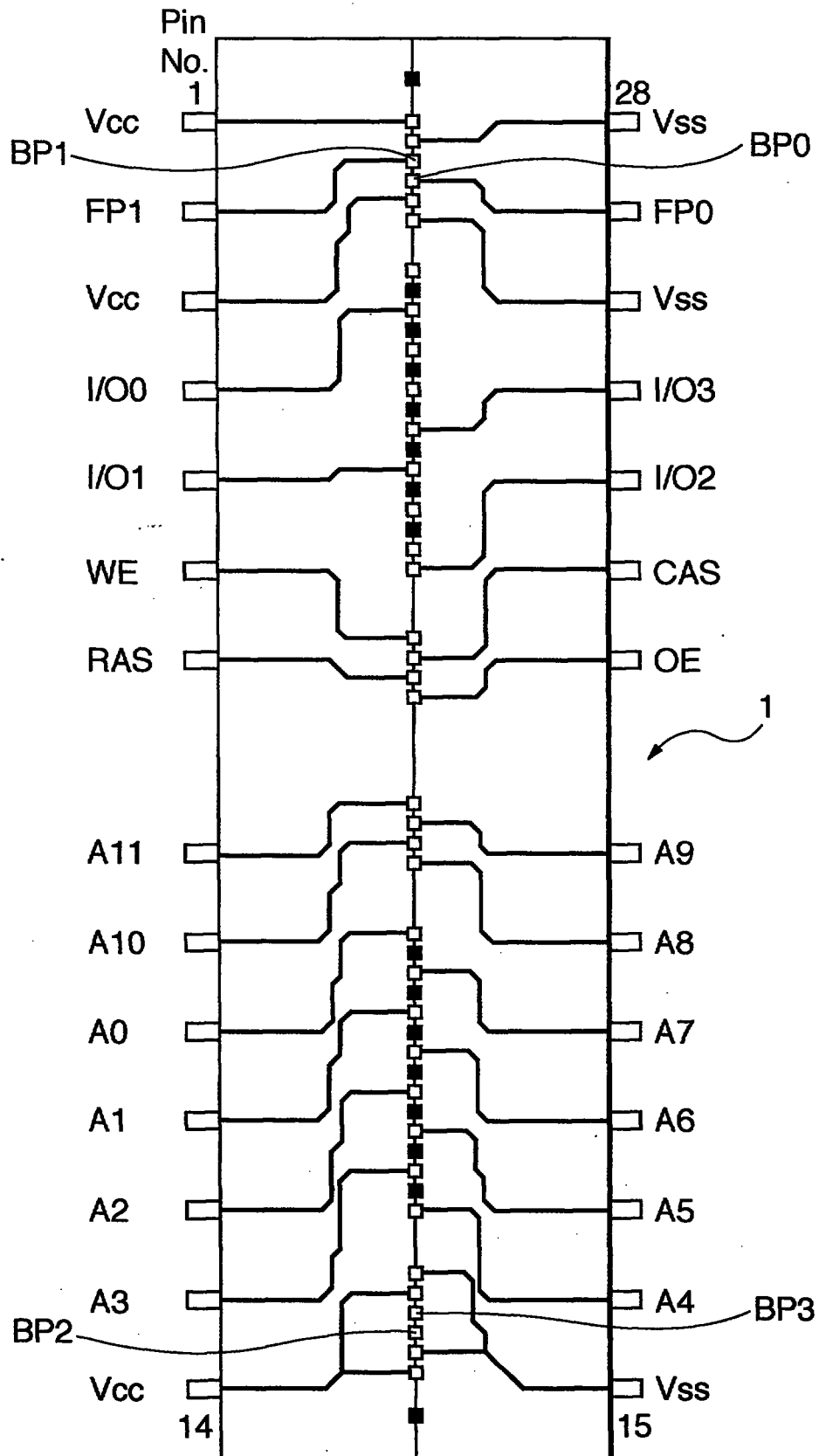


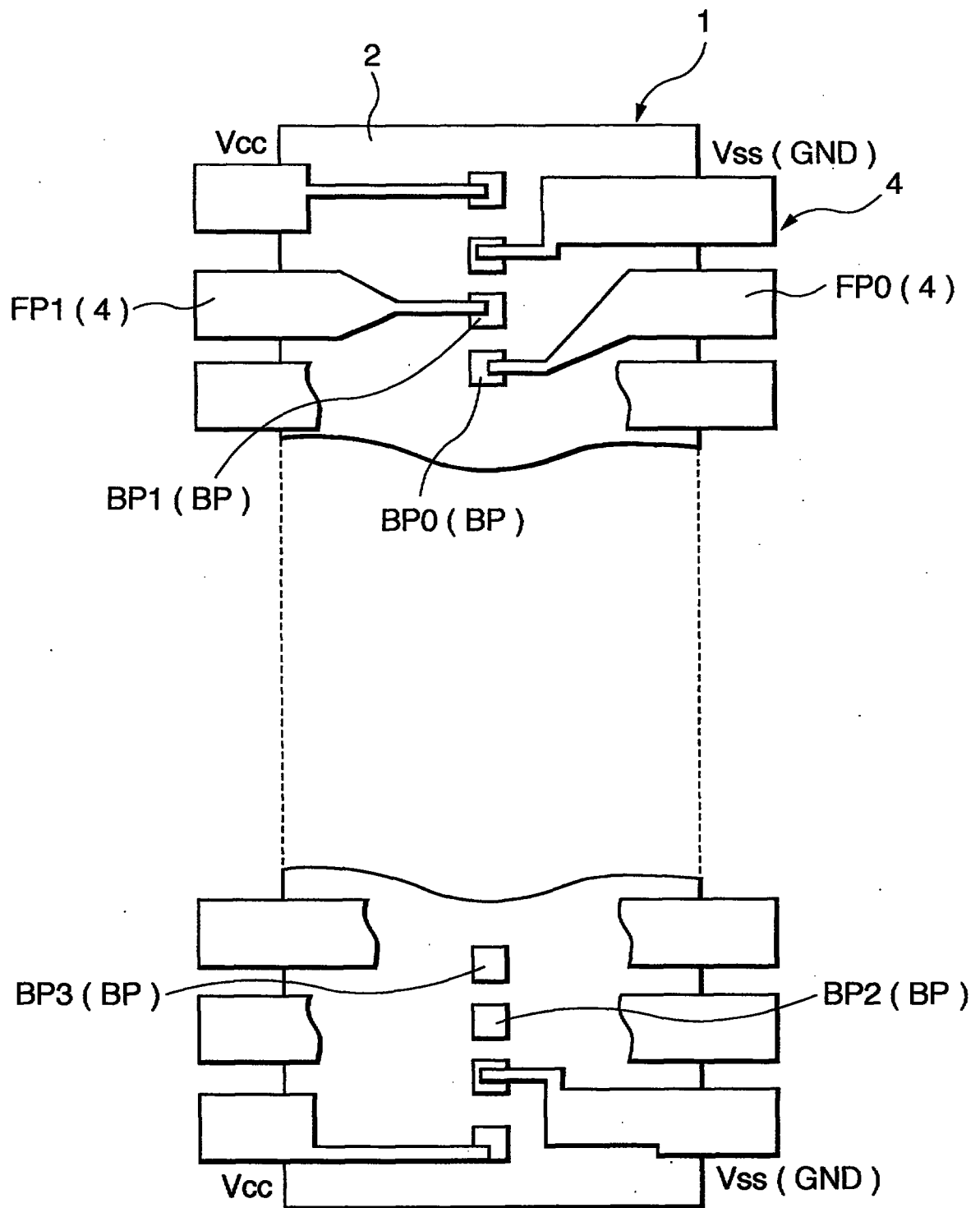
FIG. 3

FIG. 4

INPUT VOLTAGE				MODE
FP0	FP1	FP2	FP3	
OPEN	OPEN	V _{ss}	OPEN	X 1/4K cycle refresh / FAST PAGE
V _{ss}	OPEN	V _{ss}	OPEN	X 1/4K cycle refresh / EDO
OPEN	V _{cc}	OPEN	OPEN	X 4/2K cycle refresh / FAST PAGE
V _{ss}	V _{cc}	OPEN	OPEN	X 4/2K cycle refresh / EDO
OPEN	OPEN	OPEN	OPEN	X 4/4K cycle refresh / FAST PAGE
V _{ss}	OPEN	OPEN	OPEN	X 4/4K cycle refresh / EDO
OPEN	V _{cc}	OPEN	V _{cc}	X 8/2K cycle refresh / FAST PAGE
V _{ss}	V _{cc}	OPEN	V _{cc}	X 8/2K cycle refresh / EDO
OPEN	OPEN	OPEN	V _{cc}	X 8/4K cycle refresh / FAST PAGE
V _{ss}	OPEN	OPEN	V _{cc}	X 8/4K cycle refresh / EDO

FIG. 5

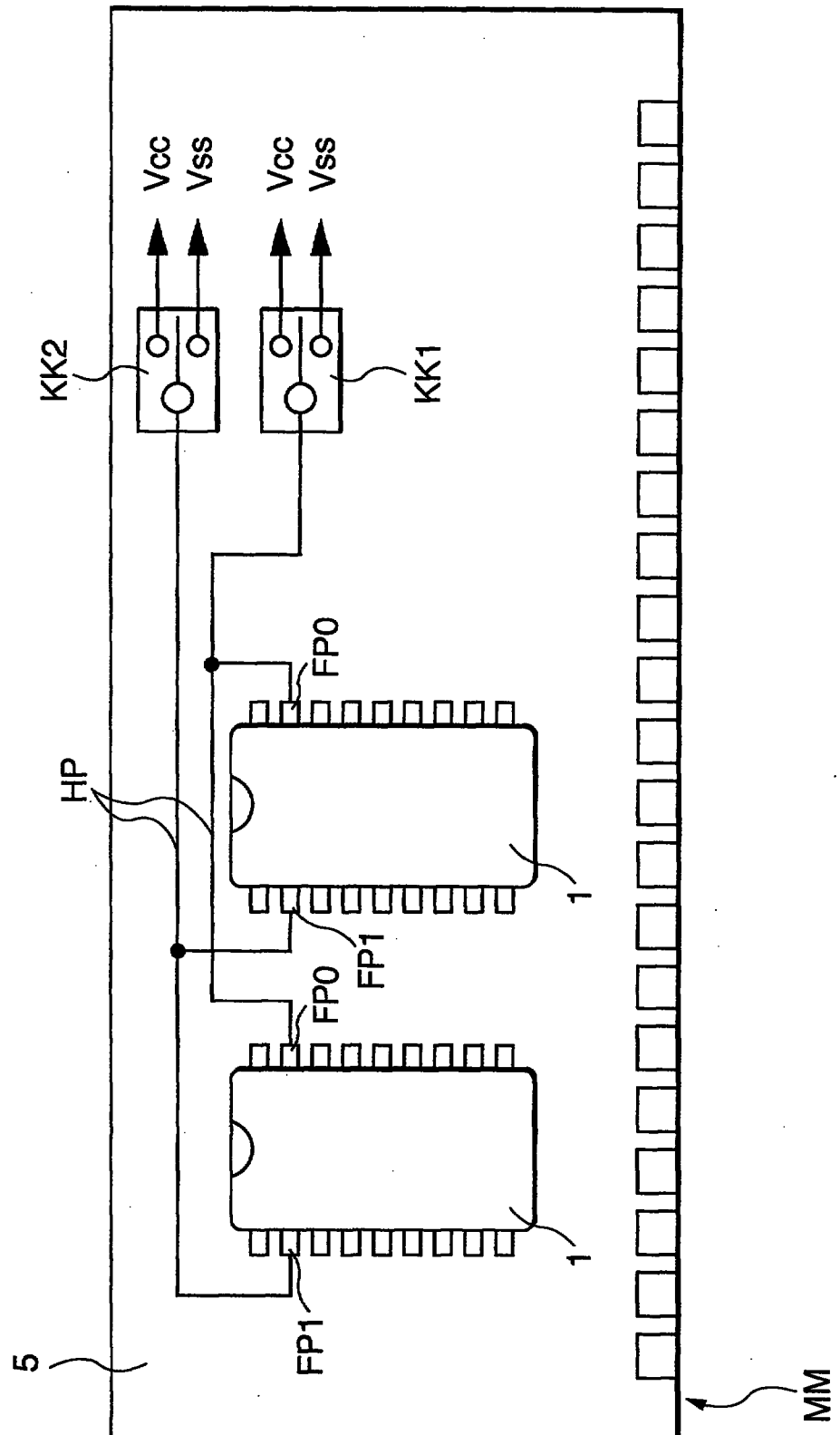


FIG. 6

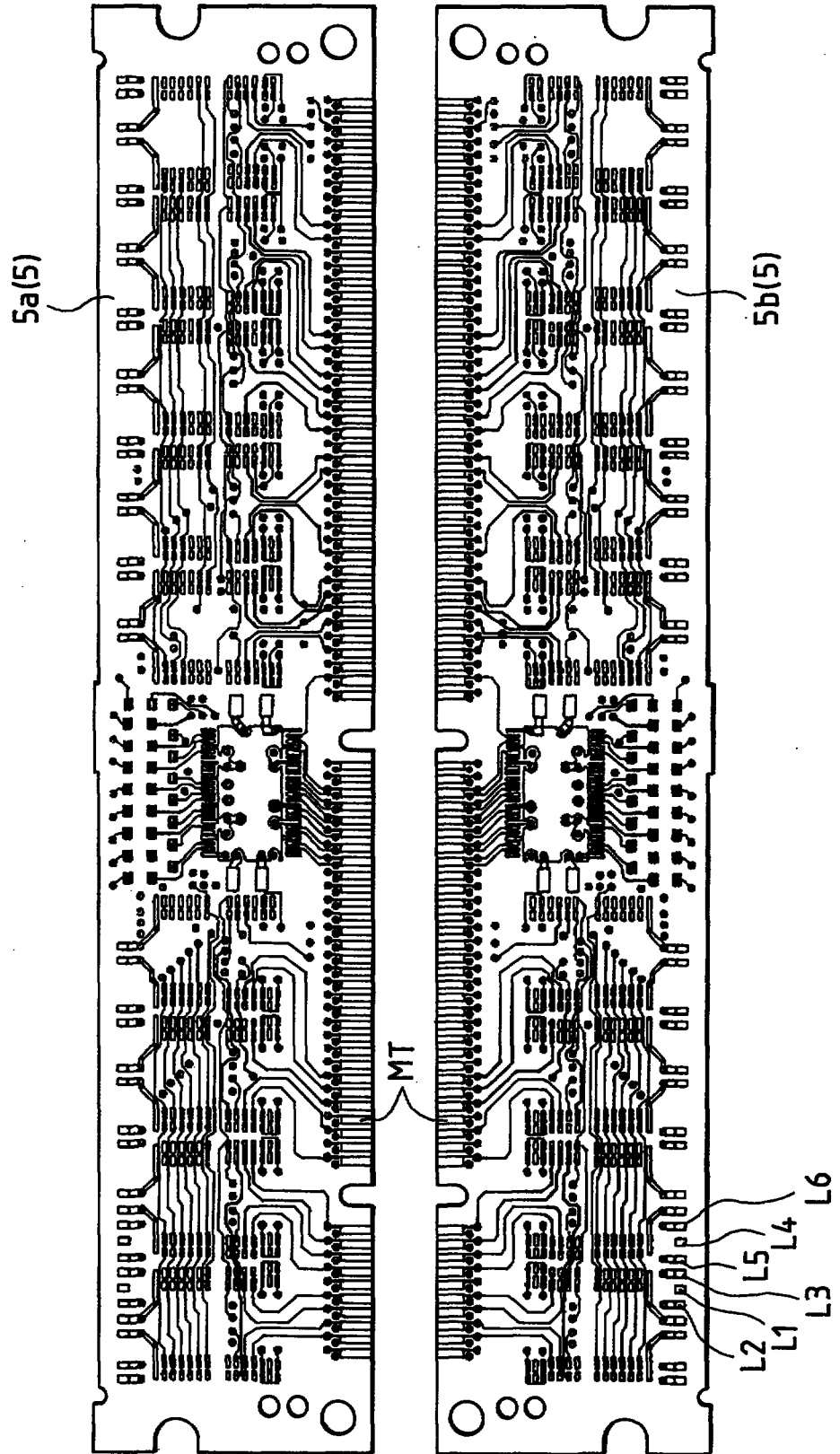


FIG. 7

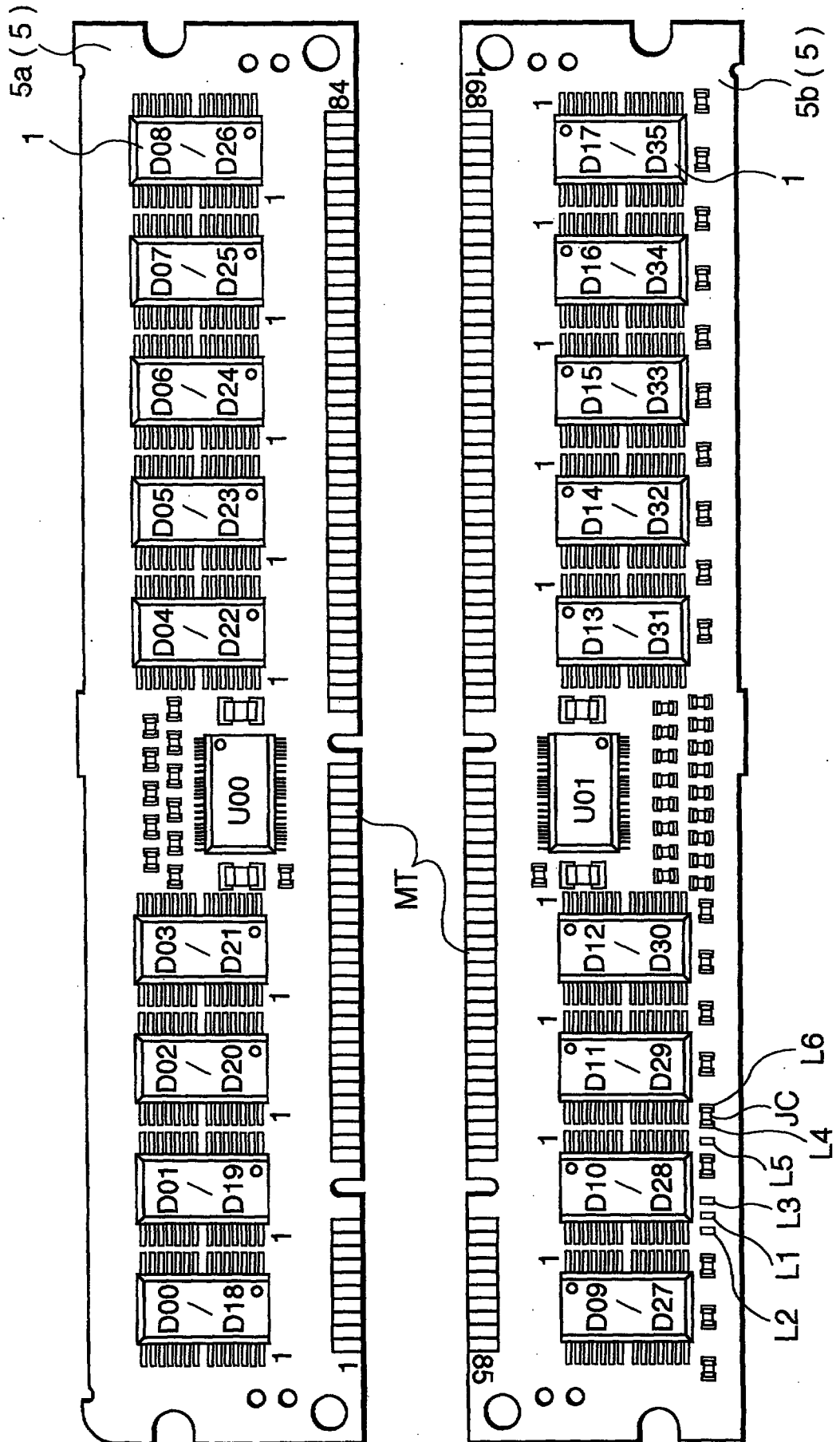


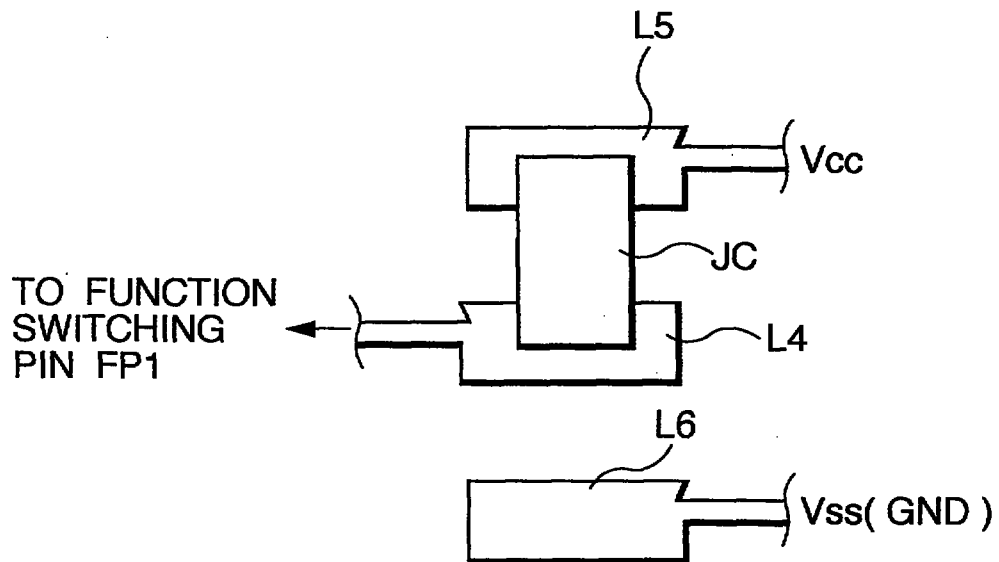
FIG. 8

FIG. 9

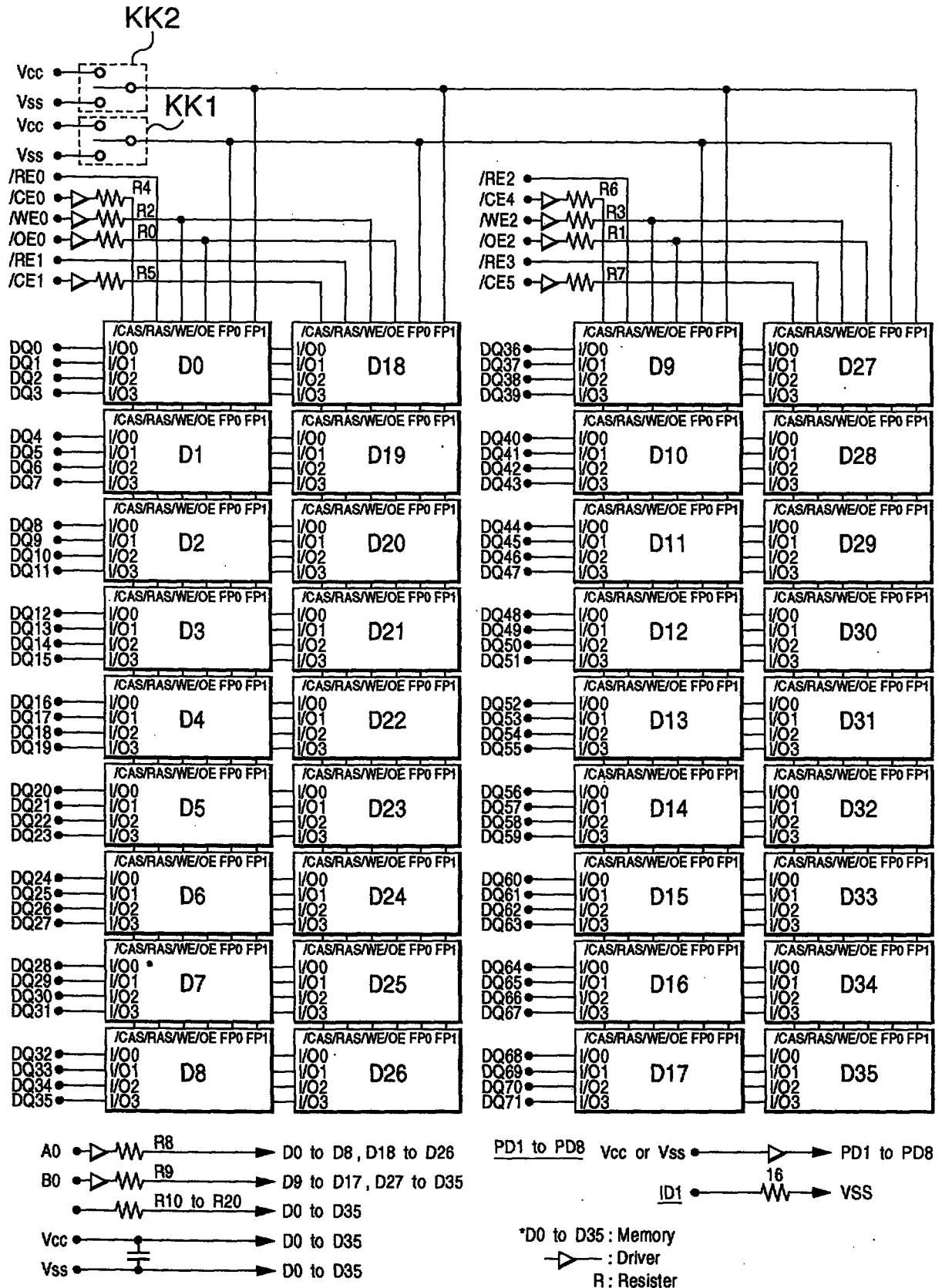


FIG. 10

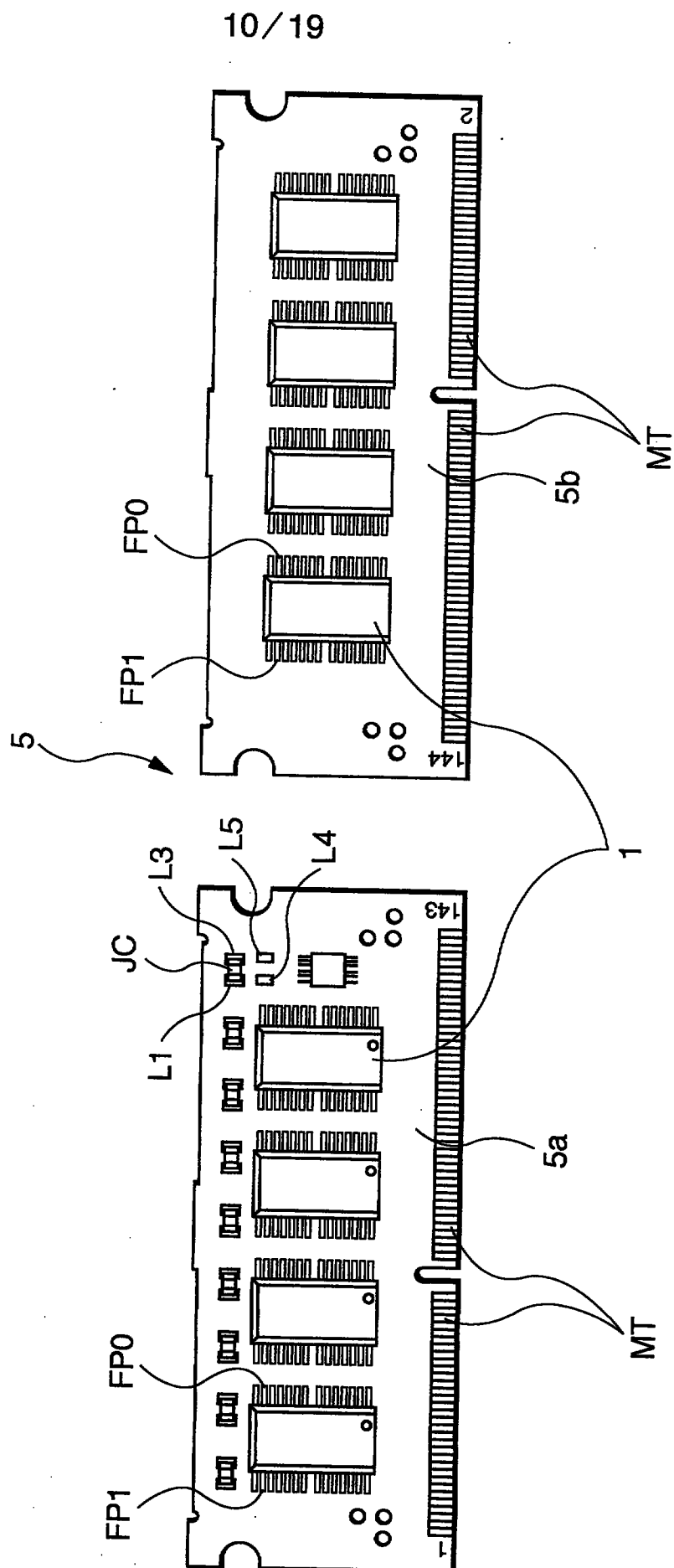


FIG. 11A

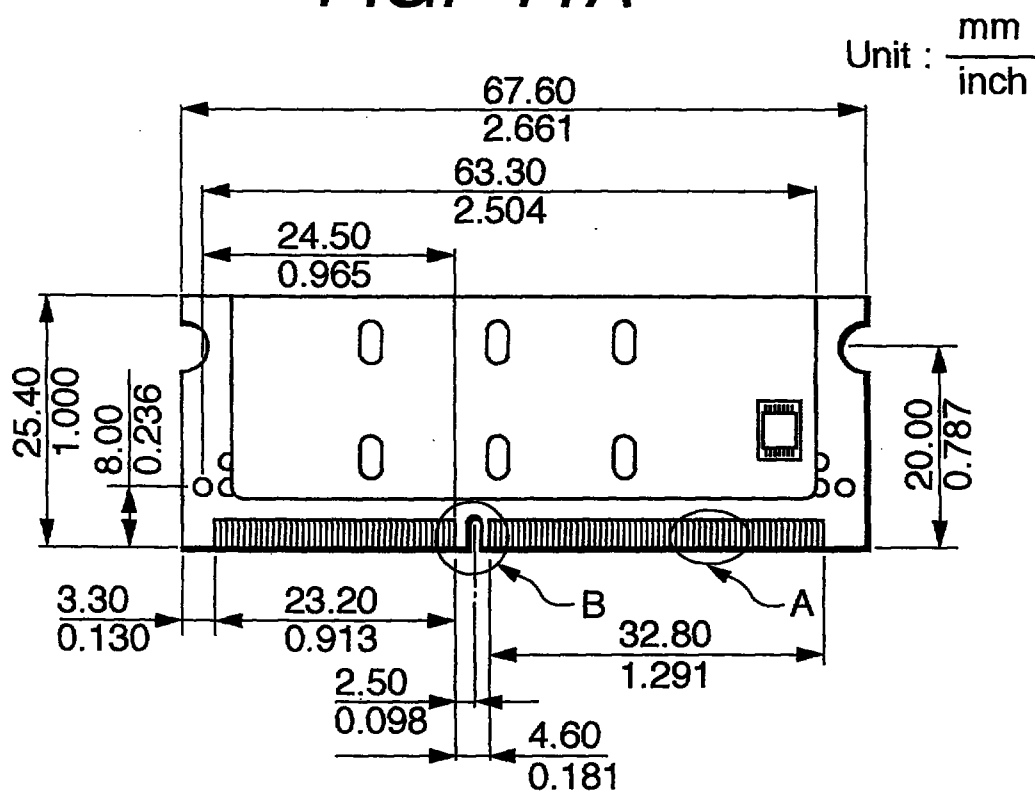


FIG. 11B

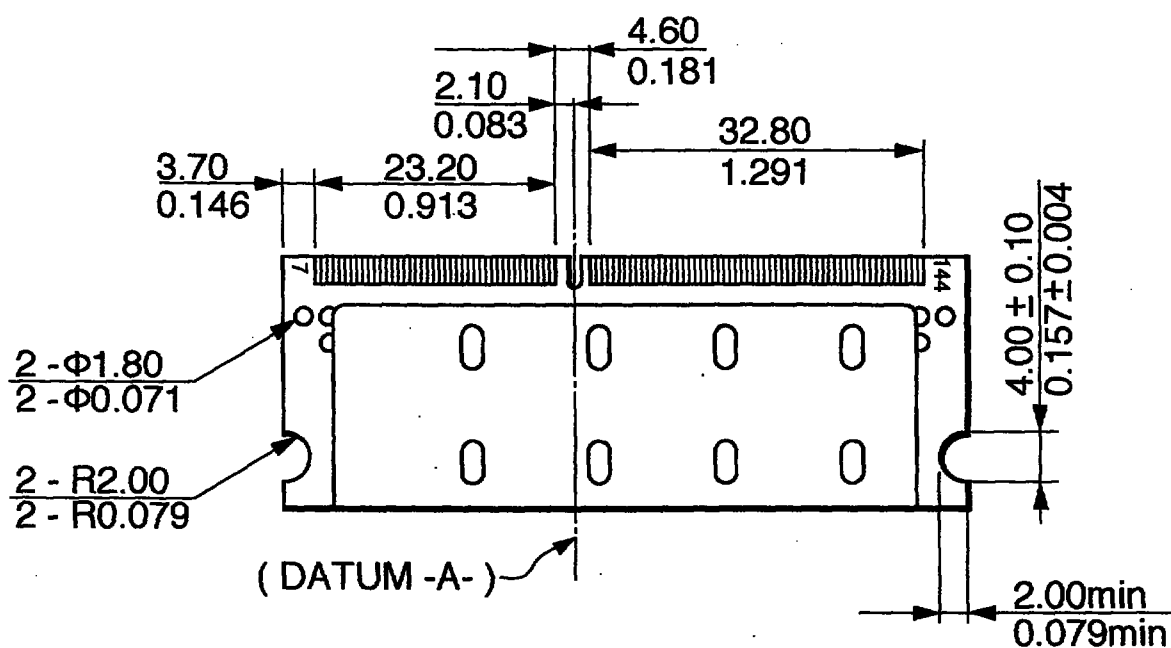


FIG. 11C

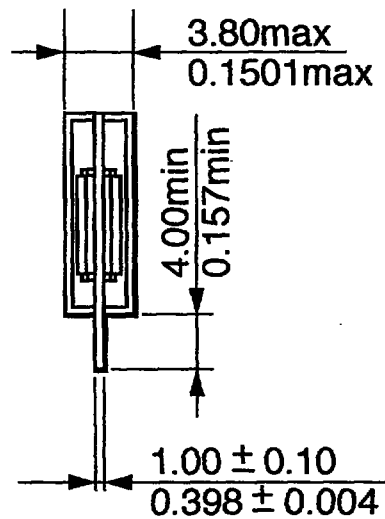


FIG. 11D

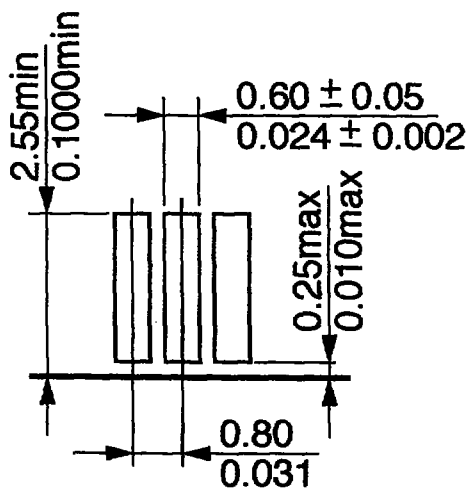


FIG. 11E

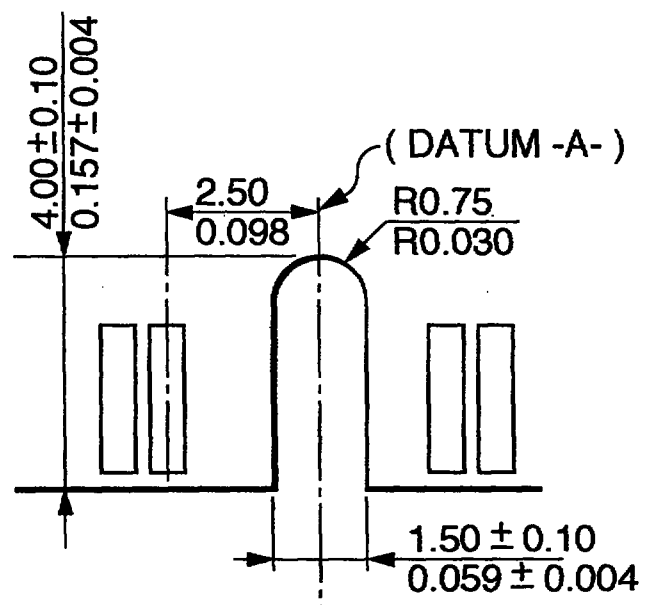


FIG. 12

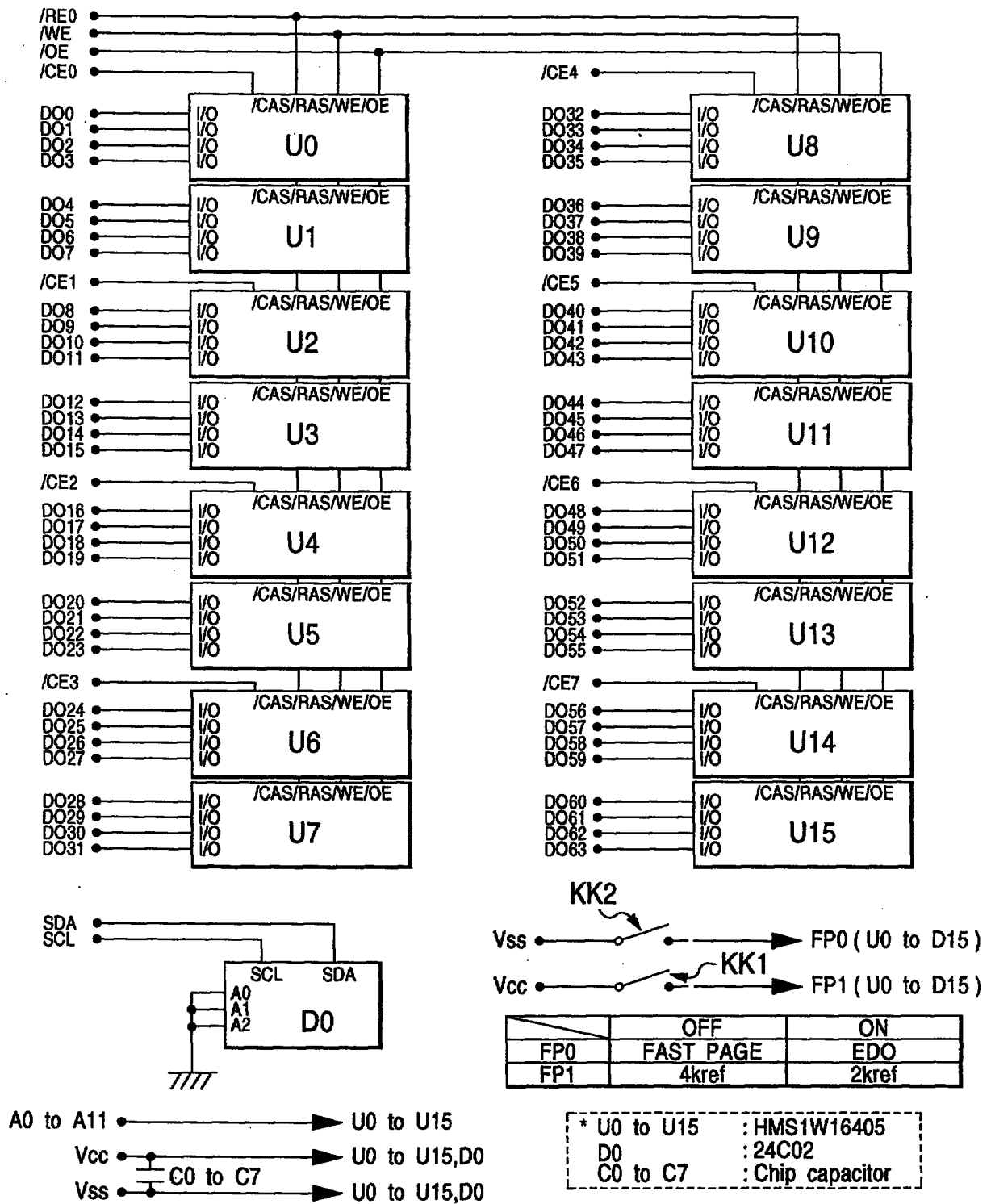


FIG. 13

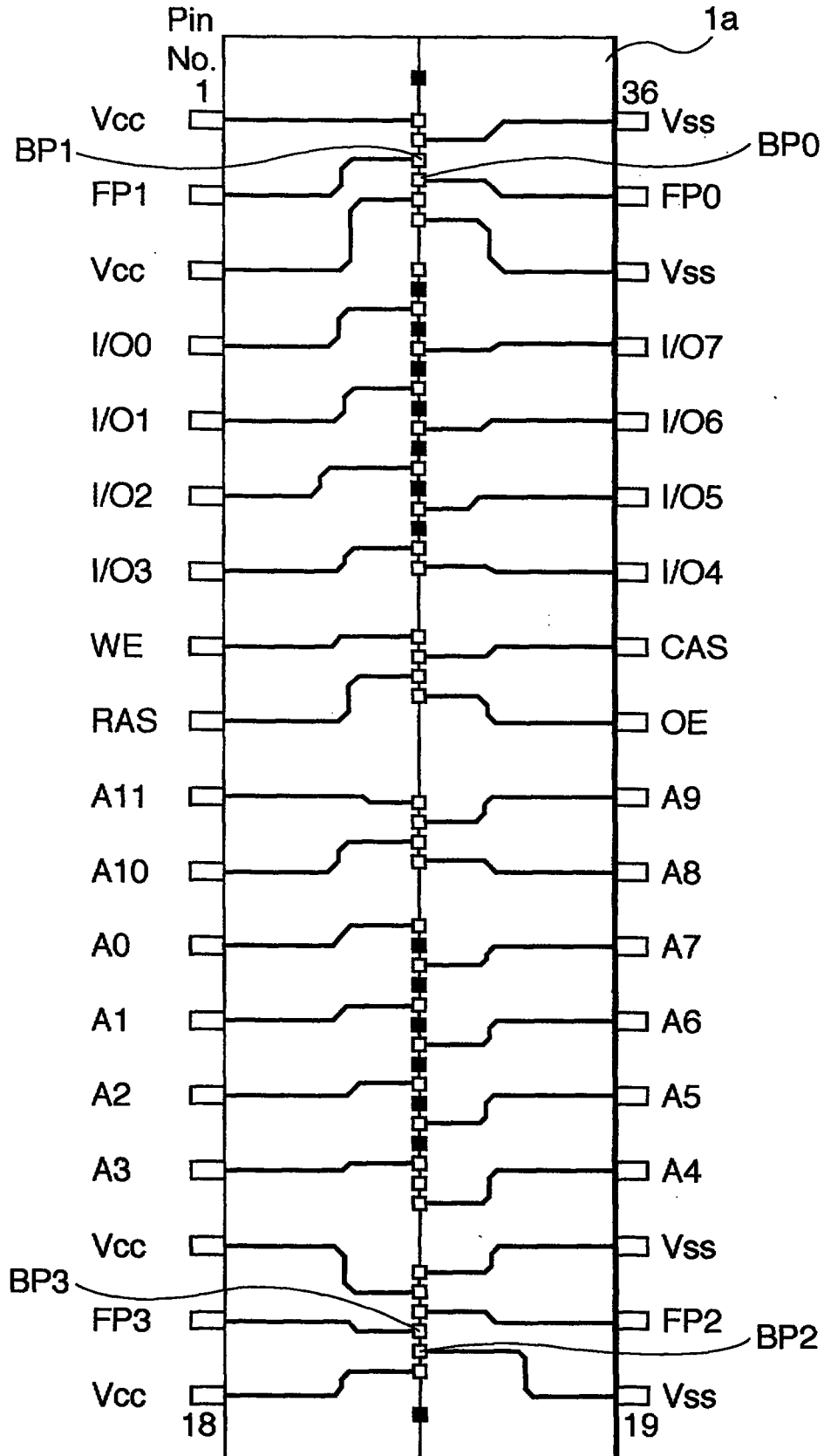


FIG. 14

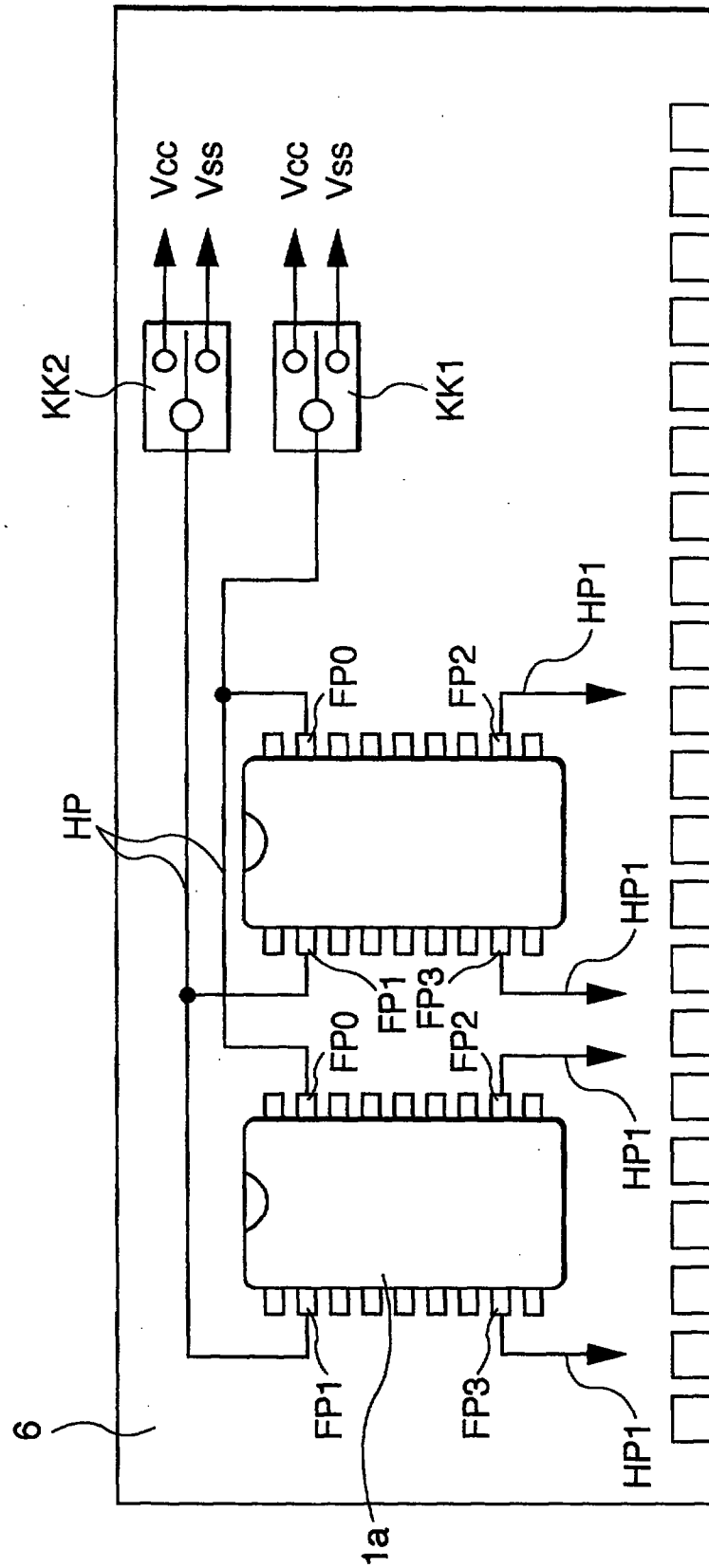


FIG. 15

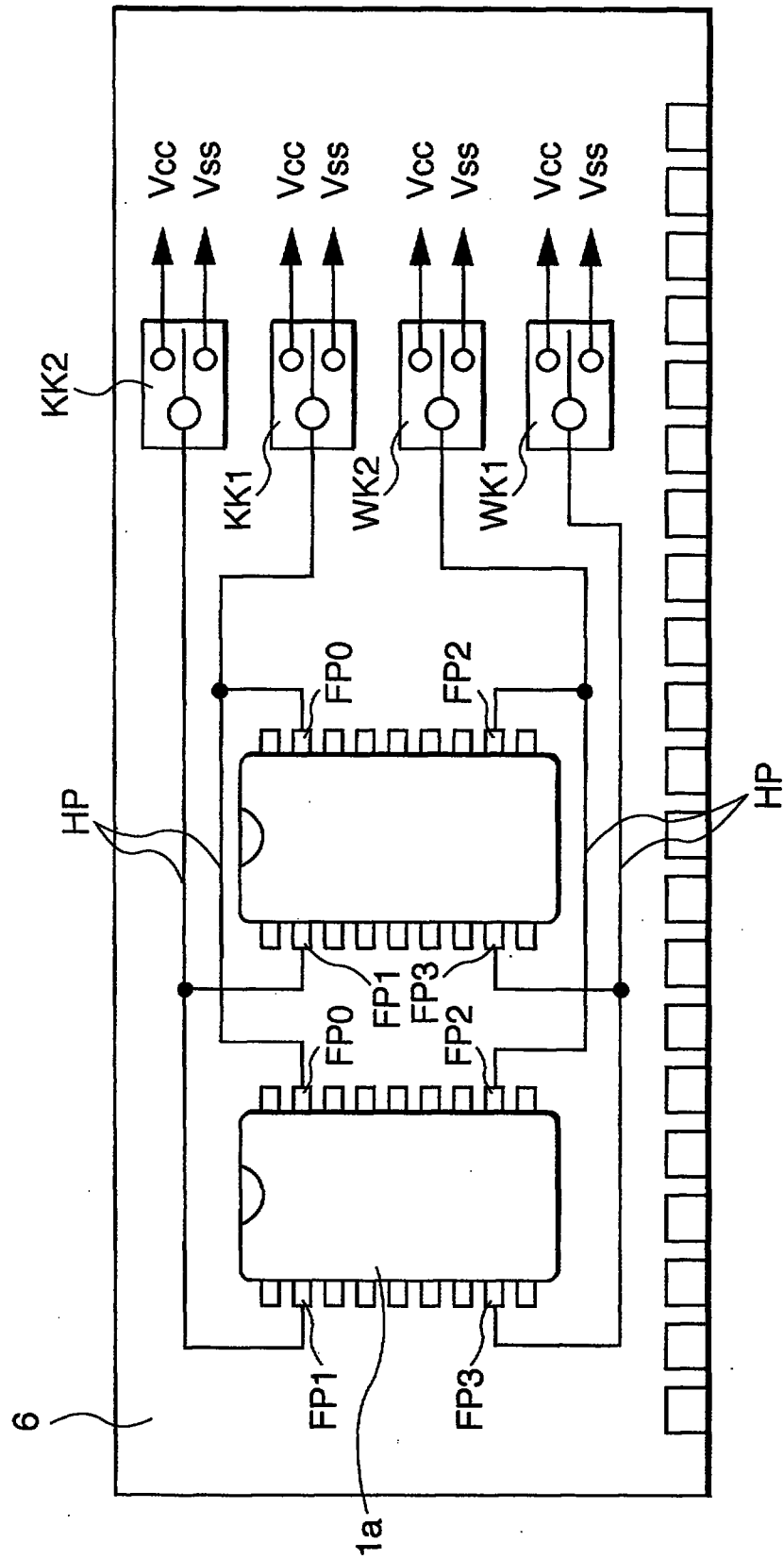


FIG. 16

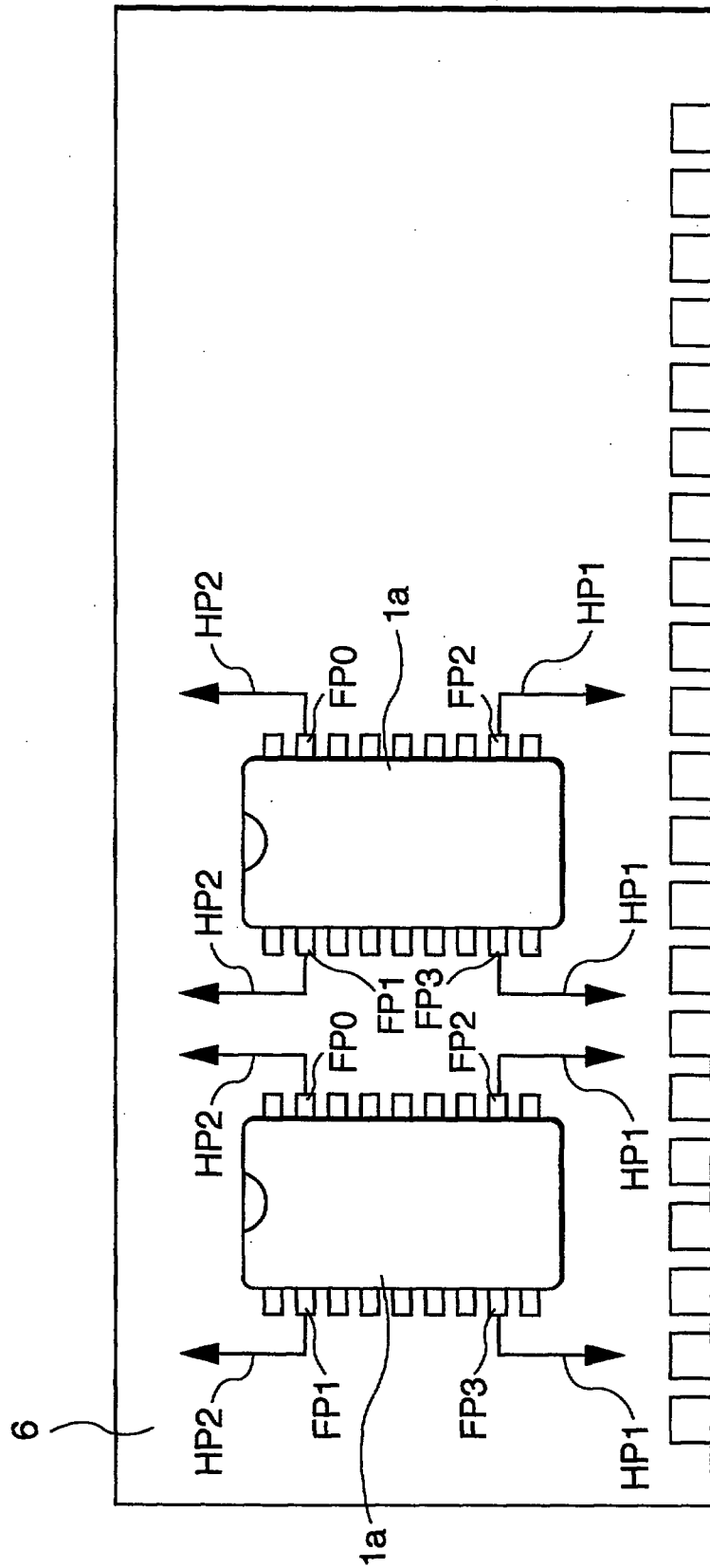


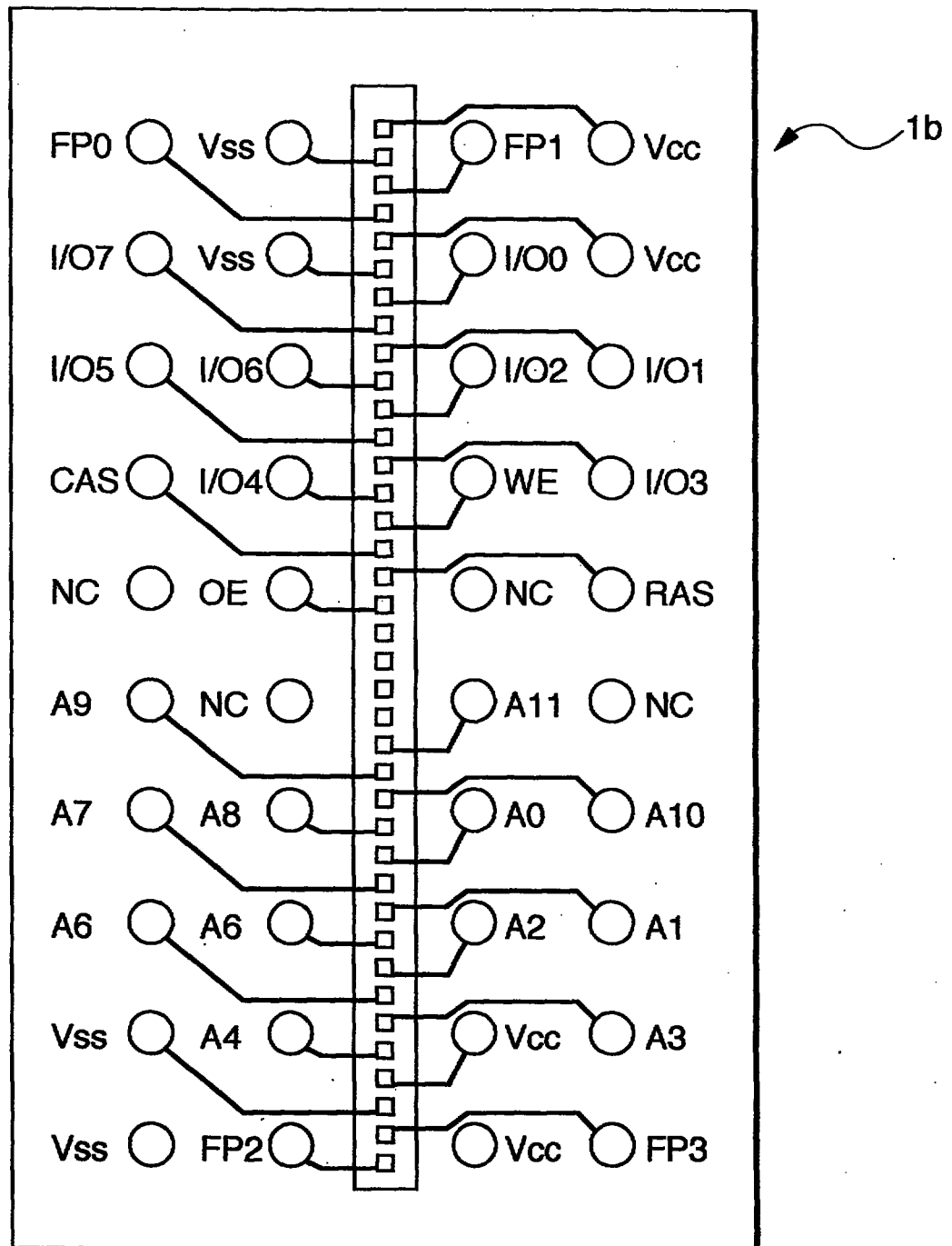
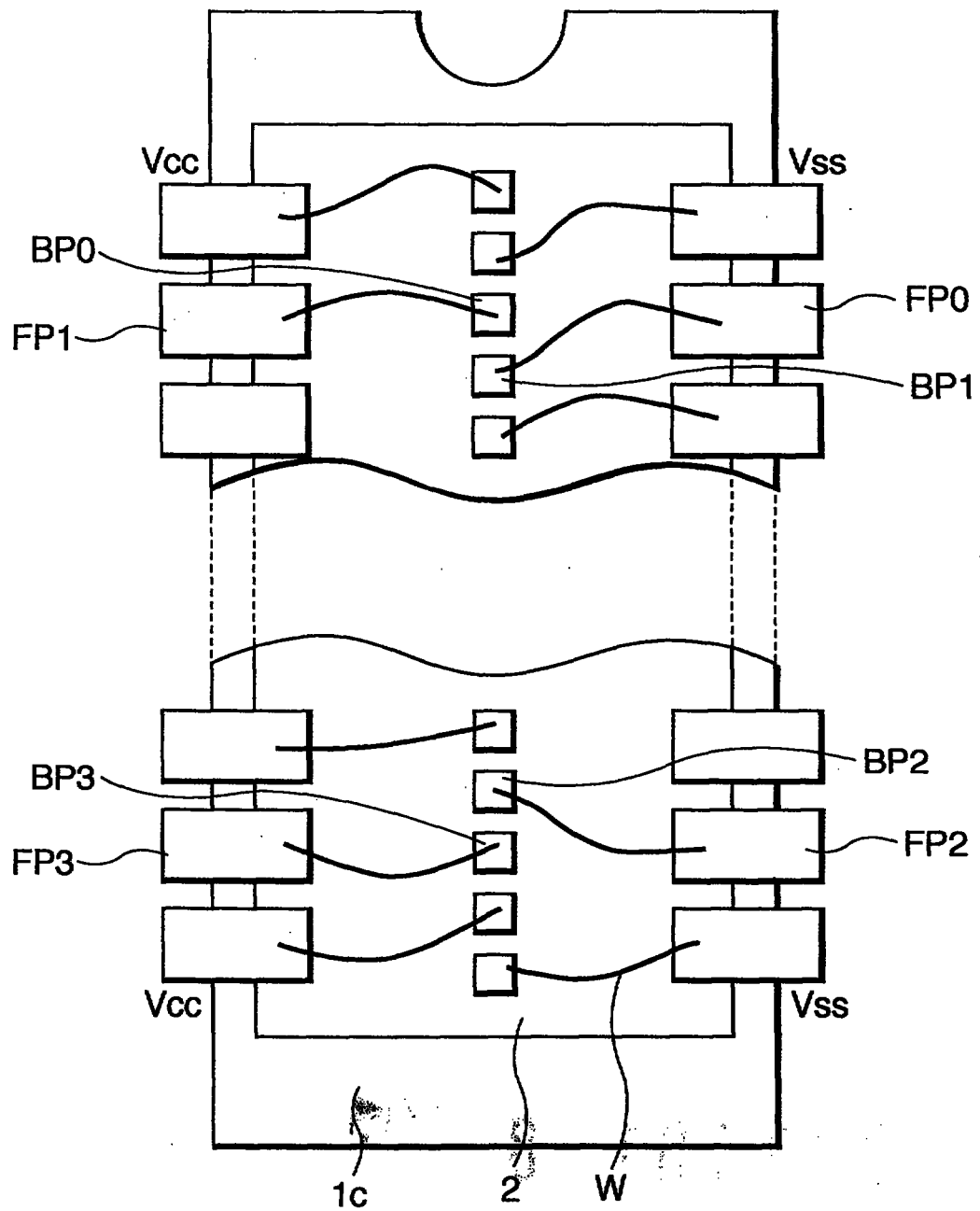
FIG. 17

FIG. 18



S P E C I F I C A T I O N

TITLE OF THE INVENTION

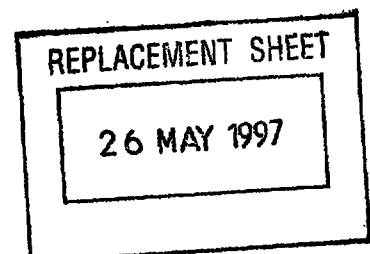
5 Semiconductor Device and Process for
 Manufacturing the Same

BACKGROUND OF THE INVENTION

 The present invention relates to a semiconductor
10 device and a process for manufacturing it and, more
 particularly, to a technique which is effective if
 applied for switching the functions and word
 structures of a memory module including a plurality of
 semiconductor devices.

15 According to our investigations, the memory
 module to be used as an extended memory in a personal
 computer or a work station is constructed by mounting
 on a module wiring substrate a memory or the DRAM
 (dynamic random access memory) semiconductor device,
20 as made of the SOJ (small outline package) type resin-
 sealed package, for example.

 In order that the memory module may have
 specifications conforming to the device to be used,
 there is mounted on the aforementioned module wiring
25 substrate the memory in which the functions are

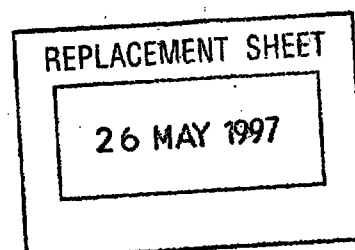


switched in the refresh cycle such as a refreshing operation cycle or a reading mode such as FAST PAGE or EDO (extended data out).

5 The switching of these functions of the memory is executed by connecting a predetermined electrode in a semiconductor chip through a bonding wire with a supply voltage V_{cc} or a ground potential V_{ss} or no connection terminal (NC) in the bonding step for packaging.

10 As another method for switching the aforementioned memory functions, moreover, there is known either the memory for selecting a predetermined reading mode in dependence upon a predetermined signal fed from the outside of the memory, as disclosed in
15 Japanese Patent Laid-Open No. 75494/1984, or the memory for designating a bit length mode programmably on the basis of a predetermined signal, as disclosed in Japanese Patent Laid-Open No. 59682/1986. On the other hand, the memory module is disclosed in Japanese
20 Patent Laid-Open No. 334112/1994.

Incidentally, the memory extended system of this kind is disclosed in detail, for example, on pp. 114 to 126 of "Semiconductor MOS Memory and Its Use", as issued on August 30, 1990 by Nikkan Kogyo Shinbunsha
25 and edited by Yasoji Suzuki. This publication



describes the circuit construction and operations of a memory extending DRAM board.

SUMMARY OF THE INVENTION

5 Incidentally, it has been found by us that the aforementioned memory module has the following problem.

 The memory, as used in a memory module to be used as the extended memory of a personal computer or the like, has a variety of function switching operations. However, the memory module, as mounted as a complete product on the module wiring substrate, cannot switch the functions. Thus, the memory modules are assembled for the individual functions, and there arises a
10 problem that the degree of freedom for the production is degraded.
15

 An object of the present invention is to provide a memory module, in which the individual functions and word structures can be arbitrarily switched outside of
20 the package, and a process for manufacturing the memory module.

 The aforementioned and other objects and novel features of the present invention will become apparent from the following description to be made with
25 reference to the accompanying drawings.

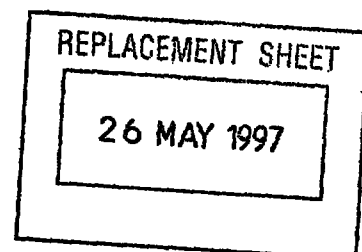
REPLACEMENT SHEET

26 MAY 1997

The summaries of the representatives of the invention to be disclosed herein will be briefly described in the following.

A memory module according to the present invention comprises at least one semiconductor device including function switching external terminals for selecting a function in dependence upon the state of a function switching signal; and a printed-wiring substrate with the semiconductor device mounted thereon and including function switching means for selecting an arbitrary function switching signal to be inputted to the function switching external terminals.

According to the present invention, moreover, the function switching means includes a first node formed on the printed-wiring substrate and electrically connected with the function switching external terminal of the semiconductor device, as mounted on the printed-wiring substrate; a second node formed on the printed-wiring substrate and connected with a supply voltage; and a third node formed on the printed-wiring substrate and connected with a reference voltage, and the function switching means is means for switching the function switching signals altogether, as inputted to the function switching external terminals, with or without conducting means



provided between the first node and the second node or the third node.

According to the present invention, moreover, the function switching means is arranged at or in the vicinity of a corner portion of the printed-wiring substrate.

According to the present invention, moreover, the function of the semiconductor device to be switched by the function switching means includes a reading mode.

According to the present invention, moreover, the function of the semiconductor device to be switched by the function switching means includes a refresh cycle.

According to the present invention, moreover, the function of the semiconductor device to be switched by the function switching means includes a reading mode and a refresh cycle.

According to the present invention, moreover, the semiconductor device further includes word structure switching external terminals for selecting a word structure in dependence upon the state of a word structure switching signal, and the printed-wiring substrate further includes a word structure setting circuit for inputting a preset word structure switching signal to the word structure switching external terminals.

REPLACEMENT SHEET

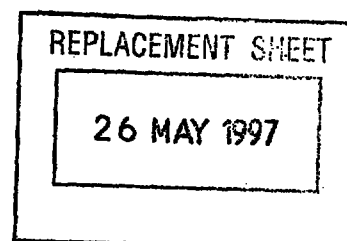
26 MAY 1997

According to the present invention, a memory module comprises at least one semiconductor device including word structure switching external terminals for selecting a word structure in dependence upon the state of a word structure switching signal; and a dedicated printed-wiring substrate with the semiconductor device mounted thereon and including dedicated lines corresponding to the switched word structure of the semiconductor device.

10 According to the present invention, moreover, the memory module further comprises word structure switching means mounted on the dedicated printed-wiring substrate for selecting an arbitrary word structure switching signal to be inputted to the word structure switching external terminals.

15 According to the present invention, moreover, the word structure switching means includes a word structure setting circuit wired on the dedicated printed-wiring substrate and adapted to be switched to a predetermined word structure by mounting the semiconductor device so that a predetermined word structure switching signal is inputted to the word structure switching external terminals.

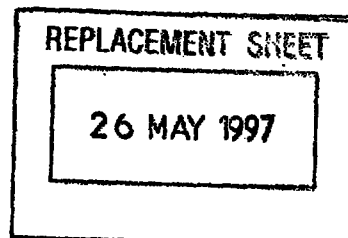
25 According to the present invention, moreover, the word structure switching means includes a fourth node



formed on the dedicated printed-wiring substrate and electrically connected with the word structure switching external terminal of the semiconductor device, as mounted on the dedicated printed-wiring substrate; a fifth node formed on the dedicated printed-wiring substrate and connected with a supply voltage; and a sixth node formed on the dedicated printed-wiring substrate and connected with a reference voltage, and the word structure switching means is means for switching the word structure switching signals altogether, as inputted to the word structure switching external terminals, with or without conducting means provided between the fourth node and the fifth node or the sixth node.

According to the present invention, moreover, the semiconductor device further includes function switching external terminals for selecting a function in dependence upon the state of a function switching signal, and the dedicated printed-wiring substrate further includes function switching means for selecting an arbitrary function switching signal to be inputted to the function switching external terminals.

According to the present invention, moreover, the function switching means includes a first node (or electrode) formed on the dedicated printed-wiring



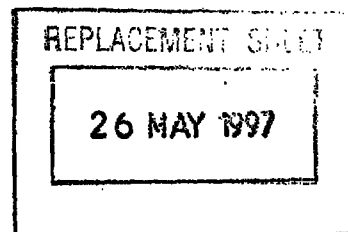
substrate and electrically connected with the function
switching external terminal of the semiconductor
device, as mounted on the dedicated printed-wiring
substrate; a second node (or electrode) formed on the
5 dedicated printed-wiring substrate and connected with
a supply voltage; and a third node (or electrode)
formed on the dedicated printed-wiring substrate and
connected with a reference voltage (or ground
potential), and the function switching means is means
10 for switching the function switching signals
altogether, as inputted to the function switching
external terminals, with or without conducting means
provided between the first node and the second node or
the third node.

15 According to the present invention, moreover, the
function of the semiconductor device to be switched by
the function switching means includes a reading mode.

 According to the present invention, moreover, the
function of the semiconductor device to be switched by
20 the function switching means includes a refresh cycle.

 According to the present invention, moreover, the
function of the semiconductor device to be switched by
the function switching means includes a reading mode
and a refresh cycle.

25 According to the present invention, moreover, the



function switching means includes a function setting
circuit wired on the dedicated printed-wiring
substrate and adapted to be switched to a
predetermined function by mounting the semiconductor
5 device so that a predetermined function switching
signal is inputted to the function switching external
terminals.

According to the present invention, a process for
manufacturing a memory module comprises the step of
10 preparing a semiconductor device for selecting a
predetermined word structure on the basis of a word
structure switching signal, as inputted to word
structure switching external terminals, and a
plurality of kinds of dedicated printed-wiring
15 substrates corresponding to a plurality of word
structures, and selecting one of the dedicated
printed-wiring substrates, as corresponding to a
demanded word structure of the semiconductor device,
from the plurality of kinds of dedicated printed-wiring
20 substrates; and the step of mounting the semiconductor
device on the selected one of the dedicated printed-
wiring substrates.

According to the present invention, moreover, a
process for manufacturing a memory module comprises
25 the step of preparing a semiconductor device for

REPLACEMENT SHEET

26 MAY 1997

switching a word structure on the basis of a word structure switching signal, as inputted to word structure switching external terminals, and for selecting a function on the basis of a function switching signal, as inputted to function switching external terminals, function switching means for selecting an arbitrary function switching signal, as inputted to the function switching external terminals, with or without conducting means provided, and a plurality of kinds of dedicated printed-wiring substrates corresponding to a plurality of word structures, and selecting one of the dedicated printed-wiring substrates, as corresponding to a demanded word structure of the semiconductor device, from the plurality of kinds of dedicated printed-wiring substrates; the step of mounting the semiconductor device on the selected one of the dedicated printed-wiring substrates; and the step of switching an arbitrary function selectively, with or without the conducting means provided.

According to the present invention, moreover, a process for manufacturing a memory module comprises the step of preparing a semiconductor device for selecting a predetermined word structure on the basis of a word structure switching signal, as inputted to

REPLACEMENT SHEET

26 MAY 1997

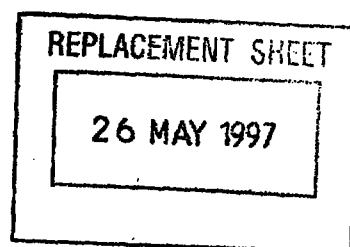
word structure switching external terminals, and for
switching a predetermined function on the basis of a
function switching signal, as inputted to function
switching external terminals, and a plurality of kinds
5 of dedicated printed-wiring substrates corresponding
to the switching operations of a plurality of word
structures and a plurality of functions, and selecting
one of the dedicated printed-wiring substrates, as
corresponding to a demanded word structure of the
10 semiconductor device and the switching operation of
the function, from the plurality of kinds of dedicated
printed-wiring substrates; and the step of mounting
the semiconductor device on the selected one of the
dedicated printed-wiring substrates.

15 As described above, it is possible to improve the
efficiency in the product development of the
semiconductor device and to facilitate the product
management thereby to reduce the cost.

20 BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is an explanatory diagram showing a
construction of an essential portion of a memory
according to Mode 1 of Embodiment of the present
invention;

25 Fig. 2 is a pin arrangement diagram of the memory



according to Mode 1 of Embodiment of the present invention;

Fig. 3 is an explanatory diagram showing internal connections of the memory according to Mode 1 of Embodiment of the present invention;

Fig. 4 is an explanatory table showing the mode switching operations of the memory according to Mode 1 of Embodiment of the present invention;

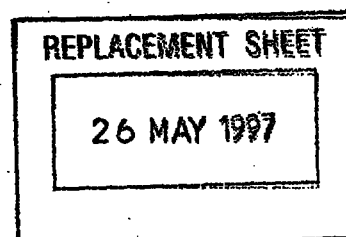
Fig. 5 is a connection diagram of one embodiment of a memory module, in which are mounted the memories according to the present invention;

Fig. 6 is a wiring diagram showing a module wiring substrate in which is mounted the memory according to Mode 1 of Embodiment of the present invention;

Fig. 7 is a mounting diagram of the module wiring substrate in which is mounted the memory according to Mode 1 of Embodiment of the present invention;

Fig. 8 is an explanatory diagram showing a mounting example of a jumper for switching the functions of the memory according to Mode 1 of Embodiment of the present invention;

Fig. 9 is a block diagram showing the memory module according to Mode 1 of Embodiment of the present invention;



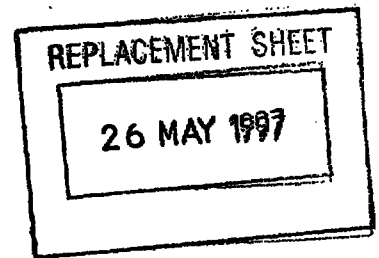


Fig. 10 is a mounting diagram showing the module mounting substrate in which is mounted a memory according to another mode of embodiment of the present invention;

5 Figs. 11A to 11E are standards diagrams of the module wiring substrate according to another mode of embodiment of the present invention;

Fig. 12 is a block diagram showing the memory module according to another mode of embodiment of the present invention;

Fig. 13 is a pin arrangement diagram of a memory according to Mode 2 of Embodiment of the present invention;

Fig. 14 is a connection diagram of another embodiment of the memory module in which are mounted memories according to the present invention;

Fig. 15 is a connection diagram of another embodiment of the memory module in which are mounted memories according to the present invention;

20 Fig. 16 is a connection diagram of another embodiment of the memory module in which are mounted memories according to the present invention;

Fig. 17 is a pin arrangement diagram showing a memory according to another mode of embodiment of the present invention; and

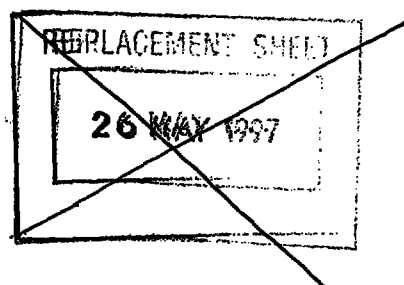


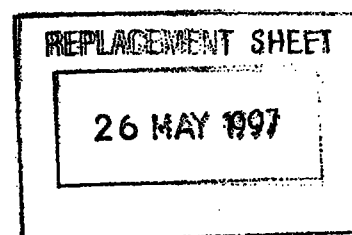
Fig. 18 is an explanatory diagram showing the internal connections of a memory according to another mode of embodiment of the present invention.

5 DESCRIPTION OF THE PREFERRED EMBODIMENTS

In the present Mode 1 of Embodiment, a memory 1, as made of a TCP (tape carrier package) type DRAM semiconductor device or a kind of surface mount package, has the bonding pads BP or electrodes which
10 are arranged at the central portion of a semiconductor chip 2.

On the other hand, the memory 1 is given such a structure that the aforementioned semiconductor chip 2 is mounted on the tape carriers which are prepared by
15 forming the wiring lines 4 of copper foil as leads repeatedly over the upper face of a film of polyimide.

Moreover, the bonding pads BP, as arranged on the semiconductor chip 2, are individually electrically connected with inner leads 4a, as formed in the tape
20 carriers, at the leading end portions of the wiring lines 4. Still moreover, the inner leads 4a are extended to form outer leads 4b to be electrically connected with external connection electrodes such as lands, as formed on the later-described module wiring
25 substrate.

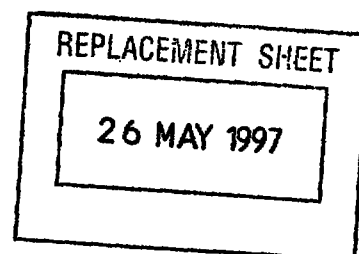


On the other hand, the semiconductor chip 2 and the inner leads 4a are sealed with an epoxy resin, for example, to form a package, and the individual leads, as protruding from the package, are bent generally in a crank shape.

Next, the memory 1 is constructed to include twenty eight pins in total, as shown in Fig. 2. Of these, the 2nd and 27th pins, as connected with bonding pads BP1 and BP0 for switching the functions, have outer leads acting as function switching pins (or function switching external terminals) FP1 and FP0.

On the other hand, the memory 1 is equipped with bonding pads BP3 and BP2 for switching the word structure so that the word structure is arbitrarily switched depending upon the states of signals to be inputted to the bonding pads BP3 and BP2.

In Fig. 2, moreover, there are provided data input/output pins IO0 to IO3, a pin WE for designating whether the access is to read or write, address input pins A0 to A11, pins RAS and CAS for row and column selecting signals, a pin OE for a signal to control the states of a data output signal and a data input/output signal at a reading time, a pin Vcc for a supply voltage Vcc, and a pin Vss for a ground potential (or earth potential) or the reference



potential.

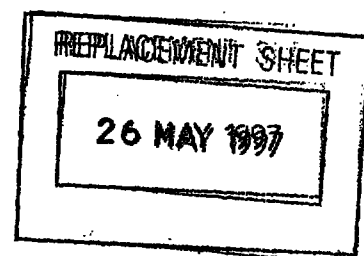
Next, the internal connection structure in the memory 1 will be specifically described with reference to Fig. 3.

5 First of all, the memory 1 is shown to have the arrangement of only: the function switching bonding pads BP1 and BP0 or the electrodes, as electrically connected with the function switching pins FP1 and FP0 of the 2nd and 27th pins, and the bonding pads BP3 and
10 BP2 for switching the word structure, of the bonding pads BP formed on the semiconductor chip 2; and the wiring lines 4 for the supply voltage Vcc of the 1st and 14th pins, and the wiring lines 4 for the ground potential of the 15th and 28th pins.

15 Here in the memory 1, the function means the reading mode which is constructed to include a refresh cycle or the cycle for a refreshing operation, and FAST PAGE and EDO.

As shown in Fig. 4, moreover, the memory 1 can
20 switch the refresh cycle, the reading modes of FAST PAGE AND EDO, and three kinds of word structures of 4 M x 1 bit, 1 M x 4 bits and 512 K x 8 bits.

On the other hand, these function switching operations in the memory 1 are executed by inputting
25 the supply voltage Vcc, the ground potential Vss or

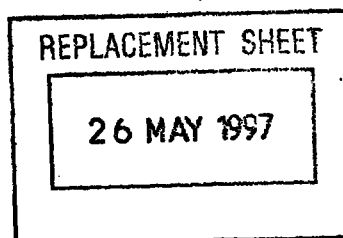


the function switching signal, as selected from the no connections, to the connection destinations of the function switching bonding pads BP1 and BP0, as arranged in the predetermined positions of the semiconductor chip 2 shown in Fig. 3, that is, the pins FP0 and FP1 for switching the functions of the 2nd and 27th pins, and by combining those function switching signals in the aforementioned manner, as shown in Fig. 4.

Moreover, the connection destinations of the word structure switching bonding pads BP3 and BP2 are predetermined by the wiring lines 4a, as formed on the tape carriers. In the memory 1 of the present Mode of Embodiment, as shown in Fig. 2, the bonding pads BP3 and BP2 have no connection.

In the word structure of the memory 1, therefore, the bonding pads BP3 and BP2 have no connection (as indicated by 'OPEN' in Fig. 4), as shown in Fig. 4, so that the word structure of 4 K x 4 bits is automatically selected.

On the other hand, if the function switching signal to be inputted to the function switching pin FP0 is OPEN (in Fig. 4) and if the function switching signal to be inputted to the function switching pin FP1 is exemplified by the supply voltage Vcc, the



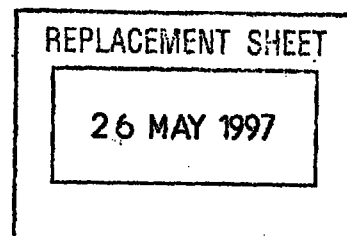
memory 1 is selected for the function in which the refresh cycle is 2 K and in which the reading mode is FAST PAGE.

With reference to Fig. 5, here will be described a method of switching the function of the memory 1 and the word structure. Moreover, Fig. 5 does not explain the actual mounting arrangement but schematically shows the connection state of the memory 1 in a memory module MM.

First of all, in the memory module MM of Fig. 5, a module wiring substrate (or printed-wiring substrate) 5 for mounting the memory 1 is equipped with function switching means KK1 for arbitrarily switching the function switching signal to be inputted to the function switching pin FP0 of the memory 1, and function switching means KK2 for arbitrarily switching the function switching signal to be inputted to the function switching pin FP1 of the memory 1.

On the other hand, the function switching signal is selected from any of the no connection, the supply voltage Vcc and the ground potential Vss.

Moreover, the function switching pins FP0 and FP1 of all the memories 1, as mounted on the module wiring substrate 5, are so wired by a wiring pattern HP that they are connected with the function switching means



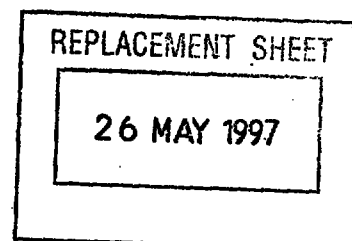
KK1 and KK2, respectively.

By these function switching means KK1 and Kk2, moreover, the aforementioned function switching signals can be arbitrarily switched and inputted as a whole to all the mounted memories 1 so that the functions, as constructed to include the reading mode and the refresh cycle as shown in Fig. 4, can be switched and arbitrarily set.

With reference to Figs. 6 and 7, here will be specifically described the memory module which is actually provided with the aforementioned function switching means KK1 and KK2 for switching the functions.

First of all, the memory module is constructed by mounting the TCP type memories 1 (as shown in Fig. 2) or a surface mounting package to make a predetermined memory structure. In this memory module, the module wiring substrate 5 for mounting the memories 1 has a front surface 5a and a back surface 5b, on which a predetermined number of memories 1 are mounted in the longitudinal direction of the module wiring substrate 5. The memories 1, as mounted on the surfaces 5a and 5b of the module wiring substrate 5, are stacked in two stages to make a stacked structure.

On the surfaces 5a and 5b of the module wiring

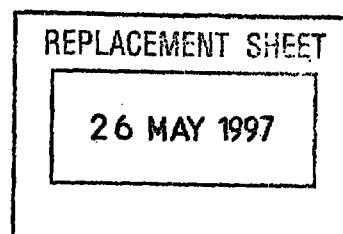


substrate 5, moreover, there are formed the lands which are so electrically connected with predetermined destinations that the memories 1 and the various chip parts necessary for the memory module may be mounted.

5 In the vicinity of the corner portion of one longer side of the back surface 5b of the module wiring substrate 5, on the other hand, there are provided: a land (or a first node) L1 for mounting a later-described conducting chip for switching the
10 state of the function switching signal to the function switching pin FP0 (as shown in Fig. 2), as disposed in the memory 1, a land (or a second node) L2, a land (or a third node) L3, a land (or a first node) L4 for mounting a conducting chip for switching the state of
15 the function switching signal to the function switching pin FP1 (as shown in Fig. 2), a land (or a second node) L5, and a land (or a third node) L6.

20 At the other longer side of the surfaces 5a and 5b of the module wiring substrate 5, moreover, there are provided a predetermined number of module I/O terminals MT which are arranged in the longitudinal direction of the module wiring substrate 5.

25 On the surfaces 5a and 5b of the module wiring substrate 5, moreover, there are formed the wiring patterns, by which the individual lands and module I/O



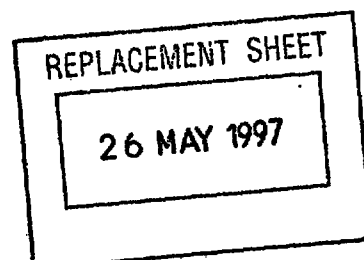
terminals MT are individually electrically connected with the predetermined connection destinations.

The land L1 is electrically connected by a predetermined wiring pattern with the land, at which
5 are overlapped the function switching pins FPO of all the mounted memories 1, and the land L2 is electrically connected through the wiring pattern with the supply voltage Vcc whereas the land L3 is electrically connected through the wiring pattern with
10 the ground potential Vss.

The later-described conducting chip is mounted or not between the land L1 and the land L2 or between the land L1 and the land L3 so that it may be inputted as the function switching signal to the memory 1 to
15 effect the function switching operations selectively all at once.

The function switching means KK1 is constructed to include those lands L1 to L3 and the conducting chips."

20 The land L4 of the module wiring substrate 5 is electrically connected by a predetermined wiring pattern with the land, at which are overlapped the function switching pins FP1 of all the memories 1 to be mounted, and the land L5 is electrically connected
25 with the supply voltage Vcc through the wiring pattern



whereas the land L6 is electrically connected with the ground potential Vss through the wiring pattern.

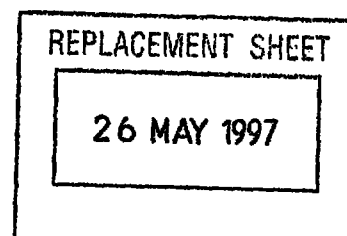
The later-described conducting chip is mounted or not between the land L4 and the land L5 or between the land L4 and the land L6 so that it may be inputted as the function switching signal to the memory 1 to effect the function switching operations selectively all at once.

The function switching means KK2 is constructed to include those lands L4 to L6 and the conducting chips.

The lands L1 to L3 and L4 to L6 of the module wiring substrate 5 for mounting the conducting chips are formed in the vicinity of the corner portion of one longer side, where the module I/O terminals MT are not disposed, so that the conducting chips can be easily mounted/demounted even for the memory module MM which is sealed by the metal case.

By mounting the memories 1 and the chip parts in the module wiring substrate 5, as shown in Fig. 7, moreover, there is constructed the memory module MM called 8-byte DIMM (dual inline memory module).

Here in Fig. 7, the memories 1 are switched such that the word structure is set in advance to 4 M x 4 bits and such that the switching of the functions is

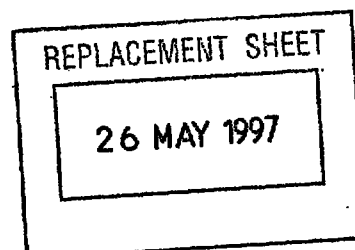


so selected by the function switching signal inputted to the function switching pins FP0 and FP1 as to set the refresh cycle to 2 K cycle and the reading mode to FAST PAGE.

5 When the refresh cycle is set to 2 K cycle and the reading mode is set to FAST PAGE, as described above, it is found from Fig. 4 that the function switching signal to be inputted to the function switching pin FP0 may be non-connected whereas the
10 function switching signal to be inputted to the function switching pin FP1 may be selected to the supply voltage Vcc.

 As a result, the function switching pin FP0 is open so that the conducting chips or the chip parts
15 such as jumpers or resistors are not mounted on the lands L1 to L3 to bring the function switching pins FP0 of all the memories 1, as mounted on the module wiring substrate 5, altogether into open state.

 Since the supply voltage Vcc is inputted to the
20 function switching pin FP1, on the other hand, a conducting chip (or conducting means) JC or a chip part such as a jumper or resistor is mounted between the land L4 and the land L5, as connected with the supply voltage Vcc, so that the supply voltage Vcc is
25 inputted to the function switching pins FP1 of all the



memories 1, as mounted on the module wiring substrate
5.

Thus, when the supply voltage V_{cc} is to be fed to
the function switching pins FP1 of all the memories 1
5 (as shown in Fig. 2), as shown in Fig. 8, it is
sufficient to mount the conducting chip JC between the
land L4 and the land L5 of the module wiring substrate
5 (as shown in Fig. 6).

Here, the connection state in this memory module
10 MM is shown in a block diagram of Fig. 9. As shown in
Fig. 9, the function switching signals to be inputted
to the function switching pins FP1 and FP0 of all the
memories 1 are selectively switched altogether by the
function switching means KK1 and KK2.

15 Next, there is shown in Fig. 10 a mounting
example of the case in which the memory module MM is
made of the SODIMM (small outlet dual inline memory
module).

In this case, too, a predetermined number of TCP
20 type memories 1 are mounted individually on the
surfaces 5a and 5b of the module wiring substrate 5 to
construct the predetermined memory structure so that
the memories 1 make the stacked structure in which
they are mounted in two stages.

25 In the vicinity of the corner portion of one

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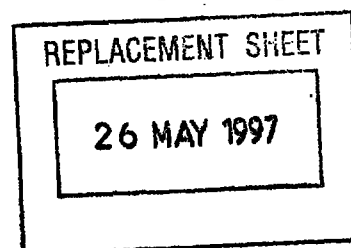
26 MAY 1997

longer side of the front surface 5a of the module wiring substrate 5, on the other hand, as in the aforementioned 8-byte DIMM memory module, there are disposed the lands L1, L3, L4 and L5 for mounting the
5 later-described conducting chips for switching the states of the function switching signals to the function switching pins FP0 and FP1, as mounted in the memory 1.

Moreover, the land L1 is electrically connected
10 by a predetermined wiring pattern with the land in which are overlapped the function switching pins FP0 of all the mounted memories 1, and the land L3 is electrically connected through the wiring pattern with the ground potential Vss.

15 On the other hand, the land L4 is electrically connected by a predetermined pattern with the land in which are overlapped the function switching pins FP1 of all the mounted memories 1, and the land L5 is electrically connected through a wiring pattern with
20 the supply voltage Vcc.

Moreover, the conducting chip is mounted or not between the land L1 and the land L3 or between the land L4 and the land L5 so that the function switching signal is inputted to the memory 1 to effect the
25 function switching operations selectively altogether.



Moreover, the lands L1 and L3 or the lands L4 and L5 of the module wiring substrate 5 for mounting the conducting chips or the chip parts such as the jumpers or resistors are formed in the vicinity of the corner portion of one longer side, where the module I/O terminals MT are not disposed, as shown in Fig. 10, and the conducting chips can be easily mounted/demounted even from the memory module which is sealed by the metal case.

10 On the other hand, the module wiring substrate 5 to be used in the memory module made of the SODIMM is formed according to the standards, as shown in Figs. 11A, 11B, 11C, 11D and 11E.

Moreover, the connection state in the memory
15 module MM is shown in a block diagram in Fig. 12.

As shown in Fig. 12, the function switching signals to be inputted to the function switching pins FP1 of all the memories 1 are selectively switched altogether to either the supply voltage Vcc or the
20 non-connection by the function switching means KK1, and the function switching signals to be inputted to the function switching pins FP0 of all the memories 1 are selectively switched altogether to the ground potential Vss or no connection by the function
25 switching means KK2.

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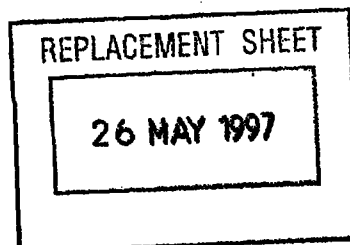
26 MAY 1997

As a result, when the input of the function switching pin FP0 is open (as indicated by 'OFF' in Fig. 12), the reading mode is the FAST PAGE. When the input of the function switching pin FP0 is at the ground potential Vss (as indicated by 'ON' in Fig. 12), the reading mode is the EDO mode.

On the other hand, when the input of the function switching pin FP1 is open, the refresh cycle is 4 K cycle. When the input of the function switching pin FP1 is at the supply voltage Vcc (as indicated by 'ON' in Fig. 12), the refresh cycle is 2 K cycle.

With the reading mode being the EDO and the refresh cycle being 4 K cycle, for example, the input of the function switching pin FP0 is at the ground potential Vss, and the input of the function switching pin FP1 may be open. As shown in Fig. 10, therefore, the conducting chip JC may be mounted between the land L1 and the land L3 but may be omitted between the lands L4 and L5.

Here, the function switching signal is selectively switched to either the supply voltage Vcc or no connection, or the ground potential Vss or no connection by the function switching means KK1 and KK2. However, these function switching means KK1 and KK2 are made to select the supply voltage Vcc, the



ground potential Vss or no connection so that those function switching signals can be combined to switch the functions in the memory 1.

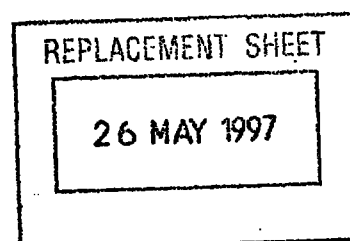
As a result, the following effects can be achieved according the present Mode 1 of Embodiment.

(1) The functions of all the mounted memories 1 can be switched and set altogether by the function switching means KK1 and KK2 so that the functions of the memory module MM can be easily switched for a short time period.

(2) The assembly specifications of the memory module MM can be made common to improve the developing efficiency of products and facilitate the product management.

(3) By providing the function switching means KK1 and KK2 at the corner portion or in its vicinity of the module wiring substrate 5, the functions of the memories 1 even in the memory module, as completed as a product, can be easily switched for a short time period to improve the degree of freedom for the productivity drastically.

Fig. 13 is a pin arrangement diagram of a memory according to Mode 2 of Embodiment of the present invention, and Figs. 14, 15 and 16 are explanatory diagrams showing the memory module in which are

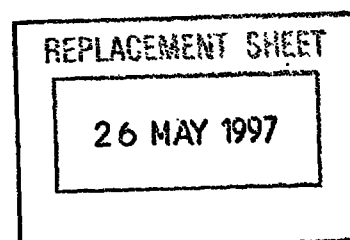


mounted the memories according to the present invention.

In the present Mode 2 of Embodiment, a memory 1a is made of a TCP type DRAM semiconductor device or a kind of surface mounting package. As shown in Fig. 13, the memory 1a is constructed to include a total number 36 of pins. Of these, the 2nd and 35th pins, as connected with the function switching bonding pads BP1 and BP0, are provided with outer leads as the function switching pins FP1 and FP0 so that an arbitrary function is switched depending upon the state of the function switching signal inputted.

On the other hand, the memory 1a is equipped as word structure switching pins (or word structure switching external terminals) FP3 and FP2 with the outer leads of the 17th and 20th pins, as connected with the bonding pads BP3 and BP2 for switching the word structure, so that an arbitrary word structure is switched depending upon the state of the word structure switching signal to be inputted to the pins FP3 and FP2.

Moreover, there are provided data input/output pins I00 to I07, a pin WE for designating whether the access is to read or write, address input pins A0 to A11, pins RAS and CAS for row and column selecting

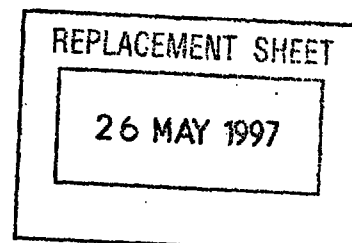


signals, a pin OE for a signal to control the states
of a data output signal and a data input/output signal
at a reading time, a pin Vcc for the supply voltage
Vcc, and a pin Vss for a ground potential or the
5 reference potential.

The internal connection structure in the memory
1a is specifically described below.

First of all, as shown in Fig. 4, for example,
the memory 1a can arbitrarily switch the functions to
10 switch the refresh cycle or the cycle of the
refreshing operation and the reading mode of FAST PAGE
and ED0, on the basis of the function switching
signals to be inputted to the function switching pins
FP1 and FP0, and can switch three kinds of word
15 structures of 4 M x 1 bit, 1 M x 4 bits and 512 K x 8
bits on the basis of the word structure switching
signals to be inputted to the word structure switching
pins FP3 and FP2.

The functions of the memory 1a are switched by
20 inputting the signals, as selected from the function
switching signals such as the supply voltage Vcc, the
ground potential Vss or no connection to the pins FP1
and FP0 for switching the functions of the 2nd and
35th pins, as shown in Fig. 13, and by combining those
25 signals, as shown in Fig. 4.



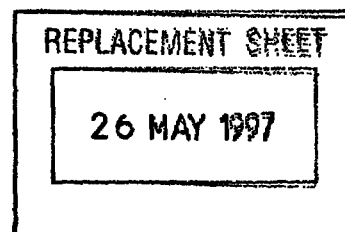
The word structure of the memory 1a is likewise switched by inputting the signals, as selected from the word structure switching signals such as the supply voltage Vcc, the ground potential Vss or no connection, to the word structure switching pins FP3 and FP2 of the 17th and 20th pins for switching the word structure, and by combining those signals, as shown in Fig. 4.

With reference to Figs. 14, 15, 16 and 17, here will be described the method of switching the functions and the word structure of the memory 1a. On the other hand, Figs. 14, 15, 16 and 17 show not the actual mounting structure but schematically the connection state of the memories 1a in the memory module.

First of all, as shown in Fig. 14, the substrate to be used for mounting the memories 1a is exemplified by a dedicated module wiring substrate (or a dedicated printed-wiring substrate) 6 which is wired in advance to correspond to a predetermined word structure.

On the module wiring substrate 6, on the other hand, there are mounted the memories 1a which are equipped with the function switching pins FP1 and FP0 and the word structure switching pins FP3 and FP2.

On the module wiring substrate 6, moreover, there



is wired a wiring pattern (or a word structure setting line) HP1 for inputting a predetermined word switching signal of no connection, the supply voltage Vcc or the ground potential Vss to the word structure switching pins FP3 and FP2 of the memories 1a so that a
5 predetermined word structure may be set.

On the other hand, the module wiring substrate 6 is equipped with the function switching means KK1 for arbitrarily switching the function switching signal,
10 as selected from no connection, the supply voltage Vcc or the ground potential Vss to be inputted to the function switching pins FP0 of the memories 1a, and the function switching means KK2 for arbitrarily switching the function switching signal, as likewise
15 selected from any of no connection, the supply voltage Vcc or the ground potential Vss to be inputted to the function switching pins FP1 of the memories 1a.

Moreover, The function switching pins FP0 and FP1 of all the memories 1a, as mounted on the module
20 wiring substrate 6, are so wired by the wiring pattern HP that they may be connected with the function switching means KK1 and KK2, respectively.

As a result, the aforementioned function switching signals can be arbitrarily switched by those
25 function switching means KK1 and KK2 to switch and set

REPLACEMENT SHEET

26 MAY 1997

arbitrarily the functions including of the reading
mods and the refresh cycles, as shown in Fig. 4.

As a result, the functions of the memories 1a can
be arbitrarily switched and set by the function .

5 switching means KK1 and KK2 even before or after the
memories 1a are mounted.

Next, in order that an arbitrary word structure
may be set on the dedicated module wiring substrate 6
mounting the memories 1 thereon, as shown in Fig. 15,
10 there are provided word structure switching means WK1
and WK2 for switching any of no connection, the supply
voltage Vcc or the ground potential Vss arbitrarily as
the word structure switching signal to the word
structure switching pins FP3 and FP2 of the memories
15 1a.

On the module wiring substrate 6, on the other
hand, there are likewise provided the function
switching means KK1 and KK2 for switching the
aforementioned function switching signal arbitrarily
20 to the function switching pins FP0 and FP1 of the
memories 1a.

Moreover, the function switching pins FP0 and FP1
of all the memories 1a, as mounted on the module
wiring substrate 6, are so wired by the wiring pattern
25 HP that they may be connected with the function

REPLACEMENT SHEET

26 MAY 1997

switching means KK1 and KK2, respectively, and the word structure switching pins FP2 and FP3 of all the memories 1a are so wired by the wiring pattern HP that they may be connected with the word structure

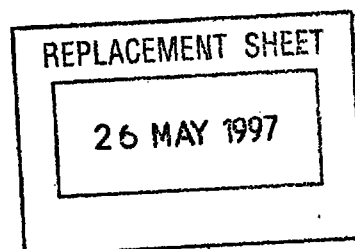
5 switching means WK1 and WK2, respectively.

As a result, the function switching signals are arbitrarily switched by those function switching means KK1 and Kk2 to arbitrarily switch and set the functions including the reading modes and the refresh
10 cycles, as shown in Fig. 4.

The word structure switching signals are so switched by the word structure switching means WK1 and WK2 that the memories 1a may be switched and set to the word structure corresponding to the module wiring
15 substrate 6.

As a result, the functions and the word structures of the memories 1a can be arbitrarily switched and set by the function switching means KK1 and KK2 and the word structure switching means WK1 and
20 WK2 even before or after the memories 1a are mounted.

Only the word structure switching means for switching the word structures may be provided on the module wiring substrate, and the functions may be switched by wiring the wiring pattern, in which a
25 predetermined function switching signal is inputted to



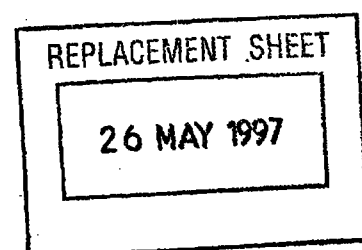
the function switching pins of the memories, as mounted for the predetermined function to be switched and set, so that the functions may be arbitrarily set by switching the word structures.

5 In this case, too, the dedicated module wiring substrate, as corresponding to the word structures and functions to be switched and set, is prepared to mount the memories thereon.

10 Next, on the dedicated module wiring substrate 6 having the memories 1a mounted thereon, as shown in Fig. 16, there are formed the wiring pattern HP1, which is so wired that the preset word structure switching signal may be inputted to the word structure switching pins FP3 and FP2, and a wiring pattern (or a
15 function setting line) HP2 which is so wired that the preset function switching signal may be inputted to the function switching pins FP1 and FP0.

20 The functions and the word structures of the memories 1a are automatically switched and set by selecting the dedicated module wiring substrate 6, for which the predetermined function and word structure are switched and set in advance, and by mounting the memories 1a on the selected module wiring substrate 6.

25 The aforementioned function switching means KK1 is constructed to include conducting chips for

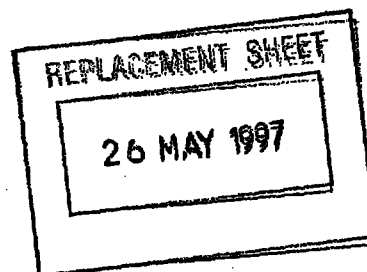


selecting the state of the function switching signal to the function switching pin FP0 (as shown in Fig. 13), as mounted on the memories 1a, and mounting lands for mounting the conducting chips.

5 These mounting lands include: function lands electrically connected by a predetermined wiring pattern with the lands, at which are overlapped the function switching pin FP0; power lands electrically connected through the wiring pattern with the supply
10 voltage Vcc; and ground lands electrically connected through the wiring pattern with the ground potential Vss.

 Likewise, the aforementioned function switching means KK2 is also constructed to include conducting
15 chips for switching the state of the function switching signal to the function switching pin FP1 (as shown in Fig. 13), as mounted on the memories 1a, and mounting lands for mounting the conducting chips.

 These mounting lands include: function lands
20 electrically connected by a predetermined wiring pattern with the lands, at which are overlapped the function switching pin FP1; power lands electrically connected through the wiring pattern with the supply voltage Vcc; and ground lands electrically connected
25 through the wiring pattern with the ground potential



Vss.

With or without the conducting chips provided between the function lands and the power lands or between the function lands and the ground lands, any of the supply voltage Vcc, the ground potential Vss and no connection may be arbitrarily selected and inputted as the function switching signal to the memories 1a to effect the function switching operations selectively altogether.

Next, the aforementioned word structure switching means WK1 include conducting chips (or conducting means) for switching the state of the function switching signal to the word structure switching pins FP2 (as shown in Fig. 13), as mounted on the memories 1a, and mounting lands for mounting the conducting chips thereon.

These mounting lands include: word lands (or fourth nodes) electrically connected by a predetermined wiring pattern with the lands, at which are overlapped the word structure switching pins FP2; power lands (or fifth nodes) electrically connected through the wiring pattern with the supply voltage Vcc; and ground lands (or sixth nodes) electrically connected through the wiring pattern with the ground potential Vss.

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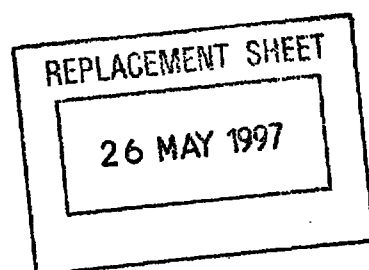
26 MAY 1997

The word structure switching means WK2 is constructed to include conducting chips for switching the state of the function switching signal to the word structure switching pins FP3 (as shown in Fig. 13), as
5 mounted on the memories 1a, and mounting lands for mounting the conducting chips thereon.

These mounting lands include: word lands electrically connected by a predetermined wiring pattern with the lands, at which are overlapped the
10 word structure switching pins FP3; power lands electrically connected through the wiring pattern with the supply voltage Vcc; and ground lands electrically connected through the wiring pattern with the ground potential Vss.

15 With or without the conducting chips provided between the word lands and the power lands or between the word lands and the ground lands, any of the supply voltage Vcc, the ground potential Vss and the non-connection may be arbitrarily selected and inputted as
20 the function switching signal to the memories 1a to effect the word switching operations selectively altogether.

The mounting lands for mounting the aforementioned conducting chips are arranged in the
25 vicinity of the corner portion of the module wiring



substrate 6 so that they can be easily mounted/
demounted even from the memory module which is
shielded by the metal case.

As a result, the following effects can be
5 achieved according the present Mode 2 of Embodiment.

(1) The functions and word structures of all the
mounted memories 1a can be switched altogether by the
function switching means KK1 and KK2 and the word
structure switching means WK1 and WK2 so that the
10 functions of the memory module MM can be easily
switched for a short time period.

(2) Thanks to the aforementioned effect (1), the
specifications of the film to be used for the memories
1a can be made common to reduce the cost and improve
15 the productivity.

(3) The assembly specifications of the memory module
MM can be made common to improve the developing
efficiency of products and facilitate the product
management.

20 (4) By providing the function switching means KK1 and
KK2 and the word structure switching means WK1 and WK2
at the corner portion or in its vicinity of the module
wiring substrate 6, the functions of the memories 1a
even in the memory module, as completed as a product,
25 can be easily switched for a short time period.

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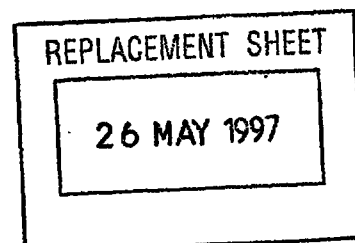
26 MAY 1997

The present Mode 2 of Embodiment has been described on the TCP type memories 1a. Despite of this description, however, the memory module may be constructed by using either the memories having BGA (ball grid array) structure such as the CSP (chip size package) type made of a package having an external diameter substantially equal to that of the semiconductor chip or the memories having the LOC (lead on chip) structure of the SOJ (small outline j-leaded Package) type.

In a CSP type memory 1b, for example, predetermined pins are assigned as the function switching pins FP1 and FP0 for switching the functions and the word structure switching pins FP3 and FP2 for switching the word structures, as shown in Fig. 17.

On the module wiring substrate having those memories 1b mounted thereon, on the other hand, there are also provided the function switching means and the word structure switching means so that the functions and the word structures can be arbitrarily switched by inputting the function switching signals to the function switching pins FP1 and FP0 and the word structure switching signals to the word structure switching pins FP3 and FP2.

Next, in the SOJ type memory 1c, for example, the

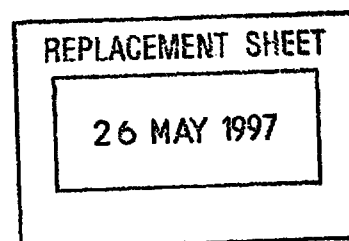


predetermined pins are assigned as the function switching pins FP1 and FP0 for switching the functions and the word structure switching pins FP3 and FP2 for switching the word structures. These function
5 switching pins FP1 and FP0 and word structure switching pins FP3 and FP2 are electrically connected bonding wires W with the bonding pads, as mounted on the semiconductor chips 2, such as the predetermined function switching pads BP1 and BP0 and the word
10 structure switching pads BP3 and BP2, respectively.

On the module wiring substrate for mounting the memories 1c, on the other hand, there are also mounted the function switching means and the word structure switching means so that the functions and the word
15 structures can be arbitrarily switched by inputting the function switching signals to the function switching pins FP1 and FP0 and the word structure switching signals to the word structure switching pins FP3 and FP2.

20 Although our invention has been specifically described on the basis of its modes of embodiment, it should not be limited to the aforementioned modes of embodiment but can naturally be modified in various manners without departing from the gist thereof.

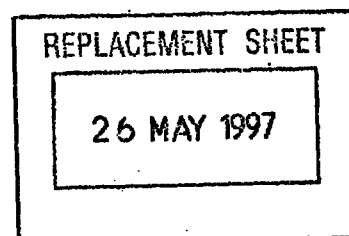
25 In the foregoing Modes 1 and 2 of Embodiment, for



example, the function switching signals and the word structure switching signals are fed altogether by the function switching means and the word structure switching means to all the memories that are mounted
5 on the memory module. Despite of this fact, however, the function switching signals and the word structure switching signals need not be fed altogether to all the memories mounted on the memory module, but the function switching means and the word structure
10 switching means may be provided for every two or three memories.

In the foregoing Modes 1 and 2 of Embodiment, on the other hand, the connection destinations are switched by selectively mounting/demounting the
15 conducting chips or the chip parts such as the jumpers or resistors. However, the function switching signals to be inputted to the function switching pins of the memories and the word structure switching signals to be inputted to the word structure switching pins may
20 be selected and switched to the module wiring substrate by using the semiconductor device such as the EEPROM (electrically erasable programmable read only memory).

In this modification, the predetermined pins of
25 the EEPROM are electrically connected by a wiring

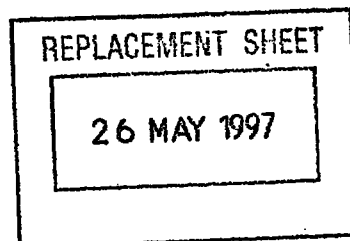


pattern with the function switching pins of the individual memories which are mounted on the module wiring substrate.

To the EEPROM, there is inputted in advance a
5 program for giving predetermined functions to the individual memories so that the EEPROM switches the functions and the word structures of the memories by setting on the basis of the program the electric levels of predetermined pins, as connected with the
10 function switching pins and the word structure switching pins, to any of the supply voltage, the ground voltage or no connection.

In the foregoing Modes 1 and 2 of Embodiment, moreover, when the function switching pins and the
15 word structure switching pins are open, the conducting chips, as connected with the function switching pins, are not mounted. However, this non-connection state may be effected by cutting the non-connected function switching pins and word structure switching pins from
20 the package end portions at the lead cutting step and disconnecting them from the lands for mounting the memories.

In the foregoing Modes 1 and 2 of Embodiment, on the other hand, the operations to switch the functions
25 of the memories are effected by the reading modes



including the refresh cycles and the FAST PAGE and
EDO. However, the various switching operations such
as the DRAM operation modes or the synchronous DRAM
operation modes may be effected from the outside by
5 the function switching means.

Effects of the Invention

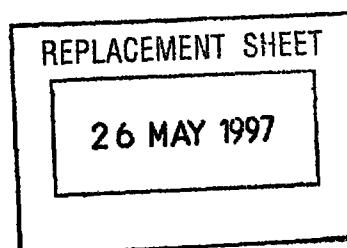
The effects to be obtained from the
representatives of the invention, as disclosed herein,
will be briefly described in the following.

10 (1) According to the present invention, the assembly
specifications of the memory module can be made common
to make it unnecessary to manage the semiconductor
device for the individual functions.

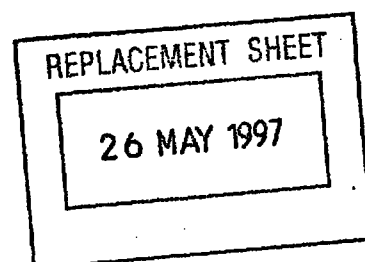
(2) In the present invention, on the other hand, the
15 functions of the semiconductor device can be
arbitrarily switched even after the memory module is
completed, so that the specifications of the printed-
wiring substrate can be unified to cope with the
change in the specifications flexibly.

20 (3) In the present invention, moreover, the functions
of the semiconductor device can be easily switched at
a low cost by selectively mounting/demounting the
conducting means such as the jumpers or resistors.

(4) In the present invention, moreover, thanks to the
25 aforementioned effects (1) to (3), it is possible to



drastically improve the product developing efficiency
and the productivity of the semiconductor device and
to facilitate the product management.





WE CLAIM:

1. A memory module comprising:

at least one semiconductor device including
5 function switching external terminals for selecting a
function in dependence upon the state of a function
switching signal; and

a printed-wiring substrate with said
semiconductor device mounted thereon and including
10 function switching means for selecting an arbitrary
function switching signal to be inputted to said
function switching external terminals.

2. A memory module according to claim 1,

15 wherein said function switching means includes:

a first node formed on said printed-wiring
substrate and electrically connected with the function
switching external terminal of said semiconductor
device, as mounted on said printed-wiring substrate;

20 a second node formed on said printed-wiring
substrate and connected with a supply voltage; and

a third node formed on said printed-wiring
substrate and connected with a reference voltage, and

wherein said function switching means is means
25 for switching the function switching signals

REPLACEMENT SHEET

26 MAY 1997



altogether, as inputted to said function switching external terminals, with or without conducting means provided between said first node and said second node or between said first node and said third node.

5

3. A memory module according to claim 1,
wherein said function switching means is arranged at or in the vicinity of a corner portion of said printed-wiring substrate.

10

4. A memory module according to claim 1,
wherein the function of said semiconductor device to be switched by said function switching means includes a reading mode.

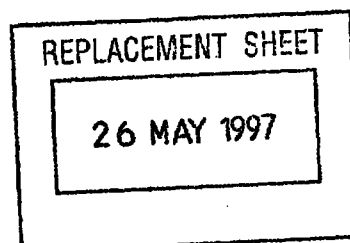
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5. A memory module according to claim 1,
wherein the function of said semiconductor device to be switched by said function switching means includes a refresh cycle.

20

6. A memory module according to claim 1,
wherein the function of said semiconductor device to be switched by said function switching means includes a reading mode and a refresh cycle.

25





7. A memory module according to claim 1,
wherein said semiconductor device further
includes word structure switching external terminals
for selecting a word structure in dependence upon the
5 state of a word structure switching signal, and

wherein said printed-wiring substrate further
includes word structure setting lines for inputting a
preset word structure switching signal to said word
structure switching external terminals.

10

8. A memory module comprising:

at least one semiconductor device including word
structure switching external terminals for selecting a
word structure in dependence upon the state of a word
15 structure switching signal; and

a dedicated printed-wiring substrate with said
semiconductor device mounted thereon and including
dedicated lines corresponding to the switched word
structure of said semiconductor device.

20

9. A memory module according to claim 8, further
comprising: word structure switching means mounted on
said dedicated printed-wiring substrate for selecting
an arbitrary word structure switching signal to be
25 inputted to said word structure switching external

REPLACEMENT SHEET

26 MAY 1997



terminals.

10. A memory module according to claim 9,

wherein said word structure switching means

5 includes word structure setting lines wired on said
dedicated printed-wiring substrate and adapted to be
switched to a predetermined word structure by mounting
said semiconductor device so that a predetermined word
structure switching signal is inputted to said word
10 structure switching external terminals.

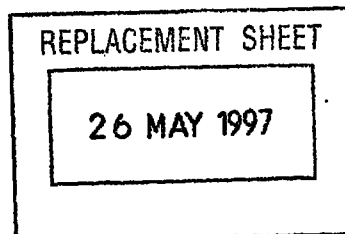
11. A memory module according to claim 9,

wherein said word structure switching means
includes:

15 a fourth node formed on said dedicated printed-
wiring substrate and electrically connected with the
word structure switching external terminal of said
semiconductor device, as mounted on said dedicated
printed-wiring substrate;

20 a fifth node formed on said dedicated printed-
wiring substrate and connected with a supply voltage;
and

a sixth node formed on said dedicated printed-
wiring substrate and connected with a reference
25 voltage, and



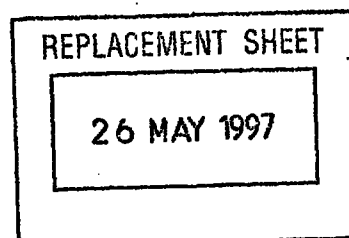


wherein said word structure switching means is means for switching the word structure switching signals altogether, as inputted to said word structure switching external terminals, with or without
5 conducting means provided between said fourth node and said fifth node or between said fourth node and said sixth node.

12. A memory module according to claim 8,
10 wherein said semiconductor device further includes function switching external terminals for selecting a function in dependence upon the state of a function switching signal, and

wherein said dedicated printed-wiring substrate
15 further includes function switching means for selecting an arbitrary function switching signal to be inputted to said function switching external terminals.

20 13. A memory module according to claim 12,
wherein said function switching means includes:
a first node formed on said dedicated printed-wiring substrate and electrically connected with the function switching external terminal of said
25 semiconductor device, as mounted on said dedicated





printed-wiring substrate;

a second node formed on said dedicated printed-wiring substrate and connected with a supply voltage;
and

5 a third node formed on said dedicated printed-wiring substrate and connected with a reference voltage, and

wherein said function switching means is means for switching the function switching signals
10 altogether, as inputted to said function switching external terminals, with or without conducting means provided between said first node and said second node or between said first node and said third node.

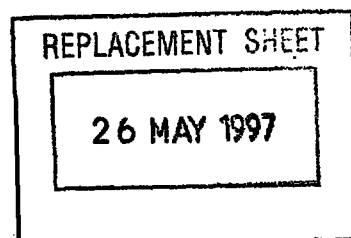
15 14. A memory module according to claim 12,

wherein the function of said semiconductor device to be switched by said function switching means includes a reading mode.

20 15. A memory module according to claim 12,

wherein the function of said semiconductor device to be switched by said function switching means includes a refresh cycle.

25 16. A memory module according to claim 12,

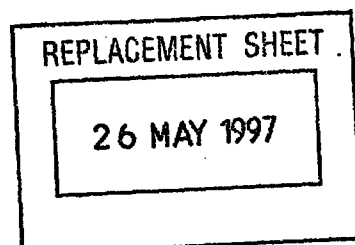




wherein the function of said semiconductor device to be switched by said function switching means includes a reading mode and a refresh cycle.

5 17. A memory module according to claim 12,
wherein said function switching means includes function setting lines wired on said dedicated printed-wiring substrate and adapted to be switched to a predetermined function by mounting said at least one
10 semiconductor device so that a predetermined function switching signal is inputted to said function switching external terminals.

18. A process for manufacturing a memory module,
15 comprising:
the step of preparing a semiconductor device for switching a predetermined word structure on the basis of a word structure switching signal, as inputted to word structure switching external terminals, and a
20 plurality of kinds of dedicated printed-wiring substrates corresponding to a plurality of word structures, and selecting one of said dedicated printed-wiring substrates, as corresponding to a demanded word structure of said semiconductor device,
25 from said plurality of kinds of dedicated printed-





wiring substrates; and

the step of mounting said semiconductor device on the selected one of said dedicated printed-wiring substrates.

5

19. A process for manufacturing a memory module, comprising:

the step of preparing a semiconductor device for selecting a word structure on the basis of a word structure switching signal, as inputted to word structure switching external terminals, and for selecting a function on the basis of a function switching signal, as inputted to function switching external terminals, function switching means for selecting an arbitrary function switching signal, as inputted to said function switching external terminals by mounting conducting means or not, and a plurality of kinds of dedicated printed-wiring substrates corresponding to a plurality of word structures, and selecting one of said dedicated printed-wiring substrates, as corresponding to a demanded word structure of said semiconductor device, from said plurality of kinds of dedicated printed-wiring substrates;

25 the step of mounting said semiconductor device on

REPLACEMENT SHEET

26 MAY 1997



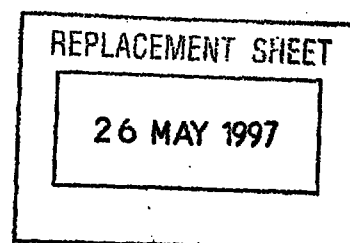
the selected one of said dedicated printed-wiring substrates; and

the step of selecting an arbitrary function selectively, with or without said conducting means
5 provided.

20. A process for manufacturing a memory module, comprising:

the step of preparing a semiconductor device for
10 selecting a predetermined word structure on the basis of a word structure switching signal, as inputted to word structure switching external terminals, and for selecting a predetermined function on the basis of a function switching signal, as inputted to function
15 switching external terminals, and a plurality of kinds of dedicated printed-wiring substrates corresponding to the switching operations of a plurality of word structures and a plurality of functions, and selecting one of said dedicated printed-wiring substrates, as
20 corresponding to a demanded word structure of said semiconductor device and the switching operation of the function, from said plurality of kinds of dedicated printed-wiring substrates; and

the step of mounting said semiconductor device on
25 the selected one of said dedicated printed-wiring





substrates.

21. A memory module comprising:

a wiring substrate having arranged lines;

5 a semiconductor device; and

a function switching circuit,

wherein said semiconductor device includes
function switching terminals for selecting an internal
function and mounted on said wiring substrate, and

10 wherein said function switching circuit is
electrically connected with the function switching
terminals of said semiconductor device and is arranged
on said wiring substrate.

15 22. A memory module according to claim 21,

wherein said function switching circuit includes
a first electrode, a second electrode and a third
electrode,

20 wherein said first electrode is electrically
connected with said function switching terminal,

wherein said second electrode is at a supply
voltage,

wherein said third electrode is at ground
potential, and

25 wherein the function of said semiconductor device

REPLACEMENT SHEET

26 MAY 1997



is switched by rendering said first electrode and said second electrode, or said first electrode and said third electrode conductive or inconductive.

- 5 23. A memory module according to claim 22, further comprising: a conducting element for rendering the first electrode and the second electrode, or the first electrode and the third electrode of said function switching circuit conductive.

10

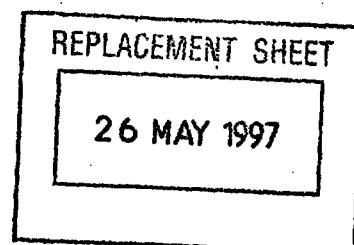
24. A memory module according to claim 22,
wherein the function of said semiconductor device to be switched by said function switching circuit includes a reading mode.

15

25. A memory module according to claim 22,
wherein the function of said semiconductor device to be switched by said function switching circuit includes a refresh cycle.

20

26. A memory module comprising:
a wiring substrate having arranged lines;
a semiconductor device;
a function switching circuit; and
25 word structure setting lines,





-57-

wherein said semiconductor device includes
function switching terminals for switching an internal
function and mounted on said wiring substrate, and
word structure switching terminals for selecting a
word structure, and

wherein said function switching circuit is
electrically connected with the function switching
terminals of said semiconductor device and is arranged
on said wiring substrate.

27. A memory module according to claim 26,

wherein said function switching circuit includes
a first electrode, a second electrode and a third
electrode,

wherein said first electrode is electrically
connected with said function switching terminal,

wherein said second electrode is at a supply
voltage,

wherein said third electrode is at ground
potential, and

wherein the function of said semiconductor device
is switched by rendering said first electrode and said
second electrode, or said first electrode and said
third electrode conductive or inconductive.

REPLACEMENT SHEET

26 MAY 1997



28. A memory module according to claim 27, further comprising: a conducting element for rendering the first electrode and the second electrode, or the first electrode and the third electrode of said function switching circuit conductive.

29. A memory module according to claim 27, wherein the function of said semiconductor device to be switched by said function switching circuit includes a reading mode.

30. A memory module according to claim 27, wherein the function of said semiconductor device to be switched by said function switching circuit includes a refresh cycle.

31. A memory module comprising:
a wiring substrate having interconnections;
a semiconductor device;
a function switching circuit; and
word structure switching lines,
wherein said semiconductor device includes function switching terminals for selecting an internal function and mounted on said wiring substrate, and word structure switching terminals for selecting a

REPLACEMENT SHEET

26 MAY 1997



word structure,

wherein said function switching circuit is connected with the function switching terminals of said semiconductor device and is arranged on said wiring substrate, and

wherein said word structure switching circuit is electrically connected with said word structure switching terminals and arranged on said wiring substrate.

10

32. A memory module according to claim 31,

wherein said function switching circuit includes a first electrode, a second electrode and a third electrode,

15

wherein said first electrode is electrically connected with said function switching terminal,

wherein said second electrode is at a supply voltage,

20

wherein said third electrode is at ground potential, and

wherein the function of said semiconductor device is switched by making on breaking the connection between said first electrode and said second electrode or said third electrode.

25

REPLACEMENT SHEET

26 MAY 1997



33. A memory module according to claim 32,
wherein said word structure switching circuit
includes a fourth electrode, a fifth electrode and a
sixth electrode,

5 wherein said fourth electrode is electrically
connected with said word structure switching terminal,
wherein said fifth electrode is at a supply
voltage,

wherein said sixth electrode is at ground
10 potential, and

wherein the word structure of said semiconductor
device is switched by making or breaking the
connection between said fourth electrode and said
fifth electrode or said sixth electrode.

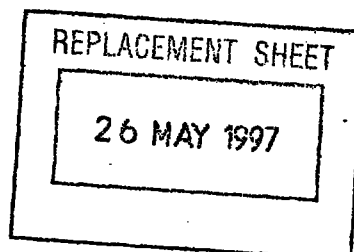
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34. A memory module according to claim 33,
wherein the function of said semiconductor device
to be switched by said function switching circuit
includes a reading mode.

20

35. A memory module according to claim 33,
wherein the function of said semiconductor device
to be switched by said function switching circuit
includes a refresh cycle.

25





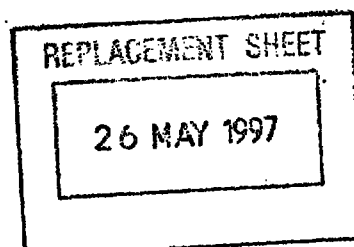
-61-

36. A memory module according to claim 33, wherein
the electrical connection between the first electrode
and the second electrode or the third electrode of
said function switching circuit is made through a
5 conducting element.

37. A memory module according to claim 36, wherein
the electrical connection between the fourth electrode
and the fifth electrode or the sixth electrode of said
10 word structure switching circuit is made through a
conducting element.

38. A memory module comprising:
a wiring substrate having interconnections;
15 a semiconductor device;
a function setting circuit; and
a word structure setting circuit,
wherein said semiconductor device includes
function switching terminals for selecting a function
20 and mounted on said wiring substrate, and word
structure switching terminals for selecting a word
structure,

wherein said function setting circuit is
connected with the function switching terminals of
25 said semiconductor device and is arranged on said





-62-

wiring substrate, and

wherein said word structure setting circuit is
electrically connected with said word structure
switching terminals and arranged on said wiring
5 substrate.

REPLACEMENT SHEET

26 MAY 1997

Semiconductor Device and Process for manufacturing
the Same

ABSTRACT OF THE DISCLOSURE

A memory module MM, in which a module wiring substrate 5 is equipped with function switching means KK1 and KK2 for arbitrarily switching function switching signals to be inputted to function switching pins FP0 and FP1 of memories 1. By these function switching means KK1 and KK2, moreover, the function switching signals are arbitrarily switched from any of no connection, a supply voltage Vcc and a ground potential Vss. These signals are inputted altogether to all the mounted memories 1 to switch and arbitrarily set functions including reading modes and refresh cycles.

Figure 5

