FIG. 1

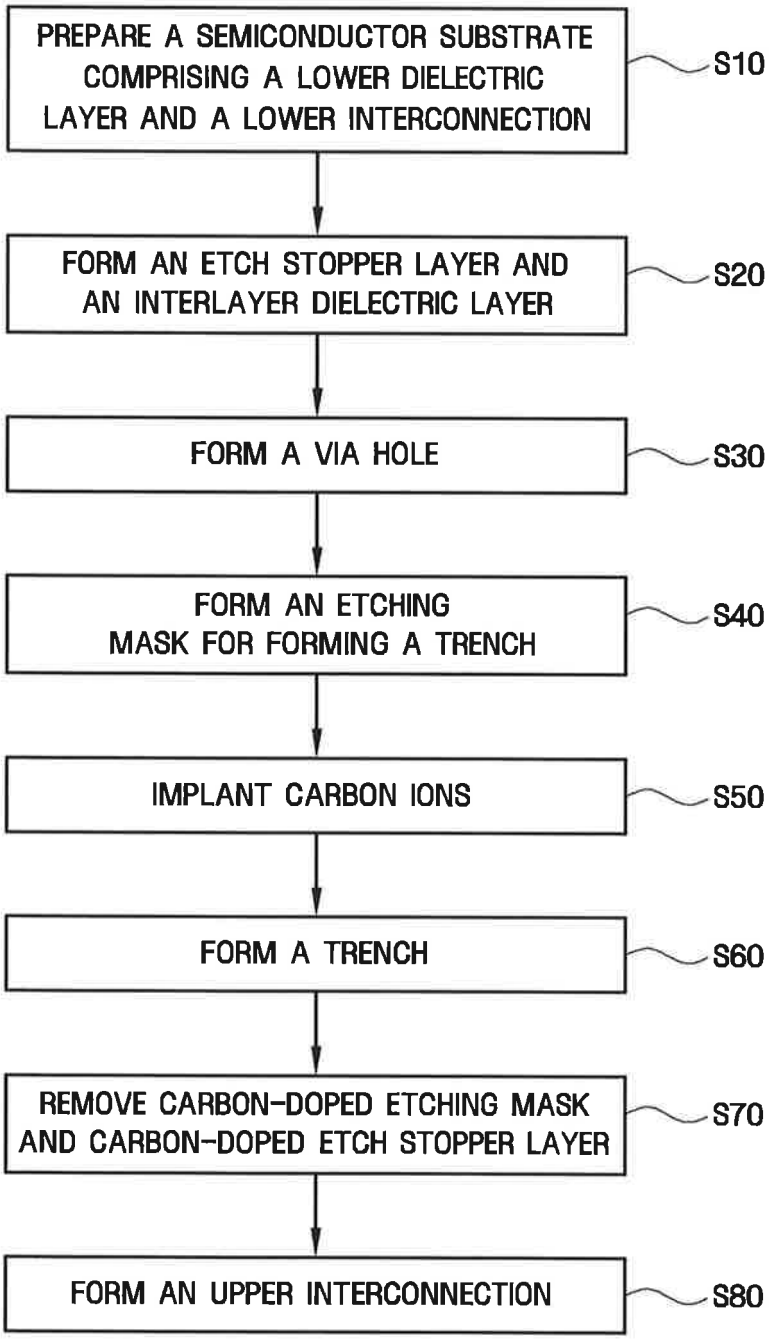

PREPARE A SEMICONDUCTOR SUBSTRATE COMPRISING A LOWER DIELECTRIC LAYER AND A LOWER INTERCONNECTION
S10
FORM AN ETCH STOPPER LAYER AND AN INTERLAYER DIELECTRIC LAYER
S20
FORM A VIA HOLE
S30
FORM AN ETCHING MASK FOR FORMING A TRENCH
S40
IMPLANT CARBON IONS
S50
FORM A TRENCH
S60
REMOVE CARBON-DOPED ETCHING MASK AND CARBON-DOPED ETCH STOPPER LAYER
S70
FORM AN UPPER INTERCONNECTION
S80

FIG. 2A

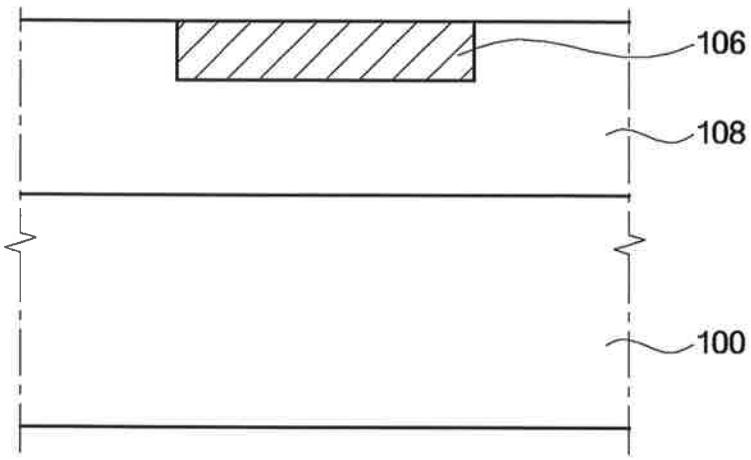


FIG. 2B

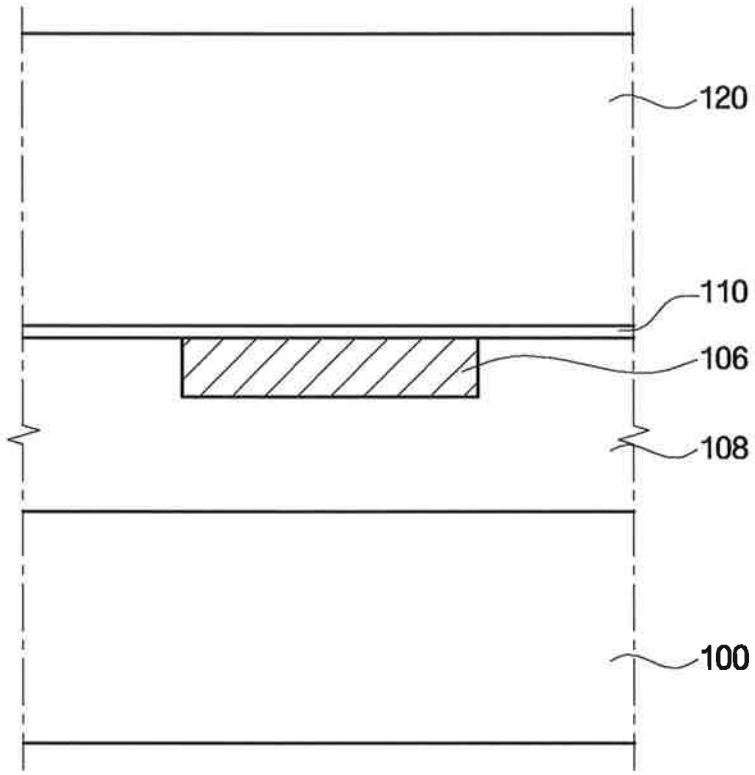


FIG. 2C

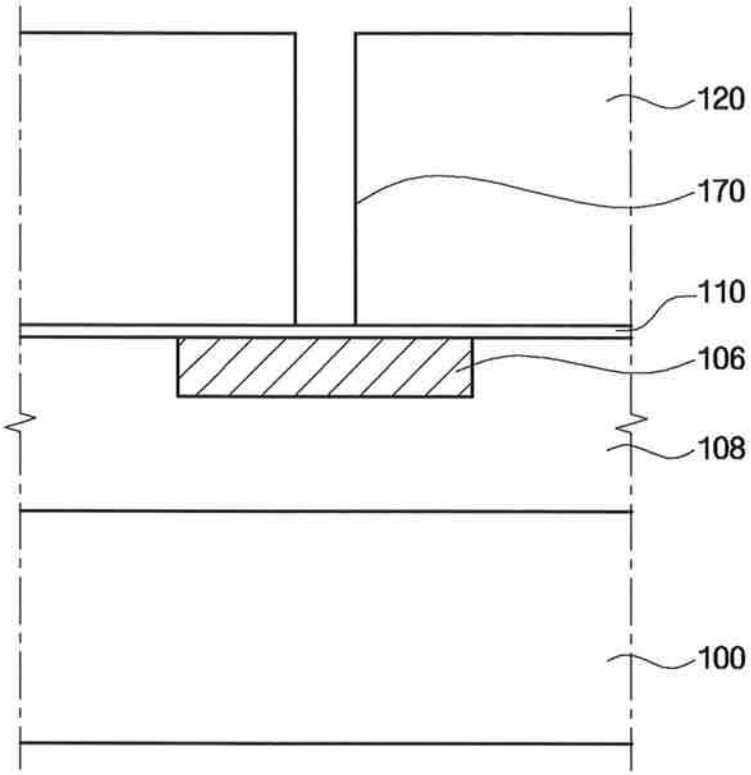


FIG. 2D

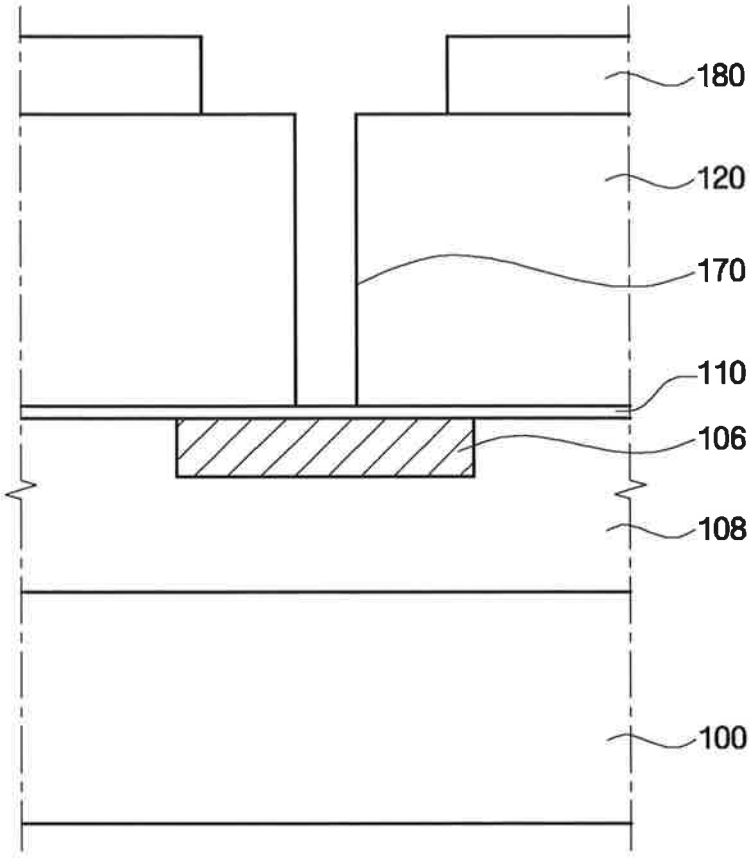


FIG. 2E

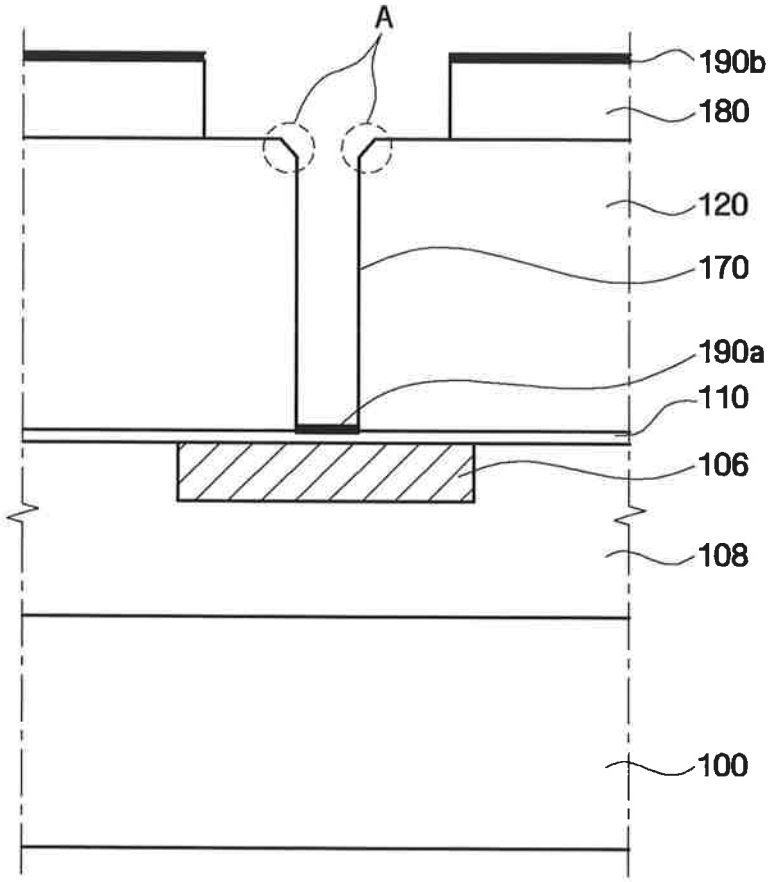


FIG. 2F

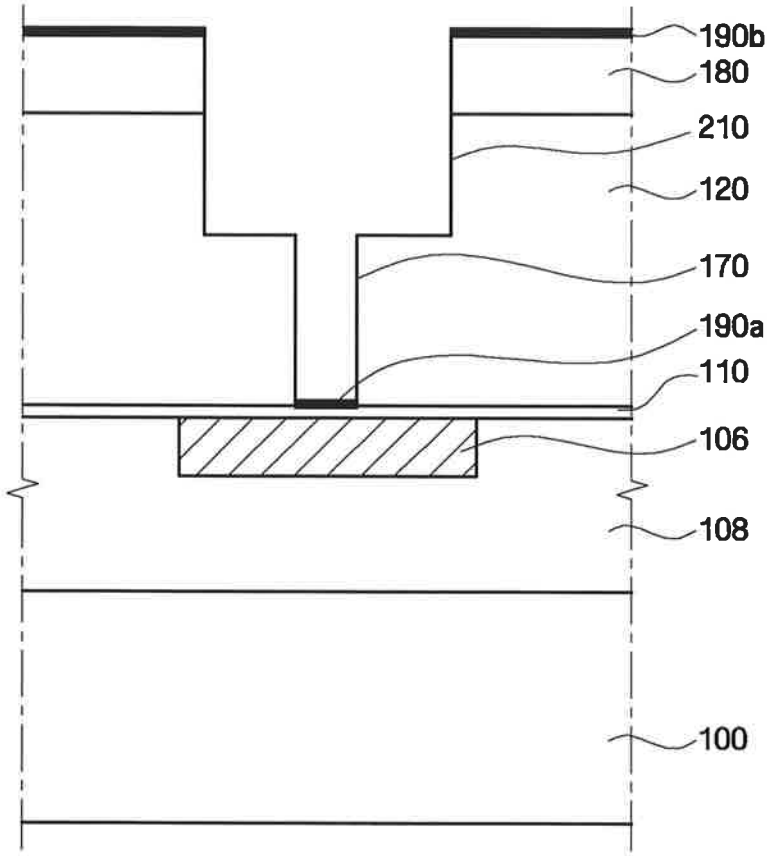


FIG. 2G

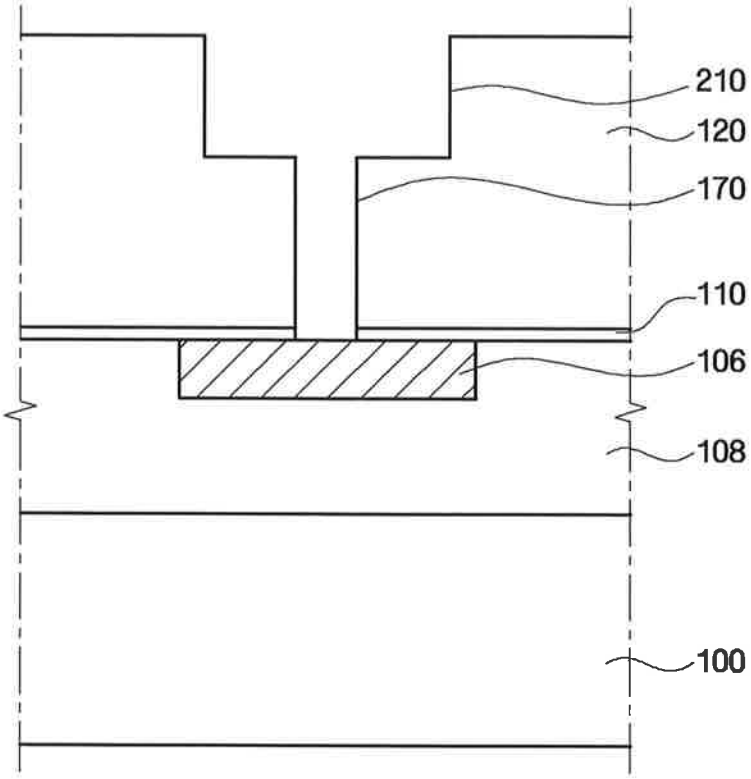


FIG. 2H

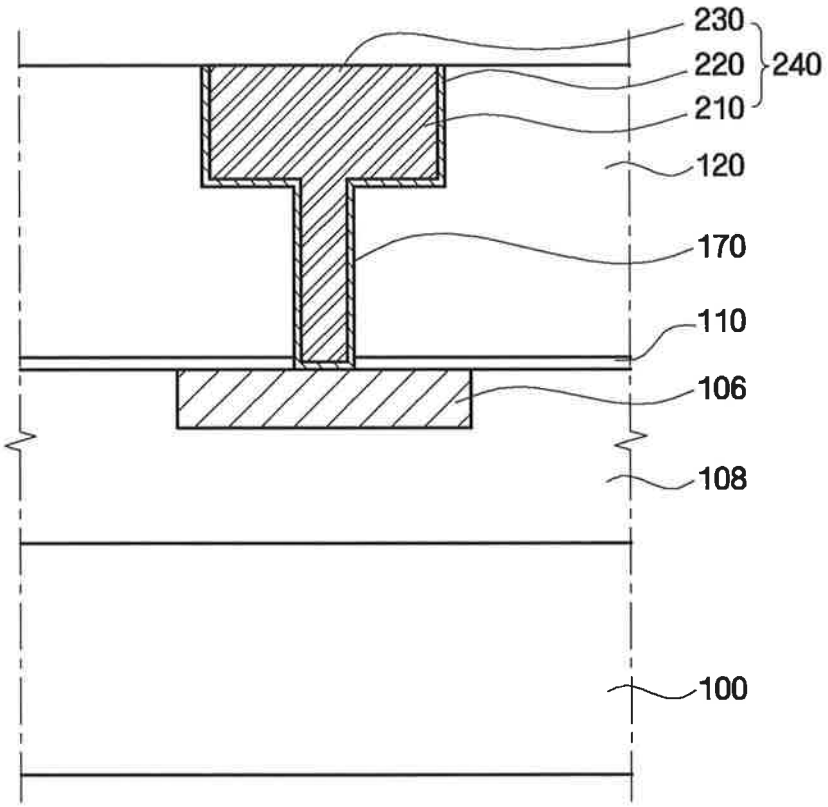


FIG. 3

