INTEGRATION OF SILICON-RICH MATERIAL IN THE SELF-ALIGNED VIA APPROACH OF DUAL DAMASCENE INTERCONNECTS

ABSTRACT

This invention relates to a method of fabrication used for semiconductor integrated circuit devices, and more specifically, in the formation of self-aligned dual damascene interconnects and vias, which incorporates low dielectric constant intermetal dielectrics (IMD) and utilizes silylated top surface imaging (TSI) photoresist, with a single or multi-step selective reactive ion etch (RIE) process, to form trench/via opening. The invention incorporates the use of a silylated top surface imaging (TSI) resist etch barrier layer to form the via pattern, in the first level of a dual damascene process. Two variations of using the top surface imaging (TSI) resist, with and without leaving an exposed region in place, are described in the first and second embodiment of the invention, and in addition, a thin dielectric layer is made use of just below the resist layer. Provided adhesion between the top surface imaging (TSI) photoresist and the low dielectric constant intermetal dielectric (IMD) is good, the thin dielectric layer described above can be omitted, yielding the third and fourth embodiment of the invention. Special attention in the process is given to protecting the integrity of the low dielectric constant intermetal dielectric (ILD) material, selected from the group consisting of organic based or carbon doped silicon dioxide.

Fig. 3