

PATENT SPECIFICATION

(11) 1 267 729

DRAWINGS ATTACHED



- (21) Application No. 50834/69 (22) Filed 16 Oct. 1969
 (31) Convention Application No. 6 815 011 (32) Filed 19 Oct. 1968 in
 (33) Netherlands (NL)
 (45) Complete Specification published 22 March 1972
 (51) International Classification H 04 n 5/08
 (52) Index at acceptance
 H4F D73X D75

(54) TELEVISION SYNCHRONIZING PULSE SEPARATOR

(71) We, PHILIPS ELECTRONIC AND ASSOCIATED INDUSTRIES LIMITED, of Abacus House, 33 Gutter Lane, London, E.C.2, a British Company, do hereby declare the invention, for which we pray that a patent may be granted to us, and the method by which it is to be performed, to be particularly described in and by the following statement:—

The invention relates to a synchronizing pulse separator for a television receiver in which a video signal is applied to an input terminal and in which separated synchronizing pulses occur at an output terminal, the synchronizing pulse separator including an amplitude limiter which employs a transistor having three electrodes a collector of which is coupled to the output terminal of the separator and through a resistor to a supply source and a further electrode of which is connected to a junction of a capacitor and a leakage resistor which form a time constant circuit.

Such a synchronizing separator is known from U.S. Patent Specification 2,890,352 in which steps are proposed in order to be able to satisfactorily separate the line synchronizing pulses from the video signal at a varying peak-to-peak value.

In the circuit arrangement of Figure 1 of the said Patent Specification a base electrode of the *n-p-n*-type transistor is connected to the input terminal of the synchronizing pulse separator through a parallel arrangement of the capacitor and the leakage resistor, which form a circuit having a time constant. An emitter electrode of the transistor is connected to a terminal conveying a bias voltage. In the circuit arrangement of Figure 2 the emitter and base electrodes are interchanged relative to those in Figure 1, while the transistor is of the opposite conductivity type. The terminal conveying a bias voltage is connected to earth through a bypass capacitor not further indicated. In both cases the object of the positive, adjustable bias voltage at the terminal is to give the transistor a fixed, but adjustable threshold voltage.

The amplitude of the line synchronizing pulses to be separated in the video signal ap-

plied to the input terminal comprises a given percentage of the peak-to-peak value of the video signal. For a given amplitude of the video signal and the synchronizing pulses the transistor starts to conduct when the pulses in the video signal exceed a level which is determined by the fixed threshold voltage plus the voltage across the parallel arrangement of the capacitor and the leakage resistor. A further increase has the result that at a second level the transistor is fully bottomed. A still further increase no longer exerts influence on the collector-emitter circuit, but produces a current in the base-emitter circuit which charges the capacitor in the parallel arrangement. Charging takes place as long as the line synchronizing pulse is present and the charge transport is dependent on the pulse amplitude. The capacitor partially discharges across the leakage resistor during the interval between two synchronizing pulses.

It has been achieved that for a varying peak-to-peak value of the video signal and hence of the amplitude of the line synchronizing pulses a bias voltage occurs across the capacitor in the parallel arrangement which voltage varies in conformity therewith and which, in cooperation with the fixed threshold voltage, ensures that the first level at which the transistor is bottomed never lies in the picture content of the video signal. As it were, a strip is clipped from the synchronizing pulses.

It has been stated that the time constant of the parallel arrangement of the capacitor and the leakage resistor may be chosen to be either larger or small. For a small time constant of the order of the repetition period of the line synchronizing pulses the result is a rapid adaptation of the synchronizing pulse separator to variations in the video signal. For obtaining a greater insensitivity to interference it is more advantageous to choose the time constant to be larger.

The known synchronizing pulse separator is described for separating the line synchronizing pulses from the video signal. If both short line synchroniz-

ing pulses and long field synchronizing pulses occur in the video signal, the known separator does not at all function satisfactorily. In fact, the long, rapidly successive field synchronizing pulses occurring during the field synchronizing interval result in the capacitor in the parallel arrangement in the amplitude limiter being charged for a long period and being discharged very little. The capacitor is charged up to the maximum value of the field synchronizing pulses. As a result the clipped strip is shifted towards the peaks of the synchronizing pulses. Interference and noise present across the pulses then directly occurs between the base and the emitter electrode of the transistor. The result is that the interference and noise may switch the transistor on and off during the field synchronizing pulses. Consequently, unwanted pulses upsetting the synchronization of the receiver appear at the output terminal of the separator. In addition there applies that after the field synchronizing interval the capacitor in the amplitude limiter first has to get rid of its superfluous charge before the line synchronizing pulses can be separated again.

It is an object of the invention to obviate the above-mentioned drawbacks.

The invention provides a synchronising pulse separator for a television receiver, the synchronising pulse separator having an input terminal adapted to receive a video signal and an output terminal adapted to provide separated synchronising pulses, the synchronising pulse separator including an amplitude limiter employing a transistor the collector electrode of which is coupled to the output terminal of the separator and is adapted to be coupled through a resistor to a supply source whilst the base electrode of the transistor is connected to the junction of a capacitor and a leakage resistor which forms a time constant circuit, the emitter electrode of said transistor being connected through an ohmic resistance to the input terminal of the separator. The input terminal of the separator may have a DC connection to a video detector from which a video signal may be derived from a negatively modulated carrier. The collector electrode of the first mentioned transistor may be connected to the base electrode of a second transistor whose emitter electrode is connected to a terminal for the supply source for the amplitude limiter the collector and base electrodes of the second transistor each being connected through a resistor to one terminal for a second supply source the other terminal of which is connected to the unsimilar terminal for the supply source for the amplitude limiter, the collector electrode of the second transistor being additionally connected to the output terminal of the separator. With such an arrangement the video

detector may be provided with a direct voltage source supplying a bias voltage, which bias voltage less the voltage drop in the DC connection is substantially equal to the voltage impressed on the collector electrode of the amplitude limiter with the aid of the supply source.

A third transistor connected as an emitter follower may be provided between the input terminal of the separator and the ohmic resistor connected to the emitter electrode of the first transistor. An automatic gain control circuit may be additionally connected to the input terminal of the separator, the automatic gain control circuit being adapted to provide an automatic gain control voltage for the television receiver.

The invention also provides an integrated circuit comprising the components of a synchronising pulse separator according to the invention.

The invention is based on the recognition of the fact that a small time constant can be obtained in the discharge circuit of the capacitor in the amplitude limiter without the noise occurring across the line and field synchronising pulses influencing the synchronization of the television receiver, if a resistive potential divider is incorporated in the emitter-collector circuit of the transistor in the amplitude limiter the transistor being arranged in common base configuration. The potential divider then determines the smallest voltage which may be present across the capacitor, while the noise occurring across the synchronizing pulses cannot influence the operation of the transistor due to the voltage drop across the resistor connected to the emitter of the transistor. The field synchronizing pulses have any noise thereon reduced as are the line synchronizing pulses.

In order that the invention may be readily carried into effect, one embodiment thereof will now be described in detail, by way of example with reference to the accompanying drawing, in which:—

Figure 1 shows a synchronizing pulse separator according to the invention; and

Figure 2 serves to explain the operation of the separator of Figure 1.

Figure 1 shows only that part of a television receiver which is relevant for the description of the synchronizing pulse separator according to the invention.

A signal transmitted by a monochrome or colour television transmitter (not shown) is received by an aerial 1 and processed in a stage 2. Stage 2 may comprise a channel selector which is formed, for example, by an RF amplifier, a mixer and a local oscillator and an IF amplifier for the television signal. The output of the receiver stage 2 is formed by the primary winding 4 of a transformer 3. A television signal 5 is applied

across the primary 4, this television signal 5 being shown as two signals 5_1 and 5_2 . The television signal 5_1 is associated, for example, with the reception of a signal having a large amplitude of the carrier, whilst the television signal 5_2 is associated with a small amplitude of the carrier. The signal is shown as being negatively modulated so that the synchronizing pulses in the television signal 5 occur at the maximum carrier level, while a maximum modulation of the carrier has ten per cent of the carrier amplitude.

Transformer 3 is provided with a secondary 6 which is connected to the series arrangement of a diode 7 and a parallel arranged resistor 8 and capacitor 9. The cathode of diode 7 is connected to the secondary 6, while the anode is connected to the base electrode of a transistor 10 connected as an emitter follower. The emitter electrode of transistor 10 is connected to earth through a resistor 11. The end of the winding 6 remote from the diode 7 is connected to one terminal of a direct voltage source V_0 conveying a positive constant potential $+V_0$, the other terminal of which is connected to earth. By detection with the aid of the video detector including the components 7, 8 and 9, a video signal 12 present across resistor 11 is obtained from the television signal 5 which video signal occurs at terminals 13 and 14 and is shown near terminal 13. In conformity with the television signal 5 the video signal 12 is also shown as two signals 12_1 and 12_2 which lie between the level indicated by the potential $+V_0$ and the earth potential 0. The signals 12_1 and 12_2 shown for approximately one line period each comprise a synchronizing part having line synchronizing pulses at an amplitude of 25% of the maximum peak-to-peak value, while the remaining part between 30 and 100% represents the picture content.

The video signal 12 occurring at terminal 13 is available for further handling in the television receiver and may be applied, for example, to a video amplifier. Terminal 14 is connected to an input of an automatic gain control (AGC) circuit 15 an output of which is connected to the receiver stage 2 for providing a control voltage. A variable resistor 16 is shown to indicate that the adjustment of the AGC circuit 15 can be varied.

Starting from the fact that with a given reception the television signal 5_1 is provided by the stage 2, it can be assumed that the weakened television signal 5_2 occurs if either the received signal is greatly weakened, for example, by atmospheric circumstances so that AGC circuit 15 cannot sufficiently readjust the signal level, or the control level of circuit 15 is shifted with the aid of resistor 16. It appears from the signals 12_1 and 12_2 that the highest possible value is determined by a level $+V_0$, which is given

by the level of potential $+V_0$ minus the voltage drop across the base-emitter junction of the transistor 10. In the case of the satisfactorily operation AGC circuit 15, the variable resistor 16 may be used for adjusting the contrast in the video signal 12.

Terminal 14 is also the input terminal of a synchronizing pulse separator according to the invention. The separator is provided with an amplitude limiter employing a transistor 17 the base electrode of which is connected to the junction of the series arrangement of a capacitor 18 and a leakage resistor 19, which series arrangement is provided between a terminal conveying the potential $+V_0$ and earth. A terminal conveying a positive potential $+V_1$ of a supply source V_1 is connected through a resistor 20 to the collector electrode of the transistor 17. The emitter electrode of transistor 17 is connected through a resistor 21 to the input terminal 14 of the separator. The separator thus includes an amplitude limiter which is built up from the transistor 17 arranged in common base configuration, the capacitor 18 and the resistors 19, 20 and 21. The resistor 19 and the capacitor 18 form a time constant circuit. Capacitor 18 in the amplitude limiter may alternatively be connected in parallel with resistor 19.

The collector electrode 17 is connected to the base electrode of a further transistor 22. A supply source V_2 is connected in series with the supply source V_1 such that the terminal $+V_1$ is connected to the terminal $-V_2$. The emitter electrode of transistor 22 is connected to the terminal conveying the potential $+V_1$ of the supply source V_1 , while the collector electrode is connected through a resistor 23 to the terminal conveying a potential $V_1 + V_2$ of the supply source V_2 . The terminal of source V_2 conveying the potential $V_1 + V_2$ is also connected through a resistor 24 to the base electrode of the transistor 22 and is directly connected to the collector electrode of the transistor 10. The collector electrode of the transistor 22 is connected to a terminal 25 which serves as an output terminal of the separator.

To explain the operation of the separator and to illustrate the manner in which the separator also operates satisfactorily in case of a greatly weakened television signal 5. Figure 1 shows the signals occurring at different points in the circuits. In conformity with the television signal 5, the other signals are also divided and denoted by the indices 1 and 2. The potential at the junction of resistor 19 and capacitor 18 is denoted by signal 26. The potential at the collector electrode of the transistor 17 is denoted by the signal 27. Whilst the synchronizing pulses occurring at the output terminal 25 are denoted by the signal 28.

The synchronizing pulses in the video signal 12 cause the transistor 17 to be bottomed during the pulse period when the signal level of the pulse is below the voltage set by the capacitor 18 at the base electrode of that transistor. Transistor 17 serves as a switch which connects resistor 21 both in parallel with capacitor 18 and in series with the resistor 20. Capacitor 18 is discharged across the resistor 21 so that a potential decreasing during the synchronizing pulse period is shown in both signal 26 and in signal 27. The bottoming of transistor 17 results in the bottomed transistor 22 being immediately cut off. Transistor 22 operates as a switch so that a pulse occurs in signal 28 which lies between the potentials $+V_1$ and $V_1 + V_2$. The transistor 17 is cut off at the end of the synchronizing pulse in the video signal 12. Transistor 22 is then bottomed during which time the base electrode of transistor 22 and the collector electrode of transistor 17, due to the voltage division across the resistors 24 and 20, acquire a potential which is denoted by the level $+V_2$ in the signal 27 being the same level as in signal 12. The capacitor 18 will be charged through the load resistor 19 as is shown by an increasing potential in signal 26.

It is found that separated synchronizing pulses having a constant amplitude occur at the output terminal 25 independently of a video signal 12, or 12₂. A second effect for which transistor 22 may be used is the elimination of the influence of the voltage drop across the base-emitter junction of transistor 10 on the level in the synchronizing pulses in the video signal 12, at which level the transistor 17 is bottomed. To this end the potential $+V_2$ as denoted in signal 27 is impressed on the collector electrode of the normally cut-off transistor 17 with the aid of the transistor 22. The result is that signal 27 (27₁, 27₂) shows pulses the amplitude of which is proportional to the amplitude of the video signal 12 (12₁, 12₂) and hence to the amplitude of the carrier in the television signal 5 (5₁, 5₂). The same applies to the voltage drop across the resistor 21 which is so large that the noise present across the pulses in the video signal 12 has no influence on the conduction of transistor 17. The said proportion results in the transistor 17 being bottomed always at the same percentage of the carrier amplitude of, for example, 8% independently of the magnitude of the synchronizing pulse in the signals 12₁ and 12₂ which amounts to, for example, 25% of the carrier amplitude. The result is that the separation of the synchronizing pulses from the video signal 12 commences at a fixed percentage from the peaks of the pulses so that the separator can never be active in the picture content of the video signal 12.

If the voltage ($V_0 - V_2$) across the base-

emitter junction of the transistor 10 when formed of germanium instead of silicon is negligibly small relative to the smallest value of the carrier, then the described second effect can be obtained without using transistor 22 by connecting the collector electrode of transistor 17 directly to the output terminal 28. If transistor 17 is likewise formed of germanium, resistors 19 and 20 can be connected to a terminal of potential $+V_0$. If on the other hand transistor 17 is a silicon transistor, resistor 20 is to be connected to a terminal of potential V_0 and resistor 19 is to be connected to a terminal of potential V_0 and resistor 19 is to be connected to a terminal conveying a potential of V_0 plus the base-emitter threshold voltage of transistor 17.

For obtaining information regarding the amplitude of the negatively modulated carrier, it is necessary that a DC connection exists between the video detector (7, 8, 9) and the input terminal 14 of the separator. If this were not the case, this information which is given relative to the potential $+V_0$ is lost due to, for example, a capacitive connection and cannot thereafter be extracted from the capacitively transmitted signal. A direct current or direct voltage amplifier can of course be included in the DC connection.

Figure 2 serves to explain the operation of the separator of Figure 1, when a few, for example, five field synchronizing pulses occur in the received television signal during the field synchronizing interval. The signal 27 shown in Figure 1 is shown by the thick lines in Figure 2. The potential denoted by V_{18} is that which occurs at the base electrode of the transistor 17 and corresponds to the signal 26 of Figure 1. The difference between the level of potential $+V_1$ and potential V_{18} occurring during the line synchronizing pulse is denoted by U_{20} so that U_{20} represents the voltage which is present across the resistor 20. The voltage drop across resistor 21 is signal 27 and the pulses shown by the thin lines denoted by U_{21} so that the combination of lines represents that portion of the video signal 21 applied to the input terminal 14 which causes the transistor 17 to be bottomed. The presence of noise on the pulses shown in thin lines is indicated by means of an undulating line. It is found that the peaks of the synchronizing pulses in the video signal 12 are reduced by resistor 21.

Figure 2 also shows a signal 27₁ in thick lines which occurs at the collector electrode of transistor 17 if the field-synchronizing signal 12 applied to the input terminal 14 of the separator. The potentials $+V_2$, $+V_1$ and V_{18} and the voltage U_{20} are again shown in the signal 27₁. As in signal 27 described above, a voltage drop U_{21} occurs across resistor 21.

Starting from the fact that the potential V_{1s} at the commencement of the first field synchronizing pulse has a value which is equal to the value of V_{1s} at the commencement of a line synchronizing pulse in signal 27 of Figure 2, then the potential V_{1s} , due to the longer duration of the field synchronizing pulse, will have greatly decreased at the end of the first pulse thereof. Capacitor 18 will only receive a very small charge in the short period between the first and the second field synchronizing pulse so that the potential V_{1s} remains substantially constant. The same effect occurs for the second field synchronizing pulse. At the third field synchronizing pulse V_{1s} reaches a level which is indicated by a dot-and-dash line. This level is determined relative to the potential $+V_1$ by the voltage division across the resistors 20 and 21 as is shown by R_{20} and R_{21} in Figure 2. It is found that the potential V_{1s} cannot decrease any further due to this resistive voltage division. The result is that the noise reduction action of the resistor 21 is also ensured when the field synchronizing pulses occur so that the noise occurring on the pulse peaks cannot at all exert an influence on the satisfactory operation of the separator.

If a television receiver provided with a synchronizing pulse separator according to the invention receives a positively modulated carrier, the receiver should include a converter stage so as to convert the received signal into a pseudo-negatively modulated signal.

The separator according to the invention may be integrated in a simple manner in a semiconductor body i.e. formed as an integrated circuit, to which for example, the capacitor 18 and resistor 19 formed as discrete components can be connected. A monolithically integrated separator can thus be obtained in a simple manner.

The separator may include a stage to which interference pulses separated from the video signal 12 are applied so that the separator remains inactive at the occurrence thereof. To this end a transistor could be provided between resistor 11 and earth, which transistor is cut off during the occurrence of interference pulses.

The values of some components for a practical embodiment employing silicon transistors may be:

	direct voltage	
	source V_0	= 5 V.
	capacitor 18	= 0.01 μ F
	resistor 19	= 200 k. Ohms
60	resistor 20	= 5 k. Ohms
	resistor 21	= 400 Ohms

It is found that in such a practical embodiment a very small time constant at a value

of 4 μ s can be realized in the discharge circuit of the capacitor 18 without jeopardizing the satisfactory operation of the separator. In the given embodiment the voltage across the capacitor 18 reaches the value determined by the potential divider formed by the resistors 20 and 21 already during the first field synchronizing pulse.

WHAT WE CLAIM IS:—

1. A synchronising pulse separator for a television receiver, said synchronising pulse separator having an input terminal adapted to receive a video signal and an output terminal adapted to provide separated synchronising pulses, said synchronising pulse separator including an amplitude limiter employing a transistor the collector electrode of which is coupled to said output terminal of the separator and is adapted to be coupled through a resistor to a supply source whilst the base electrode of said transistor is connected to the junction of a capacitor and a leakage resistor which forms a time constant circuit, the emitter electrode of said transistor being connected through an ohmic resistance to the input terminal of said separator.

2. A synchronising pulse separator as claimed in Claim 1, in which the input terminal of said separator has DC connection to a video detector from which a video signal may be derived from a negatively modulated carrier.

3. A synchronising pulse separator as claimed in Claim 1 or 2, in which the collector electrode of said first mentioned transistor is connected to the base electrode of a second transistor whose emitter electrode is connected to a terminal for the supply source for said amplitude limiter, the collector and base electrodes of said second transistor each being connected through a resistor to one terminal for a second supply source the other terminal of which is connected to the unsimilar terminal for the supply source for said amplitude limiter, the collector electrode of said second transistor being additionally connected to the output terminal of said separator.

4. A synchronising pulse separator as claimed in Claim 2 or Claim 3 when dependent upon Claim 2, said video detector is provided with a direct voltage source supplying a bias voltage, which bias voltage less the voltage drop in the said DC connection is substantially equal to the voltage impressed on the collector electrode of said amplitude limiter with the aid of the supply source.

5. A synchronising pulse separator as claimed in Claim 1, 2, 3, or 4, in which between the input terminal of said separator and the ohmic resistor connected to the emitter electrode of said first transistor is

Starting from the fact that the potential V_{18} at the commencement of the first field synchronizing pulse has a value which is equal to the value of V_{18} at the commencement of a line synchronizing pulse in signal 27 of Figure 2, then the potential V_{18} , due to the longer duration of the field synchronizing pulse, will have greatly decreased at the end of the first pulse thereof. Capacitor 18 will only receive a very small charge in the short period between the first and the second field synchronizing pulse so that the potential V_{18} remains substantially constant. The same effect occurs for the second field synchronizing pulse. At the third field synchronizing pulse V_{18} reaches a level which is indicated by a dot-and-dash line. This level is determined relative to the potential $+V_1$ by the voltage division across the resistors 20 and 21 as is shown by R_{20} and R_{21} in Figure 2. It is found that the potential V_{18} cannot decrease any further due to this resistive voltage division. The result is that the noise reduction action of the resistor 21 is also ensured when the field synchronizing pulses occur so that the noise occurring on the pulse peaks cannot at all exert an influence on the satisfactory operation of the separator.

If a television receiver provided with a synchronizing pulse separator according to the invention receives a positively modulated carrier, the receiver should include a converter stage so as to convert the received signal into a pseudo-negatively modulated signal.

The separator according to the invention may be integrated in a simple manner in a semiconductor body i.e. formed as an integrated circuit, to which for example, the capacitor 18 and resistor 19 formed as discrete components can be connected. A monolithically integrated separator can thus be obtained in a simple manner.

The separator may include a stage to which interference pulses separated from the video signal 12 are applied so that the separator remains inactive at the occurrence thereof. To this end a transistor could be provided between resistor 11 and earth, which transistor is cut off during the occurrence of interference pulses.

The values of some components for a practical embodiment employing silicon transistors may be:

direct voltage	
source V_0	= 5 V.
capacitor 18	= 0.01 μ F
resistor 19	= 200 k. Ohms
resistor 20	= 5 k. Ohms
resistor 21	= 400 Ohms

It is found that in such a practical embodiment a very small time constant at a value

of 4 μ s can be realized in the discharge circuit of the capacitor 18 without jeopardizing the satisfactory operation of the separator. In the given embodiment the voltage across the capacitor 18 reaches the value determined by the potential divider formed by the resistors 20 and 21 already during the first field synchronizing pulse.

WHAT WE CLAIM IS:—

1. A synchronising pulse separator for a television receiver, said synchronising pulse separator having an input terminal adapted to receive a video signal and an output terminal adapted to provide separated synchronising pulses, said synchronising pulse separator including an amplitude limiter employing a transistor the collector electrode of which is coupled to said output terminal of the separator and is adapted to be coupled through a resistor to a supply source whilst the base electrode of said transistor is connected to the junction of a capacitor and a leakage resistor which forms a time constant circuit, the emitter electrode of said transistor being connected through an ohmic resistance to the input terminal of said separator.

2. A synchronising pulse separator as claimed in Claim 1, in which the input terminal of said separator has DC connection to a video detector from which a video signal may be derived from a negatively modulated carrier.

3. A synchronising pulse separator as claimed in Claim 1 or 2, in which the collector electrode of said first mentioned transistor is connected to the base electrode of a second transistor whose emitter electrode is connected to a terminal for the supply source for said amplitude limiter, the collector and base electrodes of said second transistor each being connected through a resistor to one terminal for a second supply source the other terminal of which is connected to the unsimilar terminal for the supply source for said amplitude limiter, the collector electrode of said second transistor being additionally connected to the output terminal of said separator.

4. A synchronising pulse separator as claimed in Claim 2 or Claim 3 when dependent upon Claim 2, said video detector is provided with a direct voltage source supplying a bias voltage, which bias voltage less the voltage drop in the said DC connection is substantially equal to the voltage impressed on the collector electrode of said amplitude limiter with the aid of the supply source.

5. A synchronising pulse separator as claimed in Claim 1, 2, 3, or 4, in which between the input terminal of said separator and the ohmic resistor connected to the emitter electrode of said first transistor is



provided a third transistor connected as an emitter follower.

- 5 6. A synchronising pulse separator as claimed in any of the preceding claims, in which an automatic gain control circuit is additionally connected to the input terminal of said separator, said automatic gain control circuit being adapted to provide an automatic gain control voltage for said television receiver.

- 10 7. A synchronising pulse separator for a television receiver substantially as herein described with reference to the accompanying drawing.

- 15 8. An integrated circuit comprising the components of a synchronising pulse separator as claimed in any of the preceding claims with the exception of the capacitor of said time constant circuit.

- 20 9. In combination an integrated circuit

as claimed in Claim 9 and said time constant capacitor.

10. An integrated circuit comprising the components of a synchronising pulse separator as claimed in any of the preceding claims 1 to 7 with the exception of the resistor and capacitor of said time constant circuit.

11. In combination an integrated circuit as claimed in Claim 10 and the resistor and capacitor of said time constant circuit.

12. A television receiver provided with a synchronising pulse separator as claimed in any of the preceding claims 1 to 7.

C. A. CLARK,
Chartered Patent Agent,
Century House,
Shaftesbury Avenue,
London, W.C.2,
Agent for the Applicants.

Printed for Her Majesty's Stationery Office by Burgess & Son (Abingdon), Ltd.—1972
Published at The Patent Office, 25 Southampton Buildings, London, WC2A 1AY,
from which copies may be obtained.



* C L M S *