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PATENT SPECIFICATION

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(54) DIGITAL MULTI-ALARM WATCH

(71) We, KABUSHIKI KAISHA DAINI SEIKOSHA, a Japanese Company of 31—1 6-chome, Kameido, Koto-ku, Tokyo, Japan, do hereby declare the invention for which we pray that a patent may be granted to us and the method by which it is to be performed to be particularly described in and by the following statement:

This invention relates to digital multi-alarm watches.

According to the present invention there is provided a digital multi-alarm watch comprising a plurality of memory circuits each arranged to memorise a respective alarm time; timekeeping means for producing an actual time of day indication; comparison means for selectively comparing the alarm time memorised by each memory circuit with the actual time of day indication; a ring counter for causing the contents of the memory circuits to pass in turn to the comparison means, and warning means for producing an indication when the alarm time compared by the comparison means coincides with the actual time of day indication.

The watch may include alarm time setting means connected to the memory circuits for selectively setting alarm times therein.

Preferably the watch includes display means for selectively displaying the alarm time memorised by the memory circuits, and the actual time of day indication produced by the timekeeping means.

The comparison means may be an EX—OR circuit.

The watch, in the preferred embodiment includes terminating means for terminating at the end of a predetermined time, the indication given by the warning means when the alarm time compared by the comparison means coincides with the actual time of day indication. The terminating means may be a set-reset flip-flop.

The invention is illustrated, merely by way of example, in the accompanying drawings in which:

Figure 1 is a block diagram of one embodiment of a digital multi-alarm watch

according to the present invention; and

Figure 2 is a timing chart illustrating the operation of the digital multi-alarm watch of Figure 1.

Referring first to Figure 1 there is illustrated one embodiment of a digital multi-alarm watch according to the present invention. In Figure 1 only the pre-setting of the minutes of an alarm time is described, but it will be appreciated that similar arrangements may be provided to pre-set also seconds and/or hours of the alarm time. More usually, the minutes and hours of an alarm time would be preset. The watch includes a crystal controlled oscillator and frequency dividing circuit 1 for producing a standard time signal, a seconds counter, and a minutes counter 3 connected in series. An alarm time setting circuit 4 produces output signals which are fed to respective inputs of a first memory circuit or channel 5, a second memory circuit or channel 6 and a third memory circuit or channel 7 of an alarm time counter.

An output signal from the oscillator and frequency divider circuit 1 is fed to a ring counter 15. An output terminal 15a of the ring counter 15 forms one input of an AND circuit 8a the other input of which is an output signal from channel 5. An output terminal 15b of the ring counter 15 forms one input of an AND circuit 8b the other input of which is an output signal from channel 6. An output terminal 15c of the ring counter 15 forms one input of an AND circuit 8c the other input of which is an output signal from the channel 7. Output signals from the AND circuits 8a, 8b, 8c form inputs of an OR circuit 9 and an output signal from the OR circuit 9 forms one input of an EX—OR circuit 10, the other input of which is an output signal from the minutes counter 3. The output signal from the minutes counter 3 also forms one input of a display change-over circuit 16, the other three inputs of which being the output signals from channels, 5, 6, 7. The change-over circuit 16 is conditioned by an output signal from the alarm time setting circuit 4

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so that a selected one of the four inputs is fed to a decoder/driver 17 which drives a display device 18.

5 An output signal from the EX—OR circuit 10 is inverted by an inverter 11 and applied to a set terminal of a set-reset flip-flop 12. A reset terminal of a flip-flop 12 is connected to receive an output signal from the seconds counter 2. An output terminal Q of the flip-
10 flip 12 is connected to a sound generating driver 13. When the output signal at the output terminal Q of the flip-flop 12 is logical one, a driver 13 is energised to drive a sound generator 14.

15 Different alarm times set in the channels 5, 6, 7 are memorised therein as follows. Initially the channel 5 is brought into a settable condition by means of the alarm time setting circuit 4. At the same time, the
20 changeover circuit 16 passes only the contents of the channel 5 so that the contents are displayed by the display device 18. The contents of the channel 5 are then set to a desired alarm time by means of the alarm
25 time setting circuit 4. A respective desired alarm time is set in each channel 6, 7 in a similar manner. After the desired alarm times have been set, the output signals at the output terminals 15a, 15b, 15c of the ring
30 counter 15 are made successfully logical one by pulses from the oscillator and frequency divider circuit 1. When the output signal at the output terminal 15a is logical one the AND circuit 8a in ON to feed the contents of
35 the channel 5 to the OR circuit 9. This time the other output signals of the ring counter 15 are logical 0 so that the AND circuit 8b, 8c are OFF so that the contents of the channel 6, 7 are not fed to the OR circuit 9.

40 The contents of the channel 5 are passed through the OR circuit 9 and are compared to the contents of the minutes counter 3 by the EX—OR circuit 10. When both the contents of the channel 5 and the contents
45 of the minutes counter 3 coincide that is at the alarm time, the output signal from the EX—OR circuit 9 becomes logical 0 so that the output signal from the inverter 11 is logical one and the output terminal Q logical
50 flip-flop 12 become logical one. This causes the sound generating driver 13 to be energised whereby the sound generator is driven so as to produce a sound to indicate that the alarm time has been reached. In
55 order automatically to de-energise the sound generating driver 13 so that the sound made by the sound generator 14 ceases, a signal from the seconds counter 2 is fed to the reset terminal of the flip-flop 12 after a
60 predetermined time which is preferably between 5 and 30 seconds, to make the output signal of the output terminal Q logical 0 so as to de-energise the sound generating driver 13.

65 When the contents of the minutes counter

3 and the channel 5 do not coincide the output signal from the EX—OR circuit 10 is logical one so that the output signal from the inverter 11 is logical 0. This causes the output signal at the output terminal Q of flip-flop 12 to be kept at logical 0 with the result that the sound generating driver 13 is not energised.

When the output signal of the output terminals 15a 15c of the ring counter 15 are logical 0 and the output signal of the output terminal 15b is logical 8, the AND circuit 8b passes the contents of the channel 6 to the OR circuit 9 whilst the AND circuits 8a, 8c block the contents of the channels 5, 7. In a manner similar to that described above, the contents of the channel 6 are compared by the EX—OR circuit 10 with the contents of the minutes counter 3 and the sound generating driver 13 is energised when coincidence occurs.

In a similar manner, when the output signals at the output terminals 15a 15b are logical 0 and the output signal of the terminal 15c of the ring counter 15 is logical 1, the contents of the channel 7 are passed to the OR circuit 9 by the AND gate 8c whilst the contents of the channels 5, 6 are blocked by the AND circuits 8a, 8b. The contents of the channel 7 are compared by the EX—OR circuit 10 with the contents of the minutes counter 3 and the sound generating driver 13 is energised when coincidence occurs.

The ring counter 15, by virtue of the output signal it receives from the oscillator and frequency dividing circuit 1 causes an output signal of logical one to appear at the output terminals 15a, 15b, 15c in turn, so that the EX—OR circuit 10 compares the contents of the minutes counter 3 with the contents of the channels, 5, 6, 7 in turn.

Figure 2 is a time chart illustrating the operation of the digital multi-alarm watch of Figure 1. A wave form 20 represents the output signal derived from the oscillator and frequency dividing circuit 1 and applied to the ring counter 15. This output signal may have a frequency between 256Hz and 2Hz. A wave form 21 represents the output signal of the output terminal 15a of the ring counter when the contents of channel 5 are compared to the contents of the minutes counter 3 by the EX—OR circuit 10. Similarly, wave-forms 22, 23 represent the output signals of the output terminals 15b, 15c when the contents of the channels 5, 6 are respectively compared to the contents of the minutes counter 3 by the EX—OR circuit 10. A wave form 24 represents the output signal from the EX—OR circuit 10 when the contents of the channel 6 coincides with the contents of the minutes counter 3. A wave form 25 represents the output signal from the flip-flop 12 when the output signal from the EX—OR circuit 10 is

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as illustrated by wave form 24.

The above described digital multi-alarm watch has only one comparison circuit i.e. the EX—OR circuit 10 serving all three channels, 5,6,7 so that it is very advantageous to manufacture the watch from integrated circuitry.

Having regard to the provision of Section 9 of the Patents Act 1949, we direct attention to our Patent No. 1 372 620.

WHAT WE CLAIM IS:—

1. A digital multi-alarm watch comprising; a plurality of memory circuits each arranged to memorise a respective alarm time; time keeping means for producing an actual time of day indication; comparison means for selectively comparing the alarm time memorised by each memory circuit with the actual time of day indication; a ring counter for causing the contents of the memory circuits to pass in turn to the comparison means; and warning means for producing an indication when the alarm time compared by the comparison means coincides with the actual time of day indication.

2. A watch as claimed in claim 1 including alarm time setting means connected to the memory circuits for selectively setting alarm times therein.

3. A watch as claimed in claim 1 or 2 including display means for selectively displaying the alarm time memorised by the memory circuits, and the actual time of day indication produced by the time keeping means.

4. A watch as claimed in any preceding claim in which the comparison means is an EX—OR circuit.

5. A watch as claimed in any preceding claim including terminating means for terminating at the end of a predetermined time, the indication given by the warning means when the alarm time compared by the comparison means coincides with the actual time of day indication.

6. A watch as claimed in claim 5 in which the terminating means is a set re-set flip-flop.

7. A digital multi-alarm watch substantially as herein described with reference to and as shown in the accompanying drawings.

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