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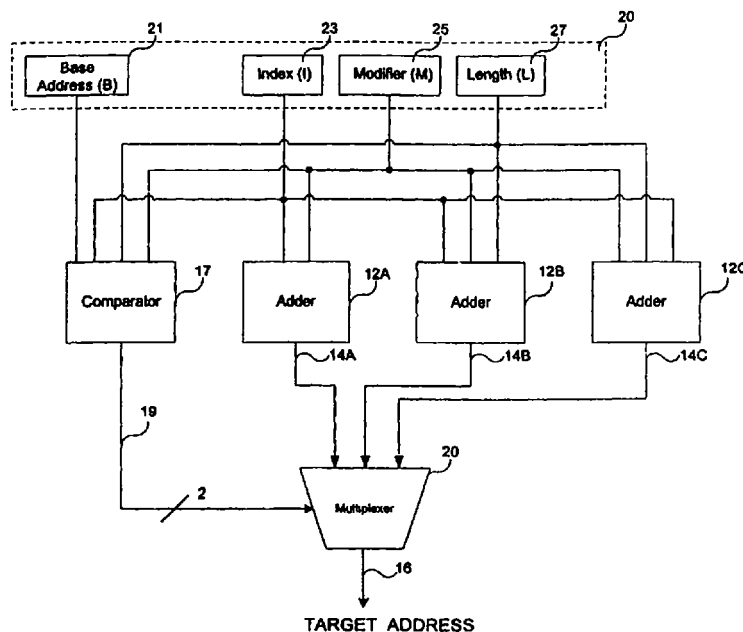
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(54) Title: MODULO ADDRESSING



(57) Abstract: In one embodiment, a modulo addressing unit for a processor is described that includes a plurality of adders to generate an uncorrected target modulo address and at least one corrected target modulo address in parallel. A comparator selects one of the target modulo addresses a function of a base address (b) for a circular buffer, a length (L) of the circular buffer, an index address (I) and a modifier value (M). In one embodiment the comparator selects a first corrected target modulo address when $I+M < B$, a second corrected target modulo address when $I+M \geq B+L$ and an uncorrected modulo address $B \leq I+M < B+L$.