METHOD FOR REDUCING SUBSTRATE CAPACITIVE COUPLING OF A THIN FILM INDUCTOR BY REVERSE P/N JUNCTIONS

ABSTRACT

A method for reducing the capacitive coupling of an inductor on an integrated circuit chip is described. The method forms the inductor over an accumulation of dielectric layers used elsewhere in the integrated circuit. In addition two back-to-back reversed p/n junctions are formed within the silicon substrate below the inductor. The junctions are serially connected and, along with the capacitance of the dielectric layers, reduce the capacitive coupling of the inductor to the substrate by a factor of between about 2 and 20 over the that of the dielectric layers alone. The decrease in capacitance improves the performance of the inductor at high operating frequencies, for example, above1 GHz. The junctions are easily formed in a twin-well CMOS circuit by the addition of only a single additional processing step. The additional step comprises the deep implantation of phosphorous to form an n-type zone between the p-well and the substrate in the region over which the inductor is formed. The junctions are not externally biased and sustain continuous depletion regions between the inductor and the substrate.

(FIGURE 3A IS SUGGESTED FOR PUBLICATION)