structure can also use bond wires, stud bump, micro bump, or other electrical interconnect.

In FIG. 4i, a portion of encapsulant 154 is removed ~~by~~ by laser direct ablation (LDA) using laser 202 to form openings or vias 200 extending down to conductive layer 172 of interconnect structure 168. Alternatively, openings 200 can be formed by an etching process through a patterned photoresist layer. Openings 200 have a tapered shape including a larger diameter at the top of opening 200 and a smaller diameter at the bottom of opening 200. The tapered via shape enables stable solder ball loading when inserting bump material 206 into opening 200. The tapered via shape also provides stable bump material heights for uniform PoP stacking. After openings 200 are formed, openings 200 and exposed conductive layer 172 are cleaned. A residue free surface of conductive layer 172 provides improved solder wetting and electrical continuity for PoP stacking.

FIG. 4j shows a plan view of composite substrate 156 after removal of a portion of encapsulant 154. Semiconductor die 124 is surrounded and covered by encapsulant 154. Openings 200 are formed around semiconductor die 124 in encapsulant 154. Openings 200 extend down to surface 178 of conductive layer 172 and include tapered sidewalls. The tapered sidewalls of opening 200 are based on larger top diameter and smaller bottom diameter that helps to achieve stable solder ball loading during solder filling and stable solder heights for uniform PoP stacking.

In FIG. 4k, an electrically conductive bump material 206 is deposited over opening 200 above the exposed conductive layer 172 using an evaporation, electrolytic plating, electroless plating, ball drop, or screen printing process. The bump material can be Al, Sn, Ni, Au, Ag, Pb, Bi, Cu, solder, and

combinations thereof, with an optional

flux solution. For example, the bump material can be eutectic Sn/Pb, high-lead solder, or lead-free solder. ~~The bump material is bonded to conductive layer 172 using a suitable attachment or bonding process~~.

In FIG. 4l, the bump material is reflowed by heating the material above its melting point to form balls or bumps 208 over surface 178 of conductive layer 172. ~~and~~ Bumps 208 are recessed within opening 200 to bond with conductive layer 172. In some applications, bumps 208 are reflowed a second time to improve electrical contact to conductive layer 172. Bumps 208 can also be compression bonded or thermocompression bonded to conductive layer 172. Bumps 208 represent one type of interconnect structure that can be formed over conductive layer 172. The interconnect structure can also use stud bump, micro bump, or other electrical interconnect. When an upper package is stacked over the lower package 220 to form a PoP device, the portion of opening 200 above interconnect 208 reduces the height of the PoP device by connecting the top and bottom packages within opening 200. The smaller package profile of semiconductor device 250 improves the thermal performance, electrical performance, and warpage behavior the semiconductor device by creating a thin, 3D PoP eWLB device.

After the formation of bumps 208, composite substrate or reconstituted wafer 156 is singulated with saw blade or laser cutting device 218 into individual semiconductor devices 220 in FIG. 4m. By singulating composite substrate 156 before mounting additional semiconductor devices over the composite substrate, the formation of individual semiconductor devices 220 is accomplished by mounting the additional semiconductor die at the individual device level rather than at the reconstituted wafer level. Alternatively, composite

substrate 156 is singulated after additional semiconductor devices are mounted to the

Claims

What is claimed:

1. A method of making a semiconductor device, comprising:

providing a semiconductor die;

depositing an encapsulant over and around the semiconductor die including a first surface of the encapsulant coplanar with an active surface of the semiconductor die;

planarizing the encapsulant to form a planar second surface of the encapsulant opposite the first surface of the encapsulant;

forming an interconnect structure ~~over~~ under the ~~a~~ first surface of the encapsulant and in physical contact with the active surface of the semiconductor die after depositing the encapsulant;

forming an opening from ~~a~~ the planar second surface of the encapsulant extending to and terminating at ~~to~~ the first surface of the encapsulant ~~to expose a surface of the interconnect structure~~ coplanar with the active surface of the semiconductor die; ~~and~~

~~forming a bump recessed within the opening and disposed over the surface of the interconnect structure~~

depositing a bump material over the opening of the encapsulant; and

reflowing the bump material to form a bump recessed within the opening and contacting the interconnect structure.

2. The method of claim 1, further including:

providing a semiconductor package; and

disposing the semiconductor package over the ~~second surface of the~~ encapsulant and electrically connecting the semiconductor package to the bump.

3. The method of claim ~~2~~1, further including forming a plurality of~~ interconnect structures over the semiconductor package to electrically connect the semiconductor package to the bump~~ bumps under the interconnect structure.

4. The method of claim 2, wherein the semiconductor package includes a memory device.

5. The method of claim ~~2~~1, wherein the semiconductor device includes a height less than 1 millimeter.

6. The method of claim 1, wherein the opening includes a tapered sidewall formed by laser direct ablation.

7. A method of making a semiconductor device, comprising:

providing a ~~first~~ semiconductor ~~package~~die; ~~and~~

~~forming an opening in the first semiconductor package including a tapered sidewall and a first interconnect structure within the opening~~

depositing an encapsulant over and around the semiconductor die including a first surface of the encapsulant coplanar with an active surface of the semiconductor die and a planar second surface of the encapsulant opposite the first surface of the encapsulant;

forming an interconnect structure under the first surface of the encapsulant after depositing the encapsulant;

forming an opening in the planar second surface of the encapsulant; and

forming a bump recessed within the opening of the encapsulant.

~~8. The method of claim 7, wherein providing the first semiconductor package includes:~~

~~providing a semiconductor die;~~

~~depositing an encapsulant over the semiconductor die;~~

~~forming the opening in the encapsulant; and~~

~~depositing a conductive material in the opening to form the first interconnect structure.~~

~~9~~8. The method of claim ~~8~~7, ~~further including~~ wherein forming ~~a second~~the interconnect structure ~~over the encapsulant and a surface of~~ further includes forming the interconnect structure under the semiconductor die.

~~10~~9. The method of claim ~~9~~8, wherein the semiconductor die and ~~first interconnect structure~~ bump material are electrically connected to the ~~second~~ interconnect structure.

1~~1~~0. The method of claim 7, further including:

providing a ~~second~~ semiconductor package; and

disposing the ~~second~~ semiconductor package over the ~~first~~ semiconductor ~~package to electrically connect the second semiconductor package to the first interconnect structure~~ die and encapsulant.

1~~2~~1. The method of claim ~~11~~7, further including forming a plurality of bumps ~~over the second semiconductor package to electrically connect the second semiconductor package to the first~~ under the interconnect structure.

1~~3~~2. The method of claim 7, ~~wherein the~~ further including forming of the opening ~~includes using~~ by laser direct ablation.

1~~4~~3. A semiconductor device, comprising:

a semiconductor die;

an encapsulant ~~deposited~~ disposed over and around ~~over~~ the semiconductor die including a first surface of the encapsulant coplanar with an active surface of the semiconductor die and a planar second surface of the encapsulant opposite the first surface of the encapsulant and over a second surface of the semiconductor die opposite the active surface;

~~a first interconnect structure formed over the encapsulant;~~

~~an opening formed in the encapsulant to expose the first interconnect structure; and~~

~~a second interconnect structure formed over the first interconnect structure and recessed within the opening~~

an insulating layer formed under the first surface of the encapsulant including a first opening formed in the insulating layer;

a conductive layer disposed under the insulating layer and in the first opening with a second opening formed in the planar

surface of the encapsulant extending to the conductive layer; and

a bump formed over the conductive layer and recessed within the second opening.

~~15. The semiconductor device of claim 14, wherein the second interconnect structure includes a bump.~~

16~~4~~. The semiconductor device of claim 14~~3~~, further including a semiconductor package disposed over the encapsulant and electrically connected to the ~~second interconnect structure~~bump.

17~~5~~. The semiconductor device of claim 16~~3~~, wherein the semiconductor device includes a height less than 1 millimeter.

18~~6~~. The semiconductor device of claim 16~~3~~, further including ~~forming~~ a plurality of ~~bumps over the semiconductor package to electrically connect the semiconductor package to the second~~ interconnect structures disposed under the conductive layer.

19~~7~~. The semiconductor device of claim 16~~3~~, wherein the second opening includes a tapered sidewall.

~~20. The semiconductor device of claim 16, wherein the second interconnect structure includes a bump.~~

~~21. A semiconductor device, comprising:~~
~~a first semiconductor package; and~~
~~an opening formed in a surface of the first semiconductor package including a tapered sidewall and a first interconnect structure within the opening.~~

~~22. The semiconductor device of claim 21, wherein the first semiconductor package includes:~~
~~a semiconductor die; and~~
~~an encapsulant deposited over the semiconductor die;~~
~~the opening formed in a first surface of the encapsulant; and~~
~~the first interconnect structure formed within the opening.~~

~~23. The semiconductor device of claim 22, further including a second interconnect structure formed over a second surface of the encapsulant opposite the first surface of the encapsulant.~~

~~24. The semiconductor device of claim 21, wherein the first interconnect structure includes a bump.~~

~~25. The semiconductor device of claim 21, further including a second semiconductor package disposed over the first semiconductor package and electrically connected to the first interconnect structure.~~

18. A method of making a semiconductor device, comprising:

providing a substrate;

depositing an encapsulant over and around the substrate including a first surface of the encapsulant coplanar with a first surface of the substrate and a planar second surface of the encapsulant opposite the first surface of the encapsulant;

forming an interconnect structure under the first surface of the encapsulant after depositing the encapsulant; and

forming an opening in the planar second surface of the encapsulant.

19. The method of claim 18, wherein forming the interconnect structure further includes forming the interconnect structure under the substrate.

20. The method of claim 18, further including:

providing a semiconductor package; and

disposing the semiconductor package over the substrate and encapsulant.

21. The method of claim 18, further including forming of the opening in the encapsulant by laser direct ablation.

22. The method of claim 1, further including forming the opening in the encapsulant by laser direct ablation.