

## Method of Encapsulating a Substrate

### Field

The present invention relates to a method of encapsulating a substrate, and  
5 more specifically, it pertains to a method of encapsulating a substrate for CMOS-compatibility.

### Background

Silicon complementary metal-oxide-semiconductor (Si-CMOS) has dominated  
10 the semiconductor industry for the last five decades, leading to sustained and significant technological advancements in integrated circuits (ICs) and microelectronics, through application of Moore's Law scaling of CMOS transistor devices. However, the most advanced CMOS devices of today have shrunk to the point where they are only on the order of a few atoms in size, and are fast  
15 approaching a point where physics and economics will preclude further meaningful scaling. Thus, any future IC performance gains likely need to be achieved using different approaches, of which one of the most promising is to use new semiconductor materials to produce hybrid devices, such as compound semiconductors (e.g. III-V semiconductors and etc.), that have better electrical  
20 and optical properties than silicon. The most beneficial way to utilize the new materials is not to have them replace silicon entirely, but to adopt each material for manufacturing specific functional portions of an integrated circuit. For instance, the high integration density of Si-CMOS makes it ideal for producing functional portions intended for digital processing and logic applications,  
25 whereas various III-V materials are highly suitable for manufacturing functional portions intended for optoelectronic and RF/wireless applications, and high energy-storage density Li-based materials are optimal for producing integrated micro-batteries. The challenge therefore is to monolithically integrate the different types of materials such that the different functional portions of the  
30 circuits are able to work together seamlessly and efficiently, while occupying minimal chip footprint.

Practical monolithic integration requires different materials to be processed within CMOS circuits in commercial CMOS fabrication facilities, without  
35 compromising the standard CMOS manufacturing processes (i.e. no

contamination). This is because, due to massive investment over the past decades, the CMOS industry and infrastructure are the most developed and advanced, compared with the equivalent for other types of electronic materials. As a result, this generally requires that non-CMOS materials, which are typically  
5 perceived as (and sometimes, in very specific situations, are considered real) CMOS contaminants, are never etched or exposed during processing by CMOS compatible tools.

In this regard, there is a recent report in literature on prevention of cross-  
10 contamination between CMOS and III-V materials, where the solution proposed is to selectively grow the III-V layers (of an LED) and then cap the III-V materials with a thin layer of silicon – see FIG. 1. The bottom contact of the LED is accessed through the 100% germanium (Ge) cap of a silicon-on-lattice-engineered substrate (SOLES) wafer 100, as shown in FIG. 1.

15 However, in cases where completed non-CMOS layers are displaced above or under the Si-CMOS layer(s), the non-CMOS materials (of the layers) may still potentially be exposed at the edges of the associated wafers, since the non-CMOS regions are not confined within oxide wells, similar to the case in the  
20 SOLES wafer 100.

One object of the present invention is therefore to address at least one of the problems of the prior art and/or to provide a choice that is useful in the art.

## 25 **Summary**

According to a 1<sup>st</sup> aspect, there is provided a method of encapsulating a substrate having at least the following layers: a CMOS device layer, a layer of first semiconductor material different to silicon, and a layer of second semiconductor material, the layer of first semiconductor material arranged  
30 intermediate the CMOS device layer and the layer of second semiconductor material. The method comprises: (i) circumferentially removing a portion of the substrate at the edges; and (ii) depositing a dielectric material on the substrate to replace the portion removed at step (i) for encapsulating at least the CMOS device layer and the layer of first semiconductor material.

35

Beneficially, the proposed method allows the CMOS device layer and the layer of first semiconductor material (being non-CMOS and different to silicon) of the substrate to be encapsulated, so that when the substrate is later returned to semiconductor foundries for backend processing, the layer of first semiconductor material will not be exposed to contaminate CMOS compatible tools in the foundries.

Preferably, the first semiconductor material may include a group III-V semiconductor material, or a material formed from combining different III-V semiconductor materials.

In particular, the group III-V semiconductor material may include GaN, InGaP, AlGaAs, InGaAsP, InGaN, AlGaN, GaAs, Ge, or InGaAs.

Preferably, the second semiconductor material may include silicon, or a CMOS-compatible material.

Preferably, the CMOS device layer may include silicon-on-insulator based devices.

Preferably, circumferentially removing the portion of the substrate may include using reactive-ion etching, or inductively coupled plasma reactive-ion etching for the removal.

Preferably, prior to step (i), the method may further comprise removably attaching a wafer mask on the CMOS device layer using kapton tape, if reactive-ion etching, or inductively coupled plasma reactive-ion etching is used.

Preferably, the wafer mask may be formed of silicon.

Preferably, circumferentially removing the portion of the substrate may include using edge trimming for the removal.

Preferably, depositing the dielectric material on the substrate may include depositing a layer of the dielectric material on a surface of the CMOS device

layer which opposes the layer of first semiconductor material, and is substantially parallel to the horizontal axis of the substrate, the method may further include: (iii) planarizing the substrate to at least partially remove the layer of the dielectric material deposited on the surface of the CMOS device layer.

5

Preferably, planarizing the substrate may include using chemical mechanical polishing for the planarization.

10 Preferably, the dielectric material may be selected from the group consisting of aluminium oxide, aluminium nitride, silicon dioxide, silicon nitride, synthetic diamond and boron nitride.

Preferably, depositing the dielectric material on the substrate may include using plasma-enhanced chemical vapour deposition for the deposition.

15

Preferably, subsequent to step (iii), the method may further comprise: (iv) depositing the dielectric material on a surface of the layer of second semiconductor material which opposes the layer of first semiconductor material.

20 Preferably, subsequent to step (iii) or (iv), the method may yet further comprise: (v) annealing the substrate to densify the deposited dielectric material.

25 Preferably, circumferentially removing the portion of the substrate may include partially removing a portion of the edge of the layer of second semiconductor material.

Preferably, the method may further comprise maintaining attachment of the wafer mask on the CMOS device layer during performance of step (ii).

30 Preferably, the method may further comprise removing the wafer mask subsequent to step (i) and prior to step (ii); and depositing a spin-on glass material as the dielectric material on the substrate in step (ii).

35 According to a 2<sup>nd</sup> aspect, there is provided a substrate comprising at least the following layers: a CMOS device layer, a layer of first semiconductor material

different to silicon, and a layer of second semiconductor material, the layer of first semiconductor material being arranged intermediate the CMOS device layer and the layer of second semiconductor material. At least the CMOS device layer and the layer of first semiconductor material are arranged to be circumferentially  
5 encapsulated by a dielectric material.

Preferably, the first semiconductor material may include a group III-V semiconductor material, or a material formed from combining different III-V semiconductor materials.

10

Preferably, the second semiconductor material may include silicon, or a CMOS-compatible material.

15

Preferably, the CMOS device layer may include silicon-on-insulator based devices.

It should be apparent that features relating to one aspect of the invention may also be applicable to the other aspects of the invention.

20

These and other aspects of the invention will be apparent from and elucidated with reference to the embodiments described hereinafter.

### **Brief Description of the Drawings**

Embodiments of the invention are disclosed hereinafter with reference to the  
25 accompanying drawings, in which:

FIG. 1 shows schematics of monolithic integration achieved on a silicon-on-lattice-engineered substrate (SOLES) wafer, according to the prior art;

FIG. 2, which includes FIGs. 2a to 2e, is a method of encapsulating a substrate, according to an embodiment;

30

FIG. 3 shows a measurement result relating to the profile around the edge of the substrate of FIG. 2, after being subjected to reactive-ion etching, or inductively coupled plasma reactive-ion etching;

FIG. 4 shows a measurement result relating to the bow profile of the substrate of FIG. 2, subsequent to deposition of a layer of dielectric material;

FIGs. 5a and 5b show respective magnified views relating to the profile around the edge of the substrate of FIG. 2, after being subjected to chemical mechanical polishing (CMP);

FIG. 6 shows a measurement result relating to the bow profile of the substrate of FIG. 2, after being subjected to chemical mechanical polishing (CMP); and  
FIGs. 7a and 7b show respective graphs depicting gallium (Ga), indium (In) and arsenic (As) contaminations measured at two selected locations of a SOI-III-V/Si substrate, before and after the substrate is encapsulated using the method of FIG. 2.

10

### **Detailed Description of Preferred Embodiments**

FIG. 2 shows a method 200 of encapsulating a substrate 202 for CMOS-compatibility, according to an embodiment. The substrate 202 has at least the following layers: a CMOS device layer 204, a layer of first semiconductor material 206 (which is different to silicon and non-CMOS compatible), and a layer of second semiconductor material 208. The layer of first semiconductor material 206 is arranged intermediate the CMOS device layer 204 and the layer of second semiconductor material 208. From a top-down perspective, the layers of the substrate 202 are arranged as: the CMOS device layer 204, the layer of first semiconductor material 206, and the layer of second semiconductor material 208 (residing at the bottom of the substrate 202).

The CMOS device layer 204 may include silicon-on-insulator (SOI) based devices. It is to be appreciated that in some instances, the CMOS device layer 204 (when provided at step 250 of the method 200) may already be pre-capped with a capping dielectric layer, e.g. formed of Borophosphosilicate glass (which is not shown in FIG. 2a), on its top surface to protect the CMOS device layer 204, but need not always be the case. The capping dielectric layer may also be of a same dielectric material to be used at step 254 (although not necessarily so always), depending on applications. Further, to clarify, the definition of CMOS device layer 204 refers to only the single-crystal Si portion of an SOI substrate. The bulk of the SOI substrate has been removed and replaced with the layer of second semiconductor material 208. It is to be noted that an SOI substrate is canonically a thin (i.e. from 10 nm to few  $\mu\text{m}$ ) silicon single-crystal layer displaced over a "buried-oxide" (BOX) layer, which is further attached to a bulk

35

silicon substrate (of hundreds of  $\mu\text{m}$  thick). So the CMOS device layer 204 is defined to include all the CMOS devices fabricated (on the SOI substrate), and part/all of the BOX layer, for avoidance of doubt. Then, the first semiconductor material includes a group III-V semiconductor material, or a material formed from combining different III-V semiconductor materials. Specifically, the group III-V semiconductor material includes GaN, InGaP, AlGaAs, InGaAsP, InGaN, AlGaIn, GaAs, Ge, InGaAs, GaAs, InSb, AlSb, AlP, GaP, AlAs, GaAs, InP, InAs, GaAs, AlSb, InSb, GaN, InN, AlN or their compositions and etc. But this is not to be construed as limiting; indeed other non III-V materials (i.e. non-CMOS or different to silicon) are possible too – any other non-CMOS materials that may be deposited close to the CMOS device layer 204 may be used as the first semiconductor material. In certain instances, the layer of first semiconductor material 206 may also be provided in a completed device form, for example, as a high-electron-mobility transistor (HEMT).

15

On the other hand, the second semiconductor material includes silicon, or a CMOS-compatible material. Hence, (in certain embodiments) the substrate 202 can be in the form of an integrated patterned SOI-InGaAs/GaAs/Ge/Si substrate or a patterned SOI-GaN/Si substrate (and in either case, may collectively be referred to as an SOI-III-V/Si substrate). It is also to be appreciated that the specific structure of the substrate 202 and associated method of manufacturing the substrate 202 *per se* have already been disclosed in PCT publication number: WO 2016/007088, and so the interested reader may refer to the said PCT publication for more details on those aspects, if desired. The contents of PCT publication number, WO 2016/007088, are also incorporated by reference herein in their entirety. To briefly highlight, the substrate 202 (provided at step 250 herein) is equivalent to the final substrate 270 at FIG. 2e disclosed in WO 2016/007088, wherein the BOX layer 254 and the layer of dielectric material 262 in FIG. 2e of WO 2016/007088 are however not shown in substrate 202 of FIG. 2a herein for simplicity sake. For good order, it is also highlighted that the relative dimensions of the CMOS device layer 204, the layer of first semiconductor material 206, and the layer of second semiconductor material 208 depicted in FIG. 2 have been exaggerated simply for clarity of illustration, and are not to be construed as representative of the actual dimensions possible.

35

The method 200 starts by first providing the substrate 202 at step 250 (i.e. see FIG. 2a), and at next step 252 (i.e. see FIG. 2b), a portion of the substrate 202 is circumferentially removed at the edges. Particularly, in this instance, the amount of material for the circumferential edge of the CMOS device layer 204, and the layer of first semiconductor material 206 to be removed is kept as low as possible bearing in mind the need to consider process edge exclusions, which means a removal of about 3 mm to 7 mm of material from the original edge, while only a portion of the circumferential edge of the layer of second semiconductor material 208 is removed by the same thickness, as shown in FIG. 2b. This means that a section of the layer of second semiconductor material 208 processed at step 252 has a smaller circumference, compared to an adjoining section of the layer of second semiconductor material 208 not subjected to the circumferential removal process. The remaining portion of the layer of second semiconductor material 208 not removed at step 252 will then serve as a base to support a layer of dielectric material 210 to be deposited at next step 254 – see below. It is also to be clarified that step 250 is an optional step of the method 200. In this regard, circumferentially removing the portion of the substrate 202 includes using reactive-ion etching (RIE), inductively coupled plasma (ICP) RIE, or edge trimming for the removal, as desired. Needless to say, removing a portion of the substrate 202 at the edges reduces the original circumferential size of at least the CMOS device layer 204, and the layer of first semiconductor material 206 to some extent. Also, if RIE or ICP-RIE is used, a wafer mask (not shown) is to be removably attached onto the top surface of the CMOS device layer 204 using kapton tape, prior to execution of step 252. The wafer mask used is to be of a slightly smaller diameter (e.g. 190 mm), and is formed of silicon. The wafer mask protects the top surface of the CMOS device layer 204, when etching is being performed, but is removed when etching is completed.

At further step 254 (i.e. see FIG. 2c), a layer of dielectric material 210 is deposited (e.g. using plasma-enhanced chemical vapour deposition (PECVD), other suitable CVD techniques, or sputtering techniques) on the substrate 202 in order to replace the portion removed at step 252 for encapsulating at least the CMOS device layer 204 and the layer of first semiconductor material 206. A thickness of the dielectric material 210 to be deposited depends on requirements of applications intended, and can flexibly be deposited as larger/smaller than a

thickness of the portion of the substrate 202 removed at step 252. If the originally-present thickness of the capping dielectric layer (if provided) on the CMOS device layer 204 is to be preserved, then a larger thickness of the dielectric material 210 needs to be deposited, since some of the dielectric material 210 may be lost during planarization. On the other hand, because the originally present capping dielectric layer (if provided) can in some cases be arranged to take the planarization-related "loss" into account, a smaller amount of the dielectric material 210 may also be deposited. Hence, there is some flexibility in terms of how much of the dielectric material 210 to be deposited at step 254. This thus restores the substrate 202 back to its original size, circumferentially speaking. During the process, the top surface of the CMOS device layer 204 is also deposited with its own layer of the dielectric material 210 as well. The dielectric material 210 may (for example) be aluminium oxide ( $\text{Al}_2\text{O}_3$ ), aluminium nitride ( $\text{AlN}$ ), silicon dioxide ( $\text{SiO}_2$ ), silicon nitride ( $\text{SiN}$ ), synthetic diamond or boron nitride ( $\text{BN}$ ). Then at step 256 (i.e. see FIG. 2d), the substrate 202 is planarized (e.g. using chemical mechanical polishing (CMP)) to at least partially remove the dielectric material 210 deposited on the top surface of the CMOS device layer 204, when step 254 is carried out. More specifically, this is to expose the top surface of the CMOS device layer 204 – in this case, the top surface can be defined as a surface of the CMOS device layer 204 which opposes the layer of first semiconductor material 206, and is substantially parallel to the horizontal axis of the substrate 202.

At optional step 258 (i.e. see FIG. 2e), the dielectric material 210 is also deposited on the back surface of the layer of second semiconductor material 208, which opposes the layer of first semiconductor material 206. Step 258 may also be termed as the "*back-side*" treatment, and is done to ensure compatibility of the substrate 202 (subsequent to processing at step 258) with certain CMOS process flows, which may require a layer of backside dielectric to be present. Moreover, after step 256 or 258, the substrate 202 may be annealed to densify the dielectric material 210 deposited on the substrate 202 in order to improve the resistance to wet-chemical etching that may be performed in subsequent processes.

FIG. 3 shows a measurement result 300 relating to the profile around the edge of the substrate 202, after being subjected to RIE, or ICP-RIE at step 252. As shown, a vertical depth of about 6  $\mu\text{m}$  of material was etched (collectively from the CMOS device layer 204, the layer of first semiconductor material 206 and the layer of second semiconductor material 208) at the edge of the substrate 202 in this embodiment. It is to be appreciated that a thickness of the substrate 202 used in the experiment for obtaining the measurement result 300 is about 730  $\mu\text{m}$ , but certainly not limiting on application of the method 200 in any manner. Accordingly, approximately 6  $\mu\text{m}$  of the dielectric material 210 is then to be deposited on the substrate 202 (at step 254) as replacement, as afore described.

FIG. 4 shows a measurement result 400 relating to the bow profile of the substrate 202, subsequent to depositing the dielectric material 210 at step 254. As measured, the bow of the (processed) substrate 202 is about 14  $\mu\text{m}$  depicted in FIG. 4. As afore described, to planarize the substrate 202 at step 256, CMP may be used, and in this case, the CMP recipe is tuned for removing more materials at the centre of the substrate 202 (in relation to the CMOS device layer 204) than at the edges of the substrate 202. After performing CMP, the step profile obtained around the edge of the substrate 202 is shown in respective magnified diagrammatic views 500, 550 of FIGs. 5a and 5b. It can be observed from FIG. 5b that there is a dip at a location where the edge of the wafer mask is, the likely reason being that there might be a higher etch rate around this region. By using spin on glass (SOG), the problem can be addressed due to its better filling capability. In addition, the bow profile of the substrate 202, after subjected to CMP is shown in the measurement result 600 of FIG. 6. From FIG. 6, it is determined that the substrate 202 does not change much from 14  $\mu\text{m}$  (as previously measured in the result 400 of FIG. 4), which is considered an acceptable figure for all processing tools of subsequent processes.

30

Total Reflection X-ray Fluorescence (TXRF) spectroscopy is used to measure a level of III-V materials contaminations on the substrate 202 before and after encapsulation using the proposed method 200. In this regard, FIGs. 7a and 7b show respective graphs 700, 702 depicting gallium (Ga), indium (In) and arsenic (As) contaminations measured at two different locations of the substrate 202,

35

before and after processing via the method 200. As depicted in 7a and 7b, the III-V materials contaminations are reduced by two-orders of magnitude to between about  $10^{10}$  to  $10^{11}$  atoms/cm<sup>2</sup> after performing the encapsulation. Separately, some pin-holes and un-bonded areas are also observed on the processed substrate 202, which may explain the higher contamination observed. By addressing these problems (i.e. the pin-holes and un-bonded areas) correctly, it is envisaged that the contaminations by III-V materials can further be lowered. According to the IMEC specification, the desired contamination levels should ideally be lower than  $10^{11}$  atoms/cm<sup>2</sup>, and on this, it is believed the said criteria is attainable using the proposed method 200 for processing.

As above mentioned, PCT publication number: WO 2016/007088 discloses allowing for CMOS and non-CMOS materials (e.g. Si-CMOS and III-V materials respectively), to be processed separately and then combined together to form an integrated substrate using a double layer transfer (DLT) process. This however only partially solves the problem (related to integrating CMOS and non-CMOS materials in a device), as the integrated substrate still needs to be returned to semiconductor foundries for backend processing (e.g. to connect the Si-CMOS and HEMT together). During the backend processing, III-V materials from the edge of the integrated wafer may still be exposed to CMOS compatible tools in the foundries resulting in contamination, which is undesirable. Hence, additional protection is required on the edge of the integrated substrate to prevent the cross-contamination issue, which is advantageously solved by the proposed method 200. Particularly, the proposed method 200 includes edge etching/trimming a portion of the edge of the integrated substrate (e.g. about 5-7 mm from the edge), and thereafter, depositing the layer of dielectric material 210 to replace the etched edge portion and then followed by performing CMP on the integrated substrate for planarization. Optionally, the *back-side* treatment may also then be carried out on the processed integrated substrate, if necessary.

While the invention has been illustrated and described in detail in the drawings and foregoing description, such illustration and description are to be considered illustrative or exemplary, and not restrictive; the invention is not limited to the disclosed embodiments. Other variations to the disclosed embodiments can be

understood and effected by those skilled in the art in practising the claimed invention.

For example, at step 252, all necessary circumferential edge of the layer of  
5 second semiconductor material 208 is removed (in accordance with the  
corresponding edge portion removed for the CMOS device layer 204, and the  
layer of first semiconductor material 206), and not just only a portion of it. Also,  
the dielectric material 210 deposited on the back surface of the layer of second  
10 semiconductor material 208 at step 258 may be a different type of dielectric  
material from that used in step 254. Further, step 256 is not always required,  
depending on circumstances, and so step 256 is therefore optional to the  
proposed method 200. In addition, it is to be appreciated that the layer of first  
semiconductor material 206 may, in variant embodiments, be replaced by a  
15 plurality of III-V or other semiconductor layers (which are non-CMOS  
compatible). Alternatively, it may be that additional layers of different  
semiconductor materials (that are non-CMOS compatible) can also be arranged  
together with (on top/below) the layer of first semiconductor material 206, but  
still sandwiched between the CMOS device layer 204 and the layer of second  
semiconductor material 208. In such a case, all those additional layers are also  
20 to be encapsulated with the dielectric material 210 at step 254, together with the  
layer of first semiconductor material 206.

Further, at step 252, selective etching may alternatively be adopted to  
circumferentially etch away the layer of first semiconductor material 206 at the  
25 edges, which also needs corresponding cooperative optimization of step 254 to  
ensure complete encapsulation to be carried out subsequently.

Moreover, the wafer mask removably attached onto the top surface of the CMOS  
device layer 204, prior to execution of step 252 (if RIE or ICP-RIE is used), may  
30 be maintained on the CMOS device layer during performance of step 254, so  
that the dielectric material 210 will not be deposited on the top surface of the  
CMOS device layer 204 during the deposition process. Thereafter, the wafer  
mask can then be removed, once step 254 is completed. It is to be appreciated  
that planarization may or may not be required for this approach, depending on  
35 requirements.

Yet further, in another variation, the wafer mask removably attached onto the top surface of the CMOS device layer 204, prior to execution of step 252 (if RIE or ICP-RIE is used), may be removed subsequent to completing step 252 and prior to executing step 254; and then for step 254, a spin-on glass (SOG) material is  
5 deposited as the dielectric material 210 on the substrate 202 at step 254. It is to be appreciated that planarization may or may not be required for this approach, depending on requirements.

## Claims

1. A method of encapsulating a substrate having at least the following layers: a CMOS device layer a layer of first semiconductor material different to silicon, and a layer of second semiconductor material, the first semiconductor material being a group III-V semiconductor material or a material formed from combining different group III-V semiconductor materials, the layer of first semiconductor material arranged intermediate the CMOS device layer and the layer of second semiconductor material such that adjoining edges of the layer of first semiconductor material, the CMOS device layer and the layer of second semiconductor material define a circumferential edge of the substrate, the method comprising:
- (i) removing a portion of the circumferential edge, the portion removed comprising a portion of the CMOS device layer and a portion of the layer of first semiconductor material; and
- (ii) depositing a dielectric material on the substrate to replace the portion removed at step (i) for encapsulating at least the CMOS device layer and the layer of first semiconductor material such that the layer of first semiconductor material is unexposed.
2. The method of claim 1, wherein the group III-V semiconductor material includes GaN, InGaP, AlGaAs, InGaAsP, InGaN, AlGaN, GaAs, Ge, or InGaAs.
3. The method of any preceding claims, wherein the second semiconductor material includes silicon, or a CMOS-compatible material.
4. The method of any preceding claims, wherein the CMOS device layer includes silicon-on-insulator based devices.
5. The method of any preceding claims, wherein removing the portion of the circumferential edge includes using reactive-ion etching, or inductively coupled plasma reactive-ion etching for the removal.

6. The method of claim 5, wherein prior to step (i), the method further comprises:

removably attaching a wafer mask on the CMOS device layer, if reactive-ion etching, or inductively coupled plasma reactive-ion etching is used.

5

7. The method of claim 6, wherein the wafer mask is formed of silicon.

8. The method of any one of claims 1 to 4, wherein removing the portion of the circumferential edge includes using edge trimming for the removal.

10

9. The method of any preceding claims, wherein depositing the dielectric material on the substrate includes depositing a layer of the dielectric material on a surface of the CMOS device layer which opposes the layer of first semiconductor material, and is substantially parallel to the horizontal axis of the substrate, further includes:

15

(iii) planarizing the substrate to at least partially remove the layer of the dielectric material deposited on the surface of the CMOS device layer.

10. The method of claim 9, wherein planarizing the substrate includes using chemical mechanical polishing for the planarization.

20

11. The method of any preceding claims, wherein the dielectric material is selected from the group consisting of aluminium oxide, aluminium nitride, silicon dioxide, silicon nitride, synthetic diamond and boron nitride.

25

12. The method of any preceding claims, wherein depositing the dielectric material on the substrate includes using plasma-enhanced chemical vapour deposition for the deposition.

30

13. The method of claim 9, wherein subsequent to step (iii), further comprises:

(iv) depositing the dielectric material on a surface of the layer of second semiconductor material which opposes the layer of first semiconductor material.

14. The method of claim 9 or 13, wherein subsequent to step (iii) or (iv), further comprises:

(v) annealing the substrate to densify the deposited dielectric material.

5 15. The method of any preceding claims, wherein removing the portion of the circumferential edge includes partially removing a portion of the edge of the layer of second semiconductor material.

16. The method of claim 6, further comprises:

10 maintaining attachment of the wafer mask on the CMOS device layer during performance of step (ii).

17. The method of claim 16, further comprises:

15 removing the wafer mask subsequent to step (i) and prior to step (ii); and depositing a spin-on glass material as the dielectric material on the substrate in step (ii).

18. A substrate comprising at least the following layers:

20 a CMOS device layer,  
a layer of first semiconductor material different to silicon, and  
a layer of second semiconductor material, the first semiconductor material being a group III-V semiconductor material or a material formed from combining different group III-V semiconductor materials, the layer of first semiconductor material arranged intermediate the CMOS device layer and the layer of second semiconductor material such that adjoining edges of the layer of first semiconductor material, the CMOS device layer and the layer of second semiconductor material define a circumferential edge of the substrate,

25 wherein a portion of the circumferential edge has been removed, the portion removed comprising a portion of the CMOS device layer and a portion of the layer of first semiconductor material; and

30 a dielectric material deposited on the substrate to replace the portion removed and which encapsulates at least the CMOS device layer and the layer of first semiconductor material such that the layer of first semiconductor material is unexposed.

35

19. The substrate of claim 18, wherein the second semiconductor material includes silicon, or a CMOS-compatible material.

5 20. The substrate of claim 18 or 19, wherein the CMOS device layer includes silicon-on-insulator based devices.

21. The substrate of any one of claims 18 to 20, wherein the dielectric material includes a layer of dielectric material deposited on a surface of the CMOS device layer which opposes the layer of first semiconductor material, and  
10 is substantially parallel to the horizontal axis of the substrate, and wherein the layer of dielectric material is at least partially removed by planarizing the substrate.

15