

Description

Field of the Invention

This invention relates generally to switched capacitor bandgap reference circuits and more particularly to CMOS bandgap reference circuits.

Description of the Prior Art

Typically, the best reference for a good reproducible stable voltage below three volts has been the bandgap reference circuit. As discussed in *Analysis and Design of Analog Integrated Circuits* by Paul R. Gray and Robert G. Meyer (John Wiley and Sons, 1977, pp. 239—261), the base to emitter voltage V_{be} of a bipolar transistor exhibits a negative temperature coefficient with respect to temperature. Thus, the sum of the base to emitter voltage, V_{be} , of a bipolar transistor and a differential voltage ΔV_{be} will be relatively independent of temperature when the sum voltage equals the energy gap of silicon. An example of this type of temperature stable reference is illustrated by David Bingham in an article entitled "CMOS: Higher Speeds, More Drive and Analog Capability Expand Its Horizons", *Electronic Design* 23, November 8, 1978, pg 81. Bandgap references operate on the principle of generating a V_{be} and summing a ΔV_{be} of such value that the sum substantially equals the bandgap voltage of 1.205 volts.

A standard CMOS process can be used to fabricate open emitter NPN bipolar transistors for use in a bandgap reference circuit such as that taught in U.S. Patent 4,287,439. To create a stable temperature independent CMOS bandgap voltage with amplifying means, such as an operational amplifier, two transistors of varying current density were used as emitter followers having resistors in their emitter circuits from which a differential voltage was obtained. The same principle of using two transistors with differing current densities as emitter followers having resistors in their emitter circuits is also taught in DE—AI—3 024 348 corresponding to U.S. Patent 4,263,519. Therefore, an output voltage having a positive, negative or zero coefficient is thereby produced.

Several factors in the CMOS circuit, however, affected the initial tolerance variation and temperature variation of the bandgap voltage. Problems with P-resistor matching and a 2:1 variation in the P-resistivity over temperature resulted in variation of the reference voltage. A dominant error is also caused by the offset voltage associated with the operational amplifier being multiplied by the ratio of two resistors in the emitter circuit of the transistor with the lowest current density. Some previous CMOS bandgap circuits have also required a startup circuit.

A circuit utilizing switched capacitors for producing an output voltage according to the sum or difference of charges stored on the switched capacitors is taught by Thomas P. Redfern et al. in U.S. Patent 4,191,900. However, such switched capacitor circuits have been used as high-gain

voltage amplifiers for applications such as comparators.

Summary of the Invention

It is an object of the present invention to provide a bandgap reference utilizing substrate bipolar transistors and MOS transistors to provide a reference voltage which is substantially temperature stable and substantially independent of process variations.

It is a further object of the invention to provide a bandgap reference suitable to be fabricated using a standard CMOS process and switched capacitor techniques, which sums the V_{be} and ΔV_{be} of substrate bipolar transistors to derive a near zero temperature coefficient reference voltage.

These objects are achieved by the invention as claimed. Accordingly there are provided a first and a second substrate bipolar transistor wherein the emitter area of the first transistor is much larger than the emitter area of the second transistor. Since the second transistor is operated at a higher current density than the first transistor, the V_{be} of the second transistor is greater than the V_{be} of the first transistor. Using switching capacitors coupled to the emitters of the transistors, the base to emitter voltages of the devices are sampled. When the difference between the two sampled voltages are added in the correct proportion, the result is a voltage with a substantially zero temperature coefficient. The above and other objects, features and advantages of the present invention will be more clearly understood from the following detailed description taken in conjunction with the accompanying drawings.

Brief Description of the Drawings

Figure 1 is a schematic diagram illustrating one preferred embodiment of the invention.

Figure 2 is a graphic timing diagram for the schematic embodiment shown in Figure 1.

Figure 3 is a schematic diagram illustrating another embodiment of the amplifier used in the present invention.

Figure 4 is a graphic timing diagram for the schematic embodiment shown in Figure 3.

Description of the Preferred Embodiment

Shown in Figure 1, is a switched capacitor bandgap reference circuit 10 constructed in accordance with the preferred embodiment of this invention. The bandgap reference circuit 10 is comprised generally of first and second bipolar transistors 12 and 14, respectively, a clock circuit 16, a first switched capacitance circuit 18, a second switched capacitance circuit 20, and an amplifier circuit 22.

Each of the first and second bipolar transistors 12 and 14 has the collector thereof connected to a positive supply V_{dd} , the base thereof connected to a common reference voltage, say analog ground V_{ss} , and the emitter thereof connected to a negative supply V_{ss} via respective current sources 24 and 26. In the preferred form, the current sources 24 and 26 are constructed to sink a predetermined

ratio of currents, and transistor 12 is fabricated with a larger emitter area than the transistor 14. Since the transistors 12 and 14 are biased at different current densities they will thus develop different base-to-emitter voltages, V_{be} . Because the transistors 12 and 14 are connected as emitter followers, the preferred embodiment may be fabricated using the substrate NPN in a standard CMOS process.

In the first switched capacitance circuit 18, a capacitor 28 has an input connected via switches 30 and 32 to the common reference voltage V_{ag} and the emitter of transistor 14, respectively. In the second switched capacitance circuit 20, a capacitor 34 has an input connected via switches 36 and 38 to the emitter of transistors 12 and 14, respectively. Capacitors 28 and 34 have the outputs thereof connected to a node 40. In the preferred embodiment, switches 30, 32, 36 and 38 are CMOS transmission gates which are clocked in a conventional manner by the clock circuit 16. Switches 30 and 36 are constructed to be conductive when a clock signal A applied to the control inputs thereof is at a high state, and non-conductive when the clock signal A is at a low state. Switches 32 and 38 are preferably constructed to be conductive when a clock signal B applied to the control inputs thereof is at a high state and non-conductive when the clock signal B is at a low state.

In this configuration, switches 30 and 32 will cooperate to charge capacitor 28 alternately to the base voltage of transistor 14 and the emitter voltage of transistor 14, thus providing a charge related to V_{be} of transistor 14. Simultaneously, switches 36 and 38 cooperated to charge capacitor 34 alternately to the emitter voltage of transistor 12 and the emitter voltage of transistor 14, thus providing a charge related to the difference between the base to emitter voltages, i.e., the ΔV_{be} , of the transistors 12 and 14. As will be clear to those skilled in the art, the voltage, V_{be} , will exhibit a negative temperature coefficient (NTC). On the other hand, it is well known that the voltage ΔV_{be} exhibits a positive temperature coefficient (PTC). Thus, it will be clear that the weighted sum of these voltages, $V_{be} + K\Delta V_{be}$, where $K = C_{34}/C_{28}$ may be made substantially temperature independent by appropriate selection of the ratio of capacitors 28 and 34.

In the amplifier circuit 22, an operational amplifier 42 has its negative input coupled to node 40 and its positive input coupled to the reference voltage V_{ag} . A feedback capacitor 44 is coupled between the output of operational amplifier 42 at node 46 and the negative input of the operational amplifier at node 40. In the preferred form, a switch 48 is coupled across feedback capacitor 44 with the control input thereof coupled to clock signal C provided by clock circuit 16. By periodically closing switch 48, the operational amplifier 42 is placed in unity gain, and any charge on capacitor 44 is removed.

As shown in Figure 2, the clock circuit 16 initially provides a clock signal A in a high state to

close switches 30 and 36, and clock signal B in a low state to open switches 32 and 38. Simultaneously, the clock circuit 16 provides the clock signal C in a high state to close the switch 48. During this precharge period, feedback capacitor 44 is discharged, and, ignoring any amplifier offset, capacitors 28 and 34 are charged to the reference voltage, V_{ag} , and the V_{be} of the transistor 12, respectively. A short time before the end of the precharge period, the clock circuit 16 opens switch 48 by providing the clock signal C in a low state. Shortly thereafter, but still before the end of the precharge period, the clock 16 opens switches 30 and 36 by providing the clock signal A in the low state. At the end of the precharge period and the start of a valid output reference period, the clock circuit 16 closes switches 32 and 38 by providing the clock signal B in the high state. At this time, the voltage on the terminals of capacitor 28 changes by $-V_{be}$ of transistor 14 and the voltage on the terminals of capacitor 34 changes by the difference between the base to emitter voltages of the transistors 12 and 14, $(V_{be12} - V_{be14})$. This switching event causes an amount of charge

$$Q = V_{be14}C_{28} + (V_{be12} - V_{be14})C_{34}$$

to be transferred to capacitor 44 resulting in an output voltage of

$$V_{ref} = -1/C_{44}[-V_{be14}C_{28} + (V_{be12} - V_{be14})C_{34}]$$

on node 46. In the preferred form, this positive bandgap reference voltage, $+V_{ref}$ is made substantially temperature independent by making the ratio of capacitors 28 and 34 equal to the ratio of the temperature coefficients of ΔV_{be} and V_{be} . If desired, a negative bandgap reference voltage, $-V_{ref}$, may be obtained by inverting clock signal C so that the precharge and valid output reference periods are reversed.

In general, the accuracy of the bandgap circuit 10 will be adversely affected by the offset voltage of the operational amplifier. Figure 3 illustrates in schematic form, a modified form of amplifier circuit 22' which can be substituted for the amplifier circuit 22 of Figure 1 to substantially eliminate the offset voltage error. Amplifier circuit 22' is comprised of the operational amplifier 42 which has its positive input coupled in parallel to feedback capacitor 44 and periodically discharges the feedback capacitor. However, one terminal of the feedback capacitor 44 is now connected via a switch 52 to the output of the operational amplifier 42 at node 46. Capacitor 44 is also coupled to an input signal, V_{in} , at node 40. In addition, an offset storage capacitor 54 is coupled between node 40 and the negative input terminal of operational amplifier 42, and a switch 56 is connected between node 40 and the reference voltage V_{ag} . In this embodiment, the clock circuit 16' generates the additional clock signals D and E, as shown in Figure 4 for controlling the switches 56 and 50, respectively, with the inverse of clock

signal D controlling switch 52. In this configuration, the bandgap reference circuit 10 has three distinct periods of operation. During the pre-charge period, the clock circuit 16' provides clock signals C, D, and E in the high state to close switches 48, 56 and 50 and open switch 52. During this period, capacitor 44 is discharged by switch 48. The operational amplifier 42 is placed in unity gain by switch 50, and the offset storage capacitor 54 is charged to the offset voltage, V_{os} , of the operational amplifier 42. Near the end of the precharge period, the clock circuit 16' provides clock signal E in the low state to open switch 50, leaving capacitor 54 charged to the offset voltage of the operational amplifier 42. A short time thereafter, the clock circuit 16' provides clock signal D in the low state to open switch 56 and close switch 52. Since the switching event tends to disturb the input mode 40, a short settling time is preferably provided before clock circuit 16' provides clock signal C in the low state to open switch 48. Thereafter, the charge stored on feedback capacitor 44 will be changed only by a quantity of charge coupled from the switched capacitor sections 18 and 20. During this third period of circuit operation, labeled the valid output reference period, the reference voltage developed on the node 46 will be substantially free of any offset voltage error. If the offset capacitor 54 is periodically charged to the offset voltage, V_{os} , the operational amplifier 42 is effectively autozeroed, with node 40 being the zero-offset input node.

While the invention has been described in the context of a preferred embodiment, it will be apparent to those skilled in the art that the present invention may be modified in numerous ways and may assume many embodiments other than that specifically set out and described above.

Claims

1. A switched capacitor bandgap reference circuit (10) for producing a substantially temperature independent reference voltage (V_{REF}) comprising first and second bipolar transistor means (12 and 14) having a predetermined base voltage and biased at different current densities to develop first and second emitter voltages, respectively, on the emitters thereof, and amplifier means for providing a reference voltage (V_{REF}), characterized by:

clock means (16) for alternately providing first and second non-overlapping clock signals;

first switched capacitance means (28) coupled to said base voltage in response to the first clock signal (A) and to said first emitter voltage in response to the second clock signal (B), for providing a first charge related to the base-emitter voltage (V_{be}) of the first transistor means;

second switched capacitor means (34) coupled to said second emitter voltage in response to the first clock signal (A) and to said first emitter voltage in response to the second clock signal (B), for providing a second charge related to the

difference in the base-emitter voltages (V_{be12} , V_{be14}) of the first and second bipolar transistors (12 and 14); and

amplifier means (22) coupled to the first and second capacitance means (28 and 34) for providing a reference voltage (V_{REF}) proportional to the sum of the first and second charges.

2. The circuit according to claim 1 wherein each of said switched capacitance means (28 and 34) comprises a capacitor and switching means (30, 32 and 36, 38, respectively), responsive to said clock signals.

3. The circuit according to claim 2 wherein said amplifier means (22) comprise an operational amplifier (42), a feedback capacitor (44), and switching means (48) for periodically connecting the input and output of the feedback capacitor (44) together for discharge.

4. The circuit according to claim 2 wherein said amplifier means (22) is an autozeroed amplifier comprising an operational amplifier (42) having positive and negative inputs and an output, a feedback capacitor (44), first switching means (48) for connecting the input and output of the feedback capacitor (44) together for discharge in response to a third clock signal (C), second switching means (52) for connecting the output of the feedback capacitor (44) to the output of the operational amplifier (42) in response to a fourth clock signal (D), and third switching means (50) for connecting the negative input and output of the operational amplifier (42) together in response to a fifth clock signal (E).

5. A method of producing a substantially temperature independent bandgap reference voltage (V_{REF}) by biasing first and second bipolar transistor means (14 and 12), respectively, having the same predetermined base voltage, at difference current densities to develop first and second emitter voltages characterized by:

providing first and second non-overlapping clock signals (A and B);

coupling the input of first capacitance means (28) to said base voltage in response to the first clock signal (A) and to the first emitter voltage in response to the second clock signal (B), whereby said first capacitance means (28) provides a first charge related to the base-emitter voltage (V_{be}) of the first transistor means (14);

coupling the input of second capacitance means (34) to said second emitter voltage in response to the first clock signal (A) and to said first emitter voltage in response to the second clock signal (B), whereby the second capacitance means (34) provides a second charge related to the difference in base-emitter voltages (V_{be12} , V_{be14}) of the first and second transistor means (14 and 12), respectively; and

amplifying the sum of the charges received from the outputs of the first and second capacitance means (28 and 34) to provide a reference voltage (V_{REF}) proportional to the sum of the first and second charges.



signal D controlling switch 52. In this configuration, the bandgap reference circuit 10 has three distinct periods of operation. During the precharge period, the clock circuit 16' provides clock signals C, D, and E in the high state to close switches 48, 56 and 50 and open switch 52. During this period, capacitor 44 is discharged by switch 48. The operational amplifier 42 is placed in unity gain by switch 50, and the offset storage capacitor 54 is charged to the offset voltage, V_{os} , of the operational amplifier 42. Near the end of the precharge period, the clock circuit 16' provides clock signal E in the low state to open switch 50, leaving capacitor 54 charged to the offset voltage of the operational amplifier 42. A short time thereafter, the clock circuit 16' provides clock signal D in the low state to open switch 56 and close switch 52. Since the switching event tends to disturb the input mode 40, a short settling time is preferably provided before clock circuit 16' provides clock signal C in the low state to open switch 48. Thereafter, the charge stored on feedback capacitor 44 will be changed only by a quantity of charge coupled from the switched capacitor sections 18 and 20. During this third period of circuit operation, labeled the valid output reference period, the reference voltage developed on the node 46 will be substantially free of any offset voltage error. If the offset capacitor 54 is periodically charged to the offset voltage, V_{os} , the operational amplifier 42 is effectively autozeroed, with node 40 being the zero-offset input node.

While the invention has been described in the context of a preferred embodiment, it will be apparent to those skilled in the art that the present invention may be modified in numerous ways and may assume many embodiments other than that specifically set out and described above.

Claims

1. A switched capacitor bandgap reference circuit (10) for producing a substantially temperature independent reference voltage (V_{REF}) comprising first and second bipolar transistor means (12 and 14) having a predetermined base voltage and biased at different current densities to develop first and second emitter voltages, respectively, on the emitters thereof, and amplifier means for providing a reference voltage (V_{REF}), characterized by:

clock means (16) for alternately providing first and second non-overlapping clock signals;

first switched capacitance means (28) coupled to said base voltage in response to the first clock signal (A) and to said first emitter voltage in response to the second clock signal (B), for providing a first charge related to the base-emitter voltage (V_{be}) of the first transistor means;

second switched capacitor means (34) coupled to said second emitter voltage in response to the first clock signal (A) and to said first emitter voltage in response to the second clock signal (B), for providing a second charge related to the

difference in the base-emitter voltages (V_{be12} , V_{be14}) of the first and second bipolar transistors (12 and 14); and

amplifier means (22) coupled to the first and second capacitance means (28 and 34) for providing a reference voltage (V_{REF}) proportional to the sum of the first and second charges.

2. The circuit according to claim 1 wherein each of said switched capacitance means (28 and 34) comprises a capacitor and switching means (30, 32 and 36, 38, respectively), responsive to said clock signals.

3. The circuit according to claim 2 wherein said amplifier means (22) comprise an operational amplifier (42), a feedback capacitor (44), and switching means (48) for periodically connecting the input and output of the feedback capacitor (44) together for discharge.

4. The circuit according to claim 2 wherein said amplifier means (22) is an autozeroed amplifier comprising an operational amplifier (42) having positive and negative inputs and an output, a feedback capacitor (44), first switching means (48) for connecting the input and output of the feedback capacitor (44) together for discharge in response to a third clock signal (C), second switching means (52) for connecting the output of the feedback capacitor (44) to the output of the operational amplifier (42) in response to a fourth clock signal ($\bar{D}$), and third switching means (50) for connecting the negative input and output of the operational amplifier (42) together in response to a fifth clock signal (E).

5. A method of producing a substantially temperature independent bandgap reference voltage (V_{REF}) by biasing first and second bipolar transistor means (14 and 12), respectively, having the same predetermined base voltage, at different current densities to develop first and second emitter voltages characterized by:

providing first and second non-overlapping clock signals (A and B);

coupling the input of first capacitance means (28) to said base voltage in response to the first clock signal (A) and to the first emitter voltage in response to the second clock signal (B), whereby said first capacitance means (28) provides a first charge related to the base-emitter voltage (V_{be}) of the first transistor means (14);

coupling the input of second capacitance means (34) to said second emitter voltage in response to the first clock signal (A) and to said first emitter voltage in response to the second clock signal (B), whereby the second capacitance means (34) provides a second charge related to the difference in base-emitter voltages (V_{be12} , V_{be14}) of the first and second transistor means (14 and 12), respectively; and

amplifying the sum of the charges received from the outputs of the first and second capacitance means (28 and 34) to provide a reference voltage (V_{REF}) proportional to the sum of the first and second charges.



Patentansprüche

1. Bandlückenreferenzschaltung (10) mit geschalteten Kondensatoren zum Erzeugen einer im wesentlichen temperaturunabhängigen Bezugsspannung (V_{REF}), enthaltend erste und zweite bipolare Transistoreinrichtungen (12 und 14), die eine vorbestimmte Basisspannung haben und mit unterschiedlichen Strömdichten vorgespannt sind, um erste bzw. zweite Emitterspannungen an ihren Emittern zu entwickeln, und Verstärkereinrichtungen zum Bereitstellen einer Bezugsspannung (V_{REF}), gekennzeichnet durch:

eine Takteinrichtung (16) zum alternierenden Abgeben von ersten und zweiten nichtüberlappenden Taktsignalen;

eine erste geschaltete Kondensatoreinrichtung (28), die mit der Basisspannung in Abhängigkeit von dem ersten Taktsignal (A) und mit der ersten Emitterspannung in Abhängigkeit von dem zweiten Taktsignal (B) verbunden ist, um eine erste Ladung zur Verfügung zu stellen, die auf die Basis-Emitter-Spannung (V_{be}) der ersten Transistoreinrichtung bezogen ist;

eine zweite geschaltete Kondensatoreinrichtung (34), die mit der zweiten Emitterspannung in Abhängigkeit von dem ersten Taktsignal (A) und mit der ersten Emitterspannung in Abhängigkeit von dem zweiten Taktsignal (B) verbunden ist, um eine zweite Ladung zur Verfügung zu stellen, die auf die Differenz der Basis-Emitter-Spannungen (V_{be12} , V_{be14}) der ersten und zweiten bipolaren Transistoren (12 und 14) bezogen ist; und

eine Verstärkereinrichtung (22), die mit den ersten und zweiten Kondensatoreinrichtungen (28 und 34) verbunden ist, um eine Bezugsspannung (V_{REF}) zur Verfügung zu stellen, die proportional der Summe der ersten und zweiten Ladungen ist.

2. Schaltung nach Anspruch 1, bei der die geschaltete Kondensatoreinrichtung (24 und 28) einen Kondensator und eine Schalteinrichtung (30, 32 bzw. 36, 38) enthält, die auf die Taktsignale anspricht.

3. Schaltung nach Anspruch 2, bei der die Verstärkereinrichtung (22) einen Operationsverstärker (42), einen Rückkopplungskondensator (44) und eine Schalteinrichtung (48) zum periodischen Verbinden des Eingangs und des Ausgangs des Rückkopplungskondensators (44) zur Entladung enthält.

4. Schaltung nach Anspruch 2, bei der die Verstärkereinrichtung (22) ein selbstrückstellender Verstärker ist, enthaltend einen Operationsverstärker (42) mit positiven und negativen Eingängen und einem Ausgang, einen Rückkopplungskondensator (44), eine erste Schalteinrichtung (48) zum Verbinden des Eingangs und des Ausgangs des Rückkopplungskondensators (44) miteinander zur Entladung in Abhängigkeit von einem dritten Taktsignal (C), eine zweite Schalteinrichtung (52) zum Verbinden des Ausgangs des Rückkopplungskondensators (44) mit dem Ausgang des Operationsverstärkers (42) in Abhängigkeit von einem vierten Taktsignal

(D), und eine dritte Schalteinrichtung (50) zum Verbinden des negativen Eingangs und des Ausgangs des Operationsverstärkers (42) miteinander in Abhängigkeit von einem fünften Taktsignal (E).

5. Verfahren zum Erzeugen einer im wesentlichen temperaturunabhängigen Bandlückenreferenzspannung (V_{REF}) durch Vorspannen erster bzw. zweiter bipolarer Transistoreinrichtungen (14 und 12), die dieselbe vorbestimmte Basisspannung haben, mit unterschiedlichen Stromdichten, um erste und zweite Emitterspannungen zu entwickeln, gekennzeichnet durch

Bereitstellen erster und zweiter nichtüberlappenden Taktsignale (A und B);

Verbinden des Eingangs einer ersten Kondensatoreinrichtung (28) mit der Basisspannung in Abhängigkeit von dem ersten Taktsignal (A) und mit der ersten Emitterspannung in Abhängigkeit von dem zweiten Taktsignal (B), wodurch die erste Kondensatoreinrichtung (28) eine erste Ladung bereitstellt, die auf die Basis-Emitter-Spannung (V_{be}) der ersten Transistoreinrichtung (14) bezogen ist;

Verbinden des Eingangs der zweiten Kondensatoreinrichtung (34) mit der zweiten Emitterspannung in Abhängigkeit von dem ersten Taktsignal (A) und mit der ersten Emitterspannung in Abhängigkeit von dem zweiten Taktsignal (B), wodurch die zweite Kondensatoreinrichtung (34) eine zweite Ladung bereitstellt, die auf die Differenz der Basis-Emitter-Spannungen (V_{be12} , V_{be14}) der ersten bzw. zweiten Transistoreinrichtungen (14 und 12) bezogen ist; und

Verstärken der Summe der Ladungen, die von den Ausgängen der ersten und zweiten Kondensatoreinrichtung (28 und 34) empfangen werden, um eine Bezugsspannung (V_{REF}) bereitzustellen, die proportional der Summe der ersten und zweiten Ladungen ist.

Revendications

1. Circuit de référence d'inter-bande (10) à condensateurs commutés servant à produire une référence de tension sensiblement indépendante de la température (V_{REF}) qui comprend un premier et un deuxième moyen à transistor bijonction (12, 14) possédant une tension de base prédéterminée et polarisés à des densités de courant différentes de manière à produire respectivement une première et une deuxième tension d'émetteur sur leurs émetteurs, et un moyen amplificateur servant à produire une tension de référence (V_{REF}), caractérisé par:

un moyen d'horloge (16) qui produit alternativement un premier et un deuxième signal d'horloge ne se chevauchant pas;

un premier moyen à capacité commutée (28) qui est connecté à ladite tension de base en réponse au premier signal d'horloge (A) et à la première tension d'émetteur en réponse au deuxième signal d'horloge (B), de manière à produire une première charge en relation avec la tension



base-émetteur (V_{be}) du premier moyen à transistor;

un deuxième moyen à capacité commutée (34) qui est couplé à ladite deuxième tension d'émetteur en réponse au premier signal d'horloge (A) et à ladite première tension d'émetteur en réponse au deuxième signal d'horloge (B), de manière à produire une deuxième charge en relation avec la différence des tensions base-émetteur (V_{be12} , V_{be14}) des premier et deuxième transistors bijonction (12 et 14); et

un moyen amplificateur (22) couplé aux premier et deuxième moyens à capacité (28 et 34) servant à produire une tension de référence (V_{REF}) proportionnelle à la somme des première et deuxième charges.

2. Circuit selon la revendication 1, où chacun desdits moyens à capacité commutée (28 et 34) comprend un condensateur et un moyen de commutation (respectivement 30, 32 et 36, 38) répondant auxdits signaux d'horloge.

3. Circuit selon la revendication 2, où ledit moyen amplificateur (22) comprend un amplificateur opérationnel (42), un condensateur de réaction (44), et un moyen de commutation (48) servant à connecter périodiquement l'entrée et la sortie du condensateur de réaction (44) ensemble en vue de sa décharge.

4. Circuit selon la revendication 2, où ledit moyen amplificateur (22) est un amplificateur à mise automatique à zéro comprenant un amplificateur opérationnel (42) qui possède des entrées positive et négative et une sortie, un condensateur de réaction (44), un premier moyen de commutation (48) servant à connecter l'entrée et la sortie du condensateur de réaction (44) ensemble pour la décharge en réponse à troisième signal d'horloge (C), un deuxième moyen de commutation (52) servant à connecter la sortie du condensateur de réaction (44) avec la sortie de

l'amplificateur opérationnel (42) en réponse à un quatrième signal d'horloge (D), et un troisième moyen de commutation (50) servant à connecter l'entrée négative et la sortie de l'amplificateur opérationnel (42) ensemble en réponse à un cinquième signal d'horloge (E).

5. Procédé de production d'une tension de référence d'inter-bande sensible indépendante de la température (V_{REF}) où on polarise respectivement un premier et un deuxième moyen à transistor bijonction (14, 12), possédant la même tension de base prédéterminée, à des densités de courant différentes afin de créer une première et une deuxième tension d'émetteur, caractérisé en ce que:

on produit un premier et un deuxième signal d'horloge ne se chevauchant pas (A et B);

on couple l'entrée du premier moyen à capacité (28) sur ladite tension de base en réponse au premier signal d'horloge (A) et sur la première tension d'émetteur en réponse au deuxième signal d'horloge (B), si bien que le premier moyen à capacité (28) produit une première charge en relation avec la tension base-émetteur (V_{be}) du premier moyen à transistor (14);

on couple l'entrée du deuxième moyen à capacité (34) sur la deuxième tension d'émetteur en réponse au premier signal d'horloge (A) et sur la première tension d'émetteur en réponse au deuxième signal d'horloge (B), si bien que le deuxième moyen à capacité (34) produit une deuxième charge en relation avec la différence des tensions base-émetteur (V_{be12} , V_{be14}) des premier et deuxième moyens à transistors (14 et 12) respectivement;

et on amplifie la somme des charges reçues de la part des sorties des premier et deuxième moyens à capacité (28 et 34) afin de produire une tension de référence (V_{REF}) proportionnelle à la somme des première et deuxième charges.



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