CLAIMS

1. A semiconductor device, comprising:

a first wafer having at least one graphene channel formed on a first substrate, a first oxide layer surrounding the graphene channel and source and drain contacts to the graphene channel that extend through the first oxide layer; and

a second wafer having a complementary metal oxide semiconductor (CMOS) device layer formed in a second substrate, a second oxide layer surrounding the CMOS device layer and a plurality of contacts to the CMOS device layer that extend through the second oxide layer, the first wafer and the second wafer being bonded together by way of an oxide-to-oxide bond between the first and second oxide layers,

wherein one or more of the contacts to the CMOS device layer are in contact with the source and drain contacts to the graphene channel, and wherein one or more other of the contacts to the CMOS device layer are gate contacts for the graphene channel.

2. The device of claim 1, wherein the CMOS device layer comprises one or more CMOS wiring, structures and devices.

3. The device of claim 1, wherein the first substrate comprises an insulating wafer, a wafer having an insulating overlayer or a silicon carbide wafer.

4. The device of claim 1, wherein the second substrate comprises a silicon-on-insulator wafer or a bulk silicon wafer.

5. The device of claim 1, wherein the source and drain contacts to the graphene channel and the contacts to the CMOS device layer each comprises copper, and wherein the first wafer and the second wafer are further bonded together by way of a copper-to-copper bond between the source and drain contacts to the graphene channel and one or more of the contacts to the CMOS device layer.

6. The device of claim 1, wherein the first wafer and the second wafer are bonded together in a face-to-face orientation.

7. A method of fabricating a semiconductor device, comprising the steps of:

forming a first wafer having at least one graphene channel formed on a first substrate, a first oxide layer surrounding the graphene channel and source and drain contacts to the graphene channel that extend through the first oxide layer;

forming a second wafer having a CMOS device layer formed in a second substrate, a second oxide layer surrounding the CMOS device layer and a plurality of contacts to the CMOS device layer that extend through the second oxide layer; and

bonding the first wafer and the second wafer together by way of an oxide-to-oxide bond between the first and second oxide layers, such that one or more of the contacts to the CMOS device layer are in contact with the source and drain contacts to the graphene channel, and one or more other of the contacts to the CMOS device layer are gate contacts for the graphene channel.

8. The method of claim 7, further comprising the step of:

flipping one of the first wafer or the second wafer to permit face-to-face bonding with an other of the first wafer or the second wafer.

9. A transistor device, comprising:

a substrate;

source and drain contacts formed on the substrate;

a graphene channel formed on the substrate connecting the source and drain contacts; and

a gate contact over the graphene channel, separated from the graphene channel by a dielectric, wherein the gate contact is in a non-overlapping position with the source and drain contacts leaving exposed sections of the graphene channel between the gate contact and the source and drain contacts, and wherein the exposed sections of the graphene channel are doped with an n-type or p-type dopant.

10. The device of claim 9, further comprising;

a capping layer over the source and drain contacts, the gate contact and the exposed sections of the graphene channel.

11. The device of claim 9, wherein the substrate comprises an insulating wafer, a wafer having an insulating overlayer or a silicon carbide wafer.

12. The device of claim 9, wherein the exposed sections of the graphene channel are doped with an n-type dopant comprising poly(ethylene imine).

13. The device of claim 9, wherein the exposed sections of the graphene channel are doped with a p-type dopant comprising diazonium salts.

14. The device of claim 10, wherein the capping layer comprises an oxide or a nitride material.

15. A method of fabricating a transistor device, comprising:

providing a substrate;

forming source and drain contacts on the substrate;

forming a graphene channel on the substrate connecting the source contact and the drain contact;

forming a gate contact over the graphene channel and separated from the graphene channel by a dielectric, wherein the gate contact is in a non-overlapping position with the source and drain contacts leaving exposed sections of the graphene channel between the gate contact and the source and drain contacts; and

doping the exposed sections of the graphene channel with an n-type or p-type dopant.

16. The method of claim 15, further comprising the step of:

forming one or more graphene layers on the substrate.

17. The method of claim 16, wherein the substrate comprises a wafer having an insulating overlayer and wherein the step of forming the graphene layers further comprises the step of:

depositing the graphene layers on a surface of the insulating overlayer using exfoliation.

18. The method of claim 16, wherein the substrate comprises a silicon carbide wafer and wherein the step of forming the graphene layers further comprises the step of:

growing the graphene layers on the silicon carbide wafer by silicon sublimation with epitaxy.

19. The method of claim 16, wherein the step of forming the source and drain contacts on the substrate further comprises the steps of:

patterning a resist mask over the graphene layers and the substrate to define source and drain contact regions;

depositing a metal around the resist mask in the source and drain contact regions to form the source and drain contacts; and

removing the resist mask.

20. The method of claim 16, wherein the step of forming the graphene channel on the substrate further comprises the step of:

patterning a mask on the graphene layers to define an active channel region;

removing portions of the graphene layers unprotected by the mask; and

removing the mask.

21. The method of claim 15, further comprising the step of:

depositing the dielectric over the graphene channel, the source and drain contacts and the substrate.

22. The method of claim 15, further comprising the step of:

forming a capping layer over the source and drain contacts, the gate contact, the exposed sections of the graphene channel and the substrate.

CLAIMS

1. A method of fabricating a transistor device, comprising:

providing a substrate;

forming source and drain contacts on the substrate;

forming a graphene channel on the substrate connecting the source contact and the drain contact;

forming a gate contact over the graphene channel and separated from the graphene channel by a dielectric, wherein the gate contact is in a non-overlapping position with the source and drain contacts leaving exposed sections of the graphene channel between the gate contact and the source and drain contacts; and

doping the exposed sections of the graphene channel with an n-type or p-type dopant, wherein the gate contact is used as a doping mask to dope the exposed sections of the graphene channel not covered by the gate contact such that the gate contact and doped sections of the graphene channel are self-aligned with one another.

2. The method of claim 1, further comprising the step of: forming one or more graphene layers on the substrate.

3. The method of claim 2, wherein the substrate comprises a wafer having an insulating overlayer and wherein the step of forming the graphene layers further comprises the step of: depositing the graphene layers on a surface of the insulating overlayer using exfoliation.

4. The method of claim 2, wherein the substrate comprises a silicon carbide wafer and wherein the step of forming the graphene layers further comprises the step of: growing the graphene layers on the silicon carbide wafer by silicon sublimation with epitaxy.

5. The method of claim 2, wherein the step of forming the source and drain contacts on the substrate further comprises the steps of:

patterning a resist mask over the graphene layers and the substrate to define source and drain contact regions;

depositing a metal around the resist mask in the source and drain contact regions to form the source and drain contacts; and

removing the resist mask.

6. The method of claim 2, wherein the step of forming the graphene channel on the substrate further comprises the step of:

patterning a mask on the graphene layers to define an active channel region;

removing portions of the graphene layers unprotected by the mask; and

removing the mask.

7. The method of claim 1, further comprising the step of: depositing the dielectric over the graphene channel, the source and drain contacts and the substrate.

8. The method of claim 1, further comprising the step of: forming a capping layer over the source and drain contacts, the gate contact, the exposed sections of the graphene channel and the substrate.

9. The method of claim 1, further comprising the step of: using the gate contact as an etching mask to remove, by etching, portions of the dielectric on the graphene channel not covered by the gate contact.