METHOD FOR FORMING AN INTEGRATED CIRCUIT

Abstract of the Disclosure

In one embodiment, a first dielectric layer (16) is formed overlying a semiconductor substrate (4). A portion of the first dielectric layer (16) is then etched using a patterned masking layer (18). The patterned masking layer (18) is removed and an intermediate polishing layer (20) is formed overlying the first dielectric layer (16). A second dielectric layer (22) is formed overlying the intermediate polishing layer (20), and the second dielectric layer (22) is polished to expose a portion of the intermediate polishing layer (20), and to determine a polishing rate for the second dielectric layer (22). The polishing rate for the second dielectric layer (22) is then used to calculate a polishing time for the first dielectric layer (16), and the first dielectric layer (16) is polished for the calculated time.

(FIGURE 1 IS SUGGESTED FOR PUBLICATION)