A METHOD OF MAKING A WAFER LEVEL INTEGRATION PACKAGE

Field of the Invention

The present invention relates in general to semiconductor devices and, more particularly, semiconductor package devices.

Background of the Invention

Semiconductors, or computer chips, are found in virtually every electrical product manufactured today. Chips are used not only in sophisticated industrial and commercial electronic equipment, but also in many household and consumer items such as televisions, clothes washers and dryers, radios, and telephones. As products become smaller and more functional, there is a need to include more chips in the smaller products to perform the functionality. The reduction in size of cellular telephones is one example of how more capabilities are incorporated into smaller electronic products.

As the demand for semiconductor devices with low-cost, high performance, increased miniaturization, and greater packaging densities has increased, devices having multiple dies, such as Multi-Chip Module (MCM) structures or similar stacked die structures have been developed to meet the demand. MCM structures have a number of dies and other semiconductor components mounted within a single semiconductor package. The number of dies and other components can be mounted in a vertical manner, a lateral manner, or combinations thereof.

One such approach is to stack one die on top of another die and then enclose the stack of dies in one package.

The final package for a semiconductor with stacked dies is much smaller than would result if the dies were each packaged separately. In addition to providing a smaller size, stacked-die packages offer a number of advantages that relate to the manufacturing of the package, such as ease of handling and assembly.

In a stacked-die arrangement, the dies are wire-bonded sequentially, typically with automated wire-bonding equipment employing well-known thermal compression or ultrasonic wire-bonding techniques. During the wire-bonding process, the head of a wire-bonding apparatus applies a downward pressure on a conductive wire held in contact with a wire-bonding pad on the die to weld, or bond, the wire to the bonding pad on the die.

In many cases, stacked-die semiconductors can be fabricated faster and more cheaply than several semiconductors, each having a single die, which perform the same functions. A stacked-die approach is advantageous because of the increase in circuit density achieved and the ability to perform differing functionality, e.g., memory, logic, application specific integrated circuit (ASIC), within the same package. As a result, such multiple die package technologies as chip scale packaging (CSP), including ball grid array (BGA) and flip chip (bumped devices), and wafer level packaging (WLCSP) have been implemented. Further integration with passive devices using technologies such as System-in-Package (SiP) and chip scale module packaging (CSMP) have been commonly used.

However, the desire to achieve higher integration using the various technologies discussed previously generally causes a final package structure to be either larger in footprint or thicker. Greater integration has generally

resulted in a tradeoff sacrifice of package miniaturization.

Summary of the Invention

Therefore, a need exists for a package that allows higher integration of devices with differing functionality and yet maintains or decreases the package profile.

Accordingly, in one embodiment, the present invention is a method of forming a semiconductor package comprising the steps of providing a wafer having a first electrical contact pad integrated into a top surface of the wafer, forming a through-hole interconnection extending downward from a first surface of the first electrical contact pad, electrically connecting a die to a second surface of the first electrical contact pad, cutting the wafer to form a channel portion and a connecting portion, disposing an encapsulant over the die and the channel portion, backgrinding the wafer to remove the connecting portion and expose a surface of the through-hole interconnection, disposing a second electrical contact pad over the surface of the through-hole interconnection, and disposing a dielectric layer along a side surface of the second electrical contact pad.

In another embodiment, the present invention is a semiconductor package comprising a wafer having a first electrical contact pad integrated into a top surface of the wafer. A through-hole interconnection extends downward from a first surface of the first electrical contact pad. A die is electrically connected to a second surface of the first electrical contact pad. A second electrical contact pad is disposed over a surface of the through-hole interconnection. A dielectric layer is disposed along a side surface of the second

electrical contact pad. The wafer is cut to form a channel portion and a connecting portion. An encapsulant is disposed over the die and channel portion. The wafer is backgrinded to remove the connecting portion and expose the surface of the through-hole interconnection.

In another embodiment, the present invention is a semiconductor package comprising a wafer having a first electrical contact pad integrated into a top surface of the wafer. A through-hole interconnection extends downward from a first surface of the first electrical contact pad. A first die is electrically connected to a second surface of the first electrical contact pad. A second electrical contact pad is disposed over a surface of the through-hole interconnection. A dielectric layer is disposed along a first surface of the second electrical contact pad. A second die is electrically connected to a second surface of the second electrical contact pad. The wafer is cut to form a channel portion and a connecting portion. A first encapsulant is disposed over the die and the channel portion. The wafer is backgrinded to remove the connecting portion and expose the surface of the through-hole interconnection.

In another embodiment, the present invention is a method of manufacturing a semiconductor device comprising the steps of providing a wafer having a first electrical contact pad integrated into a top surface of the wafer, providing a through-hole interconnection extending downward from a first surface of the first electrical contact pad, providing a die electrically connected to a second surface of the first electrical contact pad, providing a second electrical contact pad disposed over a surface of the through-hole interconnection, and providing a dielectric layer disposed

along a side surface of the second electrical contact pad. The wafer is cut to form a channel portion and a connecting portion. An encapsulant is disposed over the die and the channel portion. The wafer is backgrinded to remove the connecting portion and expose the surface of the through-hole interconnection.

Brief Description of the Drawings

FIG. 1A illustrates an exemplary prior art semiconductor device;

FIG. 1B illustrates a first exemplary prior art semiconductor substrate;

FIG. 1C illustrates a second exemplary prior art semiconductor substrate;

FIG. 2A illustrates a first step in an exemplary method of forming a semiconductor device;

FIG. 2B illustrates a second step in the exemplary method begun in FIG. 2A;

FIG. 2C illustrates a third step in the exemplary method begun in FIG. 2A;

FIG. 2D illustrates a fourth step in the exemplary method begun in FIG. 2A;

FIG. 2E illustrates a fifth step in the exemplary method begun in FIG. 2A;

FIG. 2F illustrates a sixth step in the exemplary method begun in FIG. 2A;

FIG. 2G illustrates a seventh step in the exemplary method begun in FIG. 2A;

FIG. 2H illustrates an eighth step in the exemplary method begun in FIG. 2A;

FIG. 2I illustrates a ninth step in the exemplary method begun in FIG. 2A;

FIG. 3 illustrates a first exemplary embodiment of a semiconductor device incorporating a flip chip integrated circuit;

FIG. 4 illustrates a second exemplary embodiment of a semiconductor device including a plurality of lands;

FIG. 5 illustrates a third exemplary embodiment of a semiconductor device where a top surface of an integrated die is left exposed;

FIG. 6 illustrates a fourth exemplary embodiment of a semiconductor device incorporating a heat spreader structure to provide thermal enhancement;

FIG. 7 illustrates a fifth exemplary embodiment of a semiconductor device incorporating an electrical shield structure;

FIG. 8 illustrates a sixth exemplary embodiment of a semiconductor device incorporating a wire-bonded integrated circuit; and

FIG. 9 illustrates a seventh exemplary embodiment of a semiconductor device employing package-in-package technologies.

Detailed Description of the Drawings

The present invention is described in one or more embodiments in the following description with reference to the Figures, in which like numerals represent the same or similar elements. While the invention is described in terms of the best mode for achieving the invention's objectives, it will be appreciated by those skilled in the art that it is intended to

cover alternatives, modifications, and equivalents as may be included within the spirit and scope of the invention as defined by the appended claims and their equivalents as supported by the following disclosure and drawings.

A semiconductor package can be manufactured which takes into account a stacked-die arrangement and serves to alleviate many of the problems previously described, while providing increasingly smaller sizes. The package can be manufactured more easily and with greater efficiency than previous packages, resulting in a package with lower overall manufacturing cost. Finally, the reliability of semiconductor packages having stacked dies is increased by use of the following designs and methods of manufacture.

Turning to FIG. 1A, an exemplary prior art semiconductor device 10 is illustrated. Device 10 includes a wafer or substrate 12 having a top surface 16 and a bottom surface 14. A cap 18 is disposed over the top surface to enclose electrical component 24. A dielectric liner 20 is disposed through a via in wafer 12 extending from top surface 16 to bottom surface 14. The via is filled with conductive material 22 as shown.

FIGs. 1B and 1C further illustrate various prior art embodiments of the via structure. In FIG. 1B, substrate 26 includes a bottom surface 28 and top surface 34. A conductive material 30 is disposed between surfaces 32 disposed in trenches in wafer 26. Similarly, FIG. 1C includes another wafer 36 having a bottom surface 38 and top surface 44, where a conductive material 42 is disposed within surfaces 40 which line the vias in the wafer.

The present invention improves upon such methods and techniques as seen in the prior art, to render a semiconductor

device which is smaller in height and footprint, more efficient to manufacture, and results in higher performance.

FIG. 2A illustrates a first step in an exemplary method of forming a semiconductor device according to the present invention. A wafer 50 has a silicon substrate. Wafers and similar substrates 50 can be provided which vary in size and depth for a particular application.

A second step in the exemplary method of forming a semiconductor device begun with FIG. 2A is shown in FIG. 2B. A series of electrical contact pads 52 are formed as redistribution layers (RDLs) or flex-on-cap (FOC) process. FOC involves vertically disposing the solder ball directly over an under-bump metallization (UBM) which overlies a bonding pad to a wafer. RDL involves laterally separating the location of the solder ball from the wafer bonding pad, although the solder ball remains electrically connected to the bonding bad by the RDL track. In either case, pads 52 are integrated into a top surface of wafer 50.

A third step in the exemplary method is seen in FIG. 2C, where a series of through-hole interconnections 54 are formed in substrate 50. The interconnections 54 can be etched in the substrate and filled with a conductive material, or similar techniques can be utilized. In various embodiment, the through-hole interconnections can extend to depths varying between thirty to one-hundred fifty micrometers (um).

As a next fourth step in the exemplary method, a flip chip or similar die 58, such as a wire-bondable die is attached to through-hole interconnections 54. A series of bumps 60 can provide electrical connectivity from die 58 to through-hole interconnections 54. An optional underfill material 56 can be deposited between die 58 and the top surface of substrate 50.

At the conclusion of the fourth step, a series of dies 58 are electrically connected to a plurality of through-hole interconnections 54, which are partially disposed through wafer 50. Again, as FIG. 2D represents a partial cross-section, any number of dies 58 can be provided, in a variety of configurations to suit particular applications.

FIG. 2E represents a fifth step in the exemplary method of forming a semiconductor device. As shown, a series of channels, trenches or voids 62 are formed between each respective assembly of interconnections 54, pads 52, and die 58. The various electrical connections and support mechanisms between dies 58 and interconnections 54 and pads 52 can include bumps 60 and/or underfill material 56.

An encapsulant 64 is disposed over the respective assemblies as seen in FIG. 2F, which depicts a sixth step in the exemplary method of forming a semiconductor device. Encapsulant 64 coats respective surfaces of dies 58, optional underfill material 56, and surfaces of wafer 50. Each of the channels 62 are filled with encapsulant 64. Encapsulant 64 can include polymer materials, organic material, and other encapsulating material. Encapsulant 64 provides structural support to the various components, e.g., die 58, in the semiconductor device.

Wafer 50, in a seventh step in the exemplary method of forming a semiconductor device depicted by FIG. 2G, undergoes a backgrinding operation to remove material from a bottom or back portion of wafer 50. Surface 70 results from the backgrinding operation, where once connecting portions of wafer structure 50 are removed, as denoted by arrow 68. Each of the respective assemblies remain connected by a layer of encapsulant 64.

A bottom surface 66 of through-hole interconnections 54 is exposed by use of the backgrinding process. As seen in FIGs. 2F and 2G, channels 62 are formed to roughly correspond to the depth of the plurality of interconnections 54, so that when the connecting portions of wafer 50 are removed, surfaces 66 of interconnections 54 are exposed.

FIG. 2H illustrates a next, eighth step in the exemplary method of forming a semiconductor device. A plurality of backside pads 72 are electrically connected to surfaces 66 of interconnections 54. Pads 72 can be formed in much the same manner as pads 52, using RDL or FOC, incorporated into a top side of wafer 50 as previously seen. A dielectric layer 74 is disposed along the back side or bottom surface 70 of the wafer. Dielectric layer 74 is disposed along a side surface of pads 72. Layer 74 surrounds and isolates pads 72 and provides structural support across bottom surface 70 of wafer 50.

A series of solder balls 78 can then be attached or otherwise coupled and/or connected to each of pads 72 in a next, ninth step in the depicted exemplary method of forming a semiconductor device. Each of the assemblies can be optionally function-tested to determine if respective electrical connections are satisfactorily made.

As a final step, each of the respective assemblies 80 can then be singulated into semiconductor devices 80 as seen in FIG. 2I. In one embodiment, the final semiconductor device 80 includes balls 78, which electrically connect semiconductor device 80 to another structure. Backside pads 72 are coupled to through-hole interconnections 54 and to topside pads 52. A die 58 is connected to topside pads 52 using bumps 60 and anchored by underfill material 56.

In one exemplary method of forming semiconductor device 80, a wafer can first be provided which has a series of first electrical contact pads integrated into a top surface of the wafer. A through-hole interconnection can then be formed which extends downward from a first surface of the first electrical contact pad. A die can be then attached to a second surface of the electrical contact pads. The wafer can be cut to form a channel portion and a connecting portion. An encapsulant can then be disposed over the die and the channel portion. The wafer can then undergo a backgrinding process to remove the connecting portion and expose a surface of the through-hole interconnection. A second series of electrical contact pads can be disposed over the surface of the through-hole interconnection. A dielectric layer along a side surface of the second pads. A ball can be then coupled to the second pads to provide electrical connectivity.

Turning to FIG. 3, a first exemplary embodiment of a semiconductor device 80 incorporating a flip chip IC die 58 is seen. Device 80 can be referred to as a wafer level integration package device 80. Device 80 includes such previously mentioned structures as pads 52, optional underfill layer 56, bumps 60, encapsulant 64, pads 72, dielectric layer 74, and balls 78.

In addition to the aforementioned structures, device 80 includes a passive component 82 such as a filter, balun, inductor, capacitor, resistor, or a similar electrical device 82, which is integrated into device 80 and electrically connected to the device through a portion of pads 52 as shown. The embedded passive component can perform such functionality as providing capacitance, inductance, resistance, or a combination of functions.

The wafer structure 50 in the instant embodiment incorporates a double-sided integration circuit 84. The double-sided integration circuit 84 is an active integrated circuit device. Device 84 can perform such functionality as logic, memory, application specific (ASIC), or embedded integrated passive device (IPD). The double-sided integration circuit can function as a semiconductor interposer, in that the wafer can provide structural support without providing additional electronics functionality; yet function to provide the distribution of electrical signals from a source to a destination.

Device 84 can route signals on both the top and bottom surfaces of the device. Signal routes can be provided by having single or multiple pads 52 and 72 along the X-Y directions. A series of through-hole interconnections 54 routes signals along the Z direction.

Device 84 can include various interconnection pads to accommodate such signal transfer mediums as wire, bumps, and other passive component interconnections as will be further described. Device 84, as with other materials comprising the overall semiconductor device 80, can include silicon (Si), gallium arsenide (GaAs), or any other suitable semiconductor material or a combination thereof.

The side walls of the double sided integration circuit 84 are protected by encapsulant 64, as denoted by arrows 86. As a result, the wafer level integration device 80 is made more reliable and more resilient, particularly to handling steps.

Wafer level integration packages such as package/device 80 can include single or multiple integrated circuit (IC) devices which can be attached onto a top or a

bottom side of the double-sided integration circuit device 84. The IC devices can be wire-bondable, flip chip, passive components, or a combination thereof. The IC devices can be arranged in a side-by-side configuration or by stacking. The various configurations are applicable to both respective top and bottom sides of the double-sided integration circuit device 84.

Package/device 80 can be used as an inner stacking module (ISM) for package-in-package configuration, as will be later described. Package/device 80 can also be used as a conventional ball grid array (BGA) package 80, whereby package 80 can be attached onto a substrate for further packaging and/or testing.

Turning to FIG. 4, a second exemplary embodiment of a wafer level integration package 88 is shown. Package 88 includes a passive device 82 as previously seen. Dielectric layer 74 as configured and formed renders a series of lands 90 which expose pads 72. The lands 90 can be intended to provide electrical connectivity for specific applications. The lands 90 can be formed in a variety of configurations to expose as much or as little of a portion of a respective pad 72 as needed.

FIG. 5 illustrates an additional, third embodiment of a wafer level integration package 92, where the incorporated flip chip IC 58 has an exposed top surface 94. In the instant embodiment, encapsulant 64 is formed such that the top surface of flip chip IC 58 is exposed for a particular application, such as to provide a smaller, thinner package 92. Encapsulant 64 can be deposited such that surface 94 is exposed, or surface 94 can be later exposed through a grinding procedure or a similar mechanical operation to reduce the coverage of

encapsulant 64.

A variant of the exposed surface package 92 is seen in FIG. 6 as a thermally enhanced wafer level integration package 96, where an adhesive material 98 is disposed over the top surface of die 58. The adhesive couples a heat spreader 100 structure to the top surface of die 58 to dissipate heat across the top surface of the package. The heat spreader 100 can also incorporate other thermal characteristics to enhance the overall performance of package 96 in certain conditions.

FIG. 7 illustrates a wafer level integration package 102, which incorporates an electrical shield structure 106. The electrical shield structure 106 is coupled to a portion of wafer 50 using an adhesive structure 104 and surrounds and shields electrical components, i.e., die 58 and/or other passive components 82, which are housed interior to shield structure 106. Structure 106 and adhesive mounts 104 are surrounded by encapsulant 64 to provide additional structural support to package 102. The shield is made of metal cap with holes to allow encapsulation. The shield prevents signal interference between devices within the package as well as outside package. Any interference will distort signal transmission, which can be problematic in RF applications.

FIG. 8 illustrates an additional embodiment of a wafer level integration package 108 incorporating a wire-bondable die 110, which is connected by wires 112 to wire-bonding pads 114. Wire-bonding pads 114 are integrated into the topside of wafer 50 in a manner similar to pads 52. Pads 52 can be modified to accept wire-bonding as indicated. Wire-bond IC 110 and wires 112 are covered with encapsulant 64 to provide structural support.

In an additional embodiment, FIG. 9 illustrates a

wafer level integration package 80 which is then disposed over a bumped substrate to render a package-in-package (PiP) 118 configuration. Package 80 serves as an ISM, as previously described, for PiP implementations.

A die adhesive 120 is utilized to mount the wafer level integration package 80 to a surface of a bumped substrate 122. A series of vias 128 or similar structures carry electrical signals through substrate 122 to a series of balls 78, which are disposed on a bottom surface of substrate 122.

An additional die or package 124 is disposed over device 80. Die or package 124 is electrically connected to device 80 using bumps 130. A bump pad 72 carries electrical signals over a wire 112 to an electrical terminal 126 of bumped substrate 122.

A second encapsulant 132 is disposed over package 80 and package 124 or die 124 as seen to form a complete package-in-package configuration 118. A variety of dies or packages 124 can be incorporated with device 80 to suit a particular application.

While one or more embodiments of the present invention have been illustrated in detail, the skilled artisan will appreciate that modifications and adaptations to those embodiments may be made without departing from the scope of the present invention as set forth in the following claims.

Claims

What is claimed:

1. A method of forming a semiconductor package, comprising:

providing a wafer having a first electrical contact pad integrated into a top surface of the wafer;

forming a through-hole interconnection extending downward from a first surface of the first electrical contact pad;

electrically connecting a die to a second surface of the first electrical contact pad;

cutting the wafer to form a channel portion and a connecting portion;

disposing an encapsulant over the die and the channel portion;

backgrinding the wafer to remove the connecting portion and expose a surface of the through-hole interconnection;

disposing a second electrical contact pad over the surface of the through-hole interconnection; and

disposing a dielectric layer along a side surface of the second electrical contact pad.

2. The method of claim 1, further including disposing a solder bump between the die and the first electrical contact pad to electrically connect the die to the first electrical contact pad.

3. The method of claim 1, further including disposing an underfill material between the die and the first electrical contact pad to provide structural support.

4. The method of claim 1, further including connecting a solder ball to the second electrical contact pad to provide electrical connectivity.

5. The method of claim 4, further including testing the die for functionality.

6. The method of claim 4, further including singulating the wafer into an individual segment containing the die.

7. The method of claim 1, wherein the die includes a flip chip semiconductor device, a wire bond semiconductor device, a passive component, or a combination thereof.

8. The method of claim 1, wherein the dielectric layer is disposed to form a plurality of lands extending across a bottom surface of the semiconductor device.

9. The method of claim 1, further including electrically connecting a passive component to the first surface of the first electrical contact pad.

10. A method of manufacturing a semiconductor device, comprising:

providing a wafer having a first electrical contact pad integrated into a top surface of the wafer;

providing a through-hole interconnection extending downward from a first surface of the first electrical contact pad;

providing a die electrically connected to a second surface of the first electrical contact pad;

providing a second electrical contact pad disposed over a surface of the through-hole interconnection; and

providing a dielectric layer disposed along a side surface of the second electrical contact pad, wherein:

the wafer is cut to form a channel portion and a connecting portion,

an encapsulant is disposed over the die and the channel portion, and

the wafer is backgrinded to remove the connecting portion and expose the surface of the through-hole interconnection.

11. The method of manufacture of claim 10, further including providing a solder bump disposed between the die and the first electrical contact pad to electrically connect the die to the first electrical contact pad.

12. The method of manufacture of claim 10, further including providing an underfill material disposed between the die and the first electrical contact pad to provide structural support.

13. The method of manufacture of claim 10, wherein the die includes a flip chip semiconductor device, a wire bond semiconductor device, a passive component, or a combination thereof.

14. The method of manufacture of claim 10, wherein the dielectric layer is disposed in a pattern to render a plurality of lands extending across a bottom surface of the semiconductor device.

15. The method of manufacture of claim 10, further including providing a passive component electrically connected to the first surface of the first electrical contact pad.

16. The method of manufacture of claim 10, wherein the encapsulant is disposed such that a top surface of the die is exposed.

17. The method of manufacture of claim 16, further including providing an adhesive layer disposed over the top surface of the die, and a heat spreader structure disposed over the adhesive to render a thermally enhanced semiconductor package.