

ESD PROTECTION CIRCUIT

ABSTRACT

A device which includes a substrate defined with a device region having an ESD protection circuit is disclosed. The ESD protection circuit has a transistor. The transistor includes a gate having first and second sides. A first diffusion region is disposed adjacent to the first side of the gate and a second diffusion region is disposed in the device region displaced away from the second side of the gate. The first and second diffusion regions include dopants of a first polarity type. A drift isolation region is disposed between the gate and the second diffusion region. A first device well encompasses the device region and a second device well is disposed within the first device well. A drain well having dopants of the first polarity type is disposed under the second diffusion region and within the first device well.

Fig.1a