ABSTRACT

A semiconductor memory device includes a gate stack structure including alternately stacked interlayer insulating layers and conductive layers, a core pillar penetrating the gate stack structure, a channel layer disposed between the core pillar and the gate stack structure, a memory layer disposed between the channel layer and the gate stack structure, and a doped semiconductor part in contact with the gate stack structure. The doped semiconductor part includes a first region surrounding the core pillar up to an interface in contact with the gate stack structure and a second region extending between the memory layer and the core pillar from the first region.

FIG. 2