TITLE OF THE INVENTION

PROCESS FOR THE PRODUCTION OF SEMICONDUCTOR DEVICE

BACKGROUND OF THE INVENTION AND RELATED ART STATEMENT

The present invention relates to a process for the production of a semiconductor device, particularly to a process for the production of a semiconductor device, which includes the step of filling a concave portion such as an opening portion and/or a trench portion with an electrically conductive material to form a connection hole and/or a trench wiring.

Semiconductor devices integrated to a higher degree, such as ULSIs (Ultra-Large Scale Integrated-Circuits), are required to have high processing speed and high durability against the electromigration of a wiring which is intensified with an increase in the consumption power.

Conventionally, an aluminum-based alloy (e.g., Al-0.5%Cu, Al-1%Si-0.5%Cu) is generally used as a wiring material for a semiconductor device. For a further increase in the speed of a semiconductor device, it is required to use copper (Cu), silver (Ag) or the like which have a lower specific resistance, as a wiring material. In particular, copper has a low specific resistance, as low as 1.8 $\mu\Omega\cdot$cm, and is advantageous for an increase in the speed of a semiconductor device, and further, it has an excellent electromigration durability which is one digit higher than that of any aluminum-based alloy, so that it is expected to be a next-generation wiring material which will replace the aluminum-based alloy.

Meanwhile, a semiconductor device has a number of contact holes or viaholes (these will be generically called "connection holes" hereinafter) formed for connecting elements or multi-layered wirings. Generally, the connection holes are formed by forming opening portions (holes) in an insulating interlayer and filling

an electrically conductive material in the opening portions. When an aluminum-based alloy is used as an electrically conductive material, the opening portions are easily filled. When copper is used, however, it is difficult to completely fill the opening portions with copper. That is, in a high-temperature sputtering method and a reflow method which are frequently used for filling the opening portions with an aluminum-based alloy, the process temperature is set at approximately 450 °C. Differing from the aluminum-based alloy, copper has a high melting temperature, and the opening portions cannot be reliably filled with copper at the above process temperature. Further, even if the opening portions are experimentally filled, it is very difficult to fill a 10^6 level of the opening portions in ULSI 100 per cent with copper.

In recent years, further, there is being practically employed a so-called single damascene method in which trench portions are formed in an insulating interlayer and filled with a wiring material constituted of copper to form a trench wiring, or a so-called dual damascene method in which trench portions and opening portions (holes) formed in bottoms of the trench portions are filled with a wiring material constituted of copper to form a trench wiring and viaholes integrally. The opening portion (hole) and the trench portion will be referred to as "concave portion", hereinafter.

As a method of accurately filling the concave portions with copper, an electroplating method has been attracting attention in recent years. A copper film formed by an electroplating method has a low concentration of impurities and has a low resistance. It is therefore advantageous to use copper as an electrically conductive material or a wiring material for an increase in the speed of a semiconductor device. However, filling of the concave portions with copper

greatly depends upon step coverage of an underlayer (seed layer) required for forming a copper layer by an electroplating method. That is, when the concave portions are filled with copper by an electroplating method, the seed layer is required to have sufficiently good step coverage.

Conventionally, a copper layer having a thickness of approximately 100 nm formed by a sputtering method is used as a seed layer (see monthly journal "Semiconductor World", December, 1997, page 192).

However, a seed layer formed by a sputtering method is poor in step coverage, and it is difficult to form a seed layer in the concave portions uniformly in many cases. As a result, when a copper layer is formed on the seed layer by an electroplating method, the growth rate of the copper layer is non-uniform, and there arises the problem that the concave portions cannot be reliably filled with the copper layer or that voids in the copper layer within the concave portion are liable to arise.

OBJECT AND SUMMARY OF THE INVENTION

It is therefore an object of the present invention to provide a process for the production of a semiconductor device, which permits the formation of highly reliable connection holes and/or a trench wiring by reliably filling concave (recess) portions such as opening portions (holes) and/or trench portions with an electrically conductive material according to an electroplating method.

The above object is achieved by a process for the production of a semiconductor device, provided by the present invention, which comprises the steps of

(A) forming a concave portion in an insulating interlayer formed on a substrate so that part of the substrate is exposed in a bottom of the concave portion,

(B) forming a first electrically conductive

layer on the insulating interlayer including an inside of the concave portion, by an electroless plating method, and

(C) forming a second electrically conductive layer on the first electrically conductive layer by an electroplating method, to fill the concave portion with the second electrically conductive layer.

The term "concave portion" as used herein generically refers to an opening portion (a hole), a trench portion or a combination of a trench portion with an opening portion (a hole) formed in the bottom of the trench portion.

The term "electroless plating method" means a chemical-reduction plating in which metal ions in a plating solution are reduced and precipitated with a chemical, and it is also called "chemical plating".

The first electrically conductive layer functions as a seed layer for forming the second electrically conductive layer by an electroplating method. In addition, the first electrically conductive layer also functions as a cathode for forming the second electrically conductive layer by an electroplating method. The first electrically conductive layer can be a layer which is continuously formed at least on the insulating interlayer (including the inside of the concave portion) on which the second electrically conductive layer is to be formed. Further, it is sufficient if the thickness of the first electrically conductive layer is equal to, or greater than, the thickness of a mono-molecular layer of atoms constituting the first electrically conductive layer. When the thickness of the first electrically conductive layer is too large, a portion in the vicinity of the top end portion (corner portion) of the concave portion may swell when the first electrically conductive layer is formed. As a result, when the second electrically conductive layer is formed on the first electrically

conductive layer by an electroplating method, voids may arise in the second electrically conductive layer within the concave portion under some electroplating conditions. Therefore, the thickness of the first electrically conductive layer is preferably 100 nm or less, more preferably 5 nm to 100 nm, particularly preferably 5 nm to 50 nm.

The first electrically conductive layer and the second electrically conductive layer may be constituted of the same material, or they may be constituted of different materials so long as the second electrically conductive layer can be formed by an electroplating method without any problem. The material for the first electrically conductive layer includes Cu, Ni, Ni-based alloys (e.g., Ni-Co, Ni-Co-B, Ni-Co-P, Ni-Fe-P and Ni-W-P), Pt, Ti, Cr, Co, Co-based alloys (e.g., Co-Fe-P, Co-W-P, Co-Sn-P, Co-Zn-P and Co-Mn-P), Pd, Ag, Au, Zn, Sn, Rh, TiN/Ti, TiN/Rh, TiN/Pt, Zr, Hf, Ta, Mo, W, In, Ge and Pb. The material for the second electrically conductive layer includes Cu, Ag and Pt. When the first electrically conductive layer has a two layer structure as shown by the above TiN/Ti, etc., the material before "/" forms a layer on the second electrically conductive layer side, and the material after "/" forms a layer on the insulating interlayer side. "/" in a layer structure is also used in this sense hereinafter.

The first electrically conductive layer constituted of some material sometimes has a co-function as an anti-diffusion layer (also called a barrier layer) for preventing the diffusion of atoms constituting the second electrically conductive layer into the insulating interlayer. In this case, no anti-diffusion layer is required. When the first electrically conductive layer is constituted of some material, the process for the production of a semiconductor device, provided by the present invention, preferably further includes the step

of forming an anti-diffusion layer on the insulating interlayer including the inside of the concave portion, prior to the formation of the first electrically conductive layer, for preventing the diffusion of atoms constituting the first electrically conductive layer and/or atoms constituting the second electrically conductive layer into the insulating interlayer. The material for the anti-diffusion layer includes Ti, TiN, TiW, TiSiN, W, WN, WSiN, Rh, Pt, Ta, TaN and TaSiN. Further, the anti-diffusion layer may have a two layer structure of TiN/Ti, TiN/Rh, TiN/Pt or TaN/Ta or a three layer structure of Ta/TaN/Ta. Of these, the anti-diffusion layer is preferably constituted of a material selected from the group consisting of TiN, TiN/Ti, Ta, TaN, TaN/Ta and Ta/TaN/Ta. The anti-diffusion layer can be formed, for example, by a sputtering method or a CVD method. When the second electrically conductive layer is formed directly on the anti-diffusion layer constituted of the above material, the second electrically conductive layer may not be formed on the anti-diffusion layer or the adhesion between the anti-diffusion layer and the second electrically conductive layer may be poor in some cases.

The substrate (substratum) includes a silicon semiconductor substrate, an insulating layer (lower insulating layer or substratum insulating layer) formed on, for example, a silicon semiconductor substrate, and a combination of an insulating layer (lower insulating layer or substratum insulating layer) formed on, for example, a silicon semiconductor substrate with a lower-layer wiring (substratum wiring) formed on or in the above insulating layer or with connection holes formed in the above insulating layer. The material for forming the insulating interlayer (interlayer dielectric, ILD) includes SiO_2, SiN, SiON, SiOF, SiC, organic SOG having a dielectric constant k ($= \varepsilon/\varepsilon_0$), e.g., of 3.5 or less and insulating materials having a low dielectric

constant such as polyimide resins and fluorine resins (e.g., fluorocarbon, amorphous tetrafluoroethylene, polyaryl ether, fluoroaryl ether, fluoropolyimide, parylene, benzocyclobutene, amorphous carbon, cycloperfluorocarbon polymer and fluorofullerene). Further, the insulating interlayer may have a multi-layered structure constituted of the above materials.

The present invention can be applied to the process for the production of various semiconductor devices, specifically to the production, for example, of CMOS LSI, MOS LSI, bipolar LSI and bipolar CMOS LSI. Further, it can be applied to the production of a solid state image sensing device (image element) and a thin film transistor.

According to the process for the production of a semiconductor device, provided by the present invention, the first electrically conductive layer which works as a seed layer for forming the second electrically conductive layer by an electroplating method is formed by an electroless plating method. As compared with a conventional method where the first electrically conductive layer is formed by a sputtering method or a CVD method, therefore, the first electrically conductive layer can be formed in the concave portions in a conformal state and uniformly with excellent step coverage.

Further, the second electrically conductive layer is formed on the first electrically conductive layer by an electroplating method. The basis principle of the electroplating is as follows. That is, in the electroplating, the substrate (e.g., silicon semiconductor substrate) on which the first electrically conductive layer is formed is immersed in a plating bath, and an electric field is applied using the first electrically conductive layer as a cathode and an electrode plate (bar) in the plating bath as an anode. Cations in the plating bath adhere to the substrate side

under the function of the electric field, whereby the second electrically conductive layer is deposited on the first electrically conductive layer. Since the first electrically conductive layer has been formed in a conformal state and uniformly with excellent step coverage, the growth rate of the second electrically conductive layer on the first electrically conductive layer comes to be uniform. As a result, the concave portions can be reliably filled with the second electrically conductive layer.

BRIEF DESCRIPTION OF THE DRAWINGS

Figs. 1A, 1B and 1C are schematic partial cross-sectional views of an insulating interlayer, etc., for explaining the process for the production of a semiconductor device in Example 1.

Figs. 2A and 2B, following Fig. 1C, are schematic partial cross-sectional views of the insulating interlayer, etc., for explaining the process for the production of a semiconductor device in Example 1.

Figs. 3A and 3B are schematic partial cross-sectional views of an insulating interlayer, etc., for explaining the process for the production of a semiconductor device in Example 2.

Figs. 4A and 4B, following Fig. 3B, are schematic partial cross-sectional views of the insulating interlayer, etc., for explaining the process for the production of a semiconductor device in Example 2.

Figs. 5A and 5B are schematic partial cross-sectional views of an insulating interlayer, etc., for explaining the process for the production of a semiconductor device in Example 3.

Figs. 6A and 6B, following Fig. 5B, are schematic partial cross-sectional views of the insulating interlayer, etc., for explaining the process

for the production of a semiconductor device in Example 3.

Figs. 7A and 7B, following Fig. 6B, are schematic partial cross-sectional views of the insulating interlayer, etc., for explaining the process for the production of a semiconductor device in Example 3.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

The process for the production of a semiconductor device, provided by the present invention, will be explained in details with reference to the drawings hereinafter.

Example 1

In the process for the production of a semiconductor device in Example 1, the concave portions are opening portions (holes), and so-called viaholes are formed in an insulating interlayer (ILD). The substrate (substratum) comprises a combination of a lower insulating layer (substratum insulating layer) formed on a silicon semiconductor substrate with a lower-layer wiring (substratum wiring) formed on the lower insulating layer. Further, a wiring is to be formed on the insulating interlayer (surface of the insulating interlayer) integrally with the viaholes. The process for the production of a semiconductor device in Example 1 will be explained below with reference to Figs. 1A, 1B, 1C, 2A and 2B showing schematic partial cross-sectional views of the insulating interlayer and the like.

[Step-100]

First, a lower insulating layer 11 of SiO_2 is formed, by a CVD method, on a silicon semiconductor substrate (not shown) in which elements (not shown) such as transistors, etc., are formed according to a general process for producing a semiconductor device. Then, a lower-layer wiring 12 is formed on the lower insulating layer 11. The lower-layer wiring 12 has a structure,

for example, in which a TiN/Ti layer 12A as a barrier layer, a copper layer 12B and a TiN layer 12C are consecutively formed, whereby there can be formed a substrate 10 (see Fig. 1A) which comprises a combination of the lower insulating layer 11 with the lower-layer wiring 12 formed on the lower insulating layer 11. The TiN layer 12C works as an anti-reflection layer required in a lithography step. The above lower-layer wiring 12 extends in the perpendicular direction with regard to the paper surface of the drawing.

[Step-110]

Then, an insulating interlayer (ILD) 13 having a thickness, e.g., of 0.8 μm is formed of SiO_2 on the substrate 10 by a plasma-assisted CVD method using tetraethyl orthosilicate (TEOS). Then, an opening portion (hole) 14 is formed in the insulating interlayer 13 positioned on the lower-layer wiring 12 according to a lithography technique and an etching technique. In this manner, in the insulating interlayer 13 formed on the substrate 10, there can be formed the opening portion (concave portion) 14 so that part of the substrate (the lower-layer wiring 12) is exposed in the bottom of the opening portion 14 (see Fig. 1B).

The above SiO_2 may be replaced with an insulating material having a low dielectric constant. In this case, the insulating interlayer can be formed by forming a layer of a material having a low dielectric constant on the substrate by a spin coating method and curing the material having a low dielectric constant at a temperature, e.g., of approximately 400 °C. In this case, further, an insulating layer of SiO_2 may be formed, and an insulating layer of a material having a low dielectric constant may be formed thereon, so that the insulating interlayer comprises two insulating layers.

[Step-120]

Then, an anti-diffusion layer 15 having a thickness, e.g., of 50 nm is formed, e.g., of TiN on the

insulating interlayer 13 including the inside of the opening portion 14, for example, by a sputtering method. Table 1 shows one example of conditions for forming such an anti-diffusion layer 15. Otherwise, the anti-diffusion layer 15 having a thickness, e.g., of 30 nm may be formed, e.g., of TaN. Table 2 shows conditions for forming such an anti-diffusion layer 15.

Table 1

Target	Ti
Process gas	Ar/N_2 = 60/120 SCCM
Pressure	0.67 Pa
DC power	8 kW
Formation temperature	200 °C

Table 2

Target	Ta
Process gas	Ar/N_2 = 20/70 SCCM
Pressure	0.3 Pa
DC power	12 kW
Formation temperature	200 °C

[Step-130]

After catalyst treatment and accelerator treatment are carried out, a first electrically conductive layer 16 which works as a seed layer is formed, by an electroless plating method, on the insulating interlayer 13 including the inside of the opening portion (concave portion) 14, more specifically, on the anti-diffusion layer 15 in Example 1 (see Fig. 1C). The first electrically conductive layer 16 is constituted of copper (Cu) and has a thickness, for example, of 50 nm. Table 3 shows an example of the conditions for forming the first electrically conductive layer 16. The plating solution contains small amounts

of a stabilizer and a wetting agent.

Table 3

Plating solution	Copper sulfate ($CuSO_4 \cdot 5H_2O$)	7 g/liter
	Formalin (37 % HCHO)	20 ml/liter
	Sodium hydroxide (NaOH)	10 g/liter
	Sodium potassium tartarate	20 g/liter
Plating bath temperature	50 °C	

The first electrically conductive layer 16 formed by an electroless plating method is excellent in step coverage and has a uniform thickness. Further, the crystal grains of the above first electrically conductive layer 16 generally has the closest packing atomic plane such as (111) plane orientation and therefore has excellent electromigration durability.

[Step-140]

Then, a second electrically conductive layer 17 is formed on the first electrically conductive layer 16 by an electroplating method, to fill the opening portion (concave portion) 14 with the second electrically conductive layer 17, whereby a viahole 18 is completed (see Fig. 2A). The thickness of the second electrically conductive layer 17 constituted of copper can be a thickness sufficient for completely filling the opening portion 14. Table 4 shows an example of the conditions for forming the second electrically conductive layer 17.

Table 4

Plating solution	$CuSO_4 \cdot 5H_2O$
Plating bath temperature	30 °C
Voltage	10 V
Current density	20 A/dm^2
Anode plate	Cu plate

[Step-150]

Then, the second electrically conductive layer 17 constituted of copper, the first electrically conductive layer 16 constituted of copper and the anti-diffusion layer 15 constituted of TiN are patterned according to a lithography technique and a dry etching technique to form a desired wiring pattern (see Fig. 2B). Table 5 shows an example of the drying etching conditions. In the above manner, an upper-layer wiring 19 is formed, on the insulating interlayer 13, integrally with the viahole 18.

Table 5

Etching gas	$SiCl_4/N_2$ = 10/100 SCCM
Pressure	26 Pa
RF power	500 W
Etching temperature	300 °C

Thereafter, an upper insulating layer, a wiring protective layer and the like are formed according to a general process for the production of a semiconductor device, to complete the semiconductor device.

Alternatively, in [Step-150], a wiring may be formed as follows. The second electrically conductive layer 17, the first electrically conductive layer 16 and the anti-diffusion layer 15 on the insulating interlayer 13 are removed according to a CMP (Chemical/Mechanical

Polishing) method under conditions, for example, shown in Table 6, a layer of a wiring material is formed on the insulating interlayer 13, for example, by a sputtering method, and the layer of a wiring material is patterned to form the upper-layer wiring. The method of removing the second electrically conductive layer 17, the first electrically conductive layer 16 and the anti-diffusion layer 15 shall not be limited to a CMP method, and they may be removed by an etch back method.

Table 6

Polishing material	Slurry prepared by suspending $FeNO_3$ in aqueous hydrogen peroxide
Flow rate of polishing material	20 SCCM
Polishing head pressure	0.28 kgf/cm^2
Number of turn of substrate	20 rpm
Number of turn of head	20 rpm

Example 2

In the process for the production of a semiconductor device in Example 2, the concave portions are trench portions. Viaholes are formed in a lower insulating interlayer, and then a trench wiring connected to the viaholes are formed in an insulating interlayer. That is, Example 2 is concerned with a single damascene method. The viaholes may be formed in the same manner as in Example 1, or may be formed by a different method. A substrate comprises a combination of a lower insulating interlayer formed on a lower insulating layer with a viahole formed in the lower insulating interlayer. The process for the production of a semiconductor device in Example 2 will be explained below with reference to Figs. 3A, 3B, 4A and 4B showing schematic partial cross-sectional views of the

insulating interlayer and the like. In Example 2, the anti-diffusion layer and the insulating interlayer on which a trench wiring is to be formed will be referred to as "second anti-diffusion layer" and "second insulating interlayer" for clearly distinguishing them from the anti-diffusion layer and the insulating interlayer in Example 1. Further, the lower insulating interlayer which constitutes the substrate and in which the viahole is formed will be referred to as "the insulating interlayer 13".

[Step-200]

First, [Step-100] to [Step-140] in Example 1 are carried out, and then the second electrically conductive layer 17, the first electrically conductive layer 16 and the anti-diffusion layer 15 on the insulating interlayer 13 are removed (see Fig. 3A) according to a CMP method under conditions shown in Table 6, whereby a viahole 18 is formed. The method of removing the second electrically conductive layer 17, the first electrically conductive layer 16 and the anti-diffusion layer 15 on the insulating interlayer 13 shall not be limited to the CMP method, and they may be removed by an etch back method.

Further, the method of forming the viaholes in Example 2 shall not be limited to the above formation method, and they may be formed, for example, by a so-called blanket CVD tungsten method. The blanket CVD tungsten method refers to a method in which a Ti layer and TiN layer are consecutively formed on the insulating interlayer 13 including the inside of the opening portion 14 formed in the insulating interlayer 13, then, a tungsten layer is formed on the insulating interlayer 13 including the opening portion 14 by a CVD method and then the tungsten layer, the TiN layer and the Ti layer on the insulating interlayer 13 are removed.

[Step-210]

Then, a second insulating interlayer 23 having

a thickness, for example, of 0.6 μm is formed of SiO_2 on the entire surface by a CVD method. Then, a trench portion 24 is formed in the second insulating interlayer 23 on the viahole 18 according to a lithography technique and a dry etching technique (see Fig. 3B). The above trench portion 24 extends in the perpendicular direction with regard to the paper surface of the drawing.

[Step-220]

Then, a second anti-diffusion layer 25 having a thickness, for example, of 50 nm is formed of TiN on the second insulating interlayer 23 including the inside of the trench portion 24 under the conditions shown in Table 1. Then, a first electrically conductive layer 26 is formed on the second insulating interlayer 23 including the inside of the trench portion (concave portion) 24, more specifically, on the second anti-diffusion layer 25, by an electroless plating method. The first electrically conductive layer 26 works as a seed layer, and it has a thickness of 50 nm and is constituted of copper (Cu). The first electrically conductive layer 26 can be formed under the conditions shown in Table 3.

[Step-230]

Then, a second electrically conductive layer 27 is formed on the first electrically conductive layer 26 by an electroplating method under the conditions shown in Table 4 as an example, to fill the trench portion (concave portion) 24, with the second electrically conductive layer 27 (see Fig. 4A). The thickness of the second electrically conductive layer 27 constituted of copper (Cu) can be a thickness sufficient for completely filling the trench portion 24.

[Step-240]

Then, the second electrically conductive layer 27, the first electrically conductive layer 26 and the second anti-diffusion layer 25 on the second insulating

interlayer 23 are removed (see Fig. 4B) by a CMP method under the conditions shown in Table 6, whereby a trench wiring 28 in which the trench portion (concave portion) 24 is filled with the second electrically conductive layer 27 is completed. The method of removing the second electrically conductive layer 27, the first electrically conductive layer 26 and the second anti-diffusion layer 25 on the second insulating interlayer 23 shall not be limited to the CMP method, and they may be removed, for example, by an etch back method.

Thereafter, an upper insulating layer, a wiring protective layer and the like are formed according to a general process for the production of a semiconductor device, to complete the semiconductor device.

Example 3

In the process for the production of a semiconductor device in Example 3, a concave portion is a combination of a trench portion with an opening portion. And, viaholes and a trench wiring are integrally formed in an insulating interlayer. That is, Example 3 is concerned with a dual damascene method. Further, the substrate comprises a combination of a lower insulating layer formed on a silicon semiconductor substrate with a lower-layer wiring formed on the lower insulating layer. The process for the production of a semiconductor device in Example 3 will be explained below with reference to Figs. 5A, 5B, 6A, 6B, 7A and 7B showing schematic partial cross-sectional views of the insulating interlayer and the like.

[Step-300]

First, [Step-100] in Example 1 is carried out.

[Step-310]

Then, a first insulating layer 33A having a thickness, for example, of 0.8 μm is formed of SiO_2 on a substrate 10 according to a plasma-assisted CVD method using tetraethyl orthosilicate (TEOS). Then, a second

insulating layer 33B having a thickness, for example, of 50 nm is formed of SiN on the first insulating layer 33A according to, for example, a low-pressure CVD (LP-CVD) method or a plasma-assisted CVD method. Table 7 shows an example of conditions for forming the second insulating layer 33B by a plasma-assisted CVD method.

Table 7

Reaction gas	$SiH_4/NH_3/N_2$ = 265/100/4000 SCCM
Pressure	565 Pa
Temperature	400 °C

Then, a hole portion 33b having a diameter of 0.3 μm is formed in the second insulating layer 33B according to a lithography technique and a dry etching technique (see Fig. 5A). Then, a third insulating layer 33C having a thickness, for example, of 0.5 μm is formed on the entire surface, for example, by a CVD method. The material for the third insulating layer 33C can be the same as that for the first insulating layer 33A. In this manner, an insulating interlayer 33 having a three-layered structure can be formed. Then, the surface of the insulating interlayer 33 is flattened or smoothened by polishing it, for example, by a CMP method.

Then, an etching mask is formed of a resist material on the insulating interlayer 33 according to a lithography technique, and the third insulating layer 33C is etched through the etching mask, for example, by an RIE (Reactive Ion Etching) method, whereby a trench portion 34A is formed in the third insulating layer 33C (see Fig. 5B). The trench portion 34A extends in a perpendicular direction with regard to the paper surface of the drawing. When the third insulating layer 33C is etched, the second insulating layer 33B constituted of SiN works as an etching stopper. Further, after the second insulating layer 33B is exposed, the first

insulating layer 33A is etched with the second insulating layer 33B being an etching mask, whereby an opening portion (hole) 34B is formed in the bottom of the trench portion 34A (see Fig. 6A). In this manner, the opening portion 34B and the trench portion 34A which constitute the concave portion can be formed in the insulating interlayer 33 formed on the substrate 10 so that part of the substrate 10, more specially, part of the lower-layer wiring 12 is exposed in the bottom of the concave portion, more specially, in the bottom of the opening portion 34B. Table 8 shows an example of etching conditions for forming the first and third insulating layers 33A and 33C constituted of SiO_2. Further, Table 9 shows an example of conditions for etching the first and third insulating layers 33A and 33C constituted of organic material(s) having a low dielectric constant.

Table 8

Etching gas	C_4F_8 = 50 SCCM
Pressure	2 Pa
RF power	1.2 kW

Table 9

Etching gas	$CHF_3/O_2/He$ = 5/50/200 SCCM
Temperature	-10 °C
RF power	0.5 kW

Alternatively, the opening portion which is opened through the third insulating layer 33C, the second insulating layer 33B and the first insulating layer 33A may be formed first according to a lithography technique and a dry etching technique, and then the trench portion may be formed in the third insulating layer 33C according to a lithography technique and a dry

etching technique. In this case, the second insulating layer 33B constituted of SiN works as an etching stopper when the trench portion is formed in the third insulating layer 33C.

[Step-320]

Then, an anti-diffusion layer 35 having a thickness, for example, of 50 nm is formed of TiN on the insulating interlayer 33 including the inside of the trench portion 34A and the inside of the opening portion 34B according to, for example, a sputtering method. The anti-diffusion layer 35 can be formed, for example, under conditions shown in Table 1.

[Step-330]

Then, a first electrically conductive layer 36 is formed on the insulating interlayer 33 including the insides of the trench portion 34A and the opening portion 34B which constitute the concave portion, more specifically, on the anti-diffusion layer 35 in Example 3, according to an electroless plating method (see Fig. 6B). The first electrically conductive layer 36 works as a seed layer, and it has a thickness of 50 nm and is constituted of copper (Cu). The first electrically conductive layer 36 can be formed, for example, under conditions shown in Table 3.

[Step-340]

Then, a second electrically conductive layer 37 is formed on the first electrically conductive layer 36 by an electroplating method, to fill the trench portion 34A and the opening portion 34B (which constitute the concave portion) with the second electrically conductive layer 37, whereby a viahole 38B is completed (see Fig. 7A). The thickness of the second electrically conductive layer 37 constituted of copper (Cu) can be a thickness sufficient for completely filling the trench portion 34A and the opening portion 34B, for example, 1.0 μm. The second electrically conductive layer 37 can be formed, for example, under

the conditions shown in Table 4.

[Step-350]

Then, the second electrically conductive layer 37, the first electrically conductive layer 36 and the anti-diffusion layer 35 on the insulating interlayer 33 are removed according to a CMP method under the conditions shown in Table 6, whereby there is completed a trench wiring 38A in which the trench portion (concave portion) 34A is filled with the second electrically conductive layer 37 (see Fig. 7B). The above trench wiring 38A and the viahole 38B are integrally formed.

Thereafter, an upper insulating layer, a wiring protective layer and the like are formed according to a general process for the production of a semiconductor device, to complete the semiconductor device.

Example 4

In each Example explained above, the first electrically conductive layer is constituted of copper (Cu). In Example 4, the first electrically conductive layer is constituted of nickel (Ni).

The crystal size of copper in a copper layer formed by an electroless copper plating method is liable to be relatively large. When the thickness of the first electrically conductive layer is designed to be small, therefore, it is sometimes difficult to form the first electrically conductive layer having a uniform thickness. When the first electrically conductive layer having a uniform thickness is constituted of copper, therefore, the first electrically conductive layer is required to have a thickness of several tens nm. When a layer is formed by an electroless plating, the layer grows isotropically in principle, and with an increase in the thickness of the first electrically conductive layer, the opening portion is decreased in diameter or the trench portion is decreased in width. As a result, when the second electrically conductive layer is formed, the

substantial aspect ratio of the concave portion increases, it is difficult to supply the inside of the concave portion with a fresh electroplating solution, and voids are liable to arise in the second electrically conductive layer within the concave portion.

For overcoming the above problem, for example, an electroless nickel plating method can be employed for forming the first electrically conductive layer having a small thickness. A nickel crystal grains formed by the electroless nickel plating method has the form or shape of a pillar, and the first electrically conductive layer having a small thickness can be uniformly formed with excellent step coverage. As a result, the increase in the substantial aspect ratio of the concave portion can be prevented when the second electrically conductive layer is formed. There can be therefore avoid the problem that voids are liable to arise in the second electrically conductive layer within the concave portion. Further, the control of the temperature and the composition of an electroless nickel plating bath is easier than the control of those of an electroless copper plating bath, and the electroless nickel plating is advantageously more feasible for the automation of formation of the first electrically conductive layer. Further, when the first electrically conductive layer is constituted of nickel, it can prevent the diffusion, e.g., of copper atoms constituting the second electrically conductive layer into the insulating interlayer, and the formation of the anti-diffusion layer can be omitted in some cases. In other words, the first electrically conductive layer of nickel can be formed directly on the insulating interlayer including the inside of the concave portion, by an electroless nickel plating method.

A 10 nm thick first electrically conductive layer of nickel can be formed, after catalyst treatment with Catalyst 9F (trade name, supplied by Shipley Far

East Ltd.) and accelerator treatment with Accelerator 240 (trade name, supplied by Shipley Far East Ltd.) are carried out, by immersing the substrate in an electroless nickel plating bath (e.g., electroless nickel plating solution which is a mixture of CP1, CP2, CP3, CP4 and CP5 (trade names, supplied by Sony Corporation)) at a plating bath temperature of 50 °C with ultrasonic for 1 minute.

The present invention has been explained with Examples, while the present invention shall not be limited thereto. Various kinds of the materials and the conditions which are explained in Examples are presented for illustrative purposes and may be changed as required, and the structures of the semiconductor devices are also presented for illustrative purposes.

For example, the first electrically conductive layer may be constituted of a Ti layer formed by an electroless plating method. The plating solution in this case can be selected from a plating solution prepared by adding PdS as a catalytic reactant substance to titanium sulfate or a plating solution prepared by adding HCHO and H_2O to titanium sulfate. Further, the first electrically conductive layer may be constituted of a TiN layer formed by an electroless plating method. The plating solution in this case can be selected from a plating solution prepared by adding PdS as a catalytic reactant substance to titanium sulfate containing NH_4OH or HNO_3 or a plating solution prepared by adding HCHO and NH_4OH to titanium sulfate.

The second electrically conductive layer may be constituted of silver (Ag). Table 10 shows an example of conditions for forming the second electrically conductive layer of silver by an electroplating method. Further, the second electrically conductive layer may be constituted of platinum (Pt). Table 11 shows an example of conditions for forming the second electrically conductive layer of platinum by an

electroplating method.

Table 10

Plating solution	Silver nitrate Sodium carbonate Sodium phosphate
Plating bath temperature	30 °C
Voltage	10 V
Current density	30 mA/dm^2

Table 11

Plating solution	Platinic acid chloride	4 g/liter
	Ammonium phosphate	20 g/liter
	Sodium phosphate	100 g/liter
Plating bath temperature	80 °C	
Voltage	4 V	
Current density	1 mA/dm^2	

As an anti-oxidation layer for a trench wiring constituted of copper (Cu), for example, a capping layer (wiring protective layer) may be formed of TiN on the surface of the trench wiring. The capping layer can be formed by forming a TiN layer having a thickness of 30 nm on the entire surface under sputtering conditions shown in Table 12 and then patterning the TiN layer according to a lithography technique and a dry etching technique. Table 13 shows dry etching conditions.

Table 12

Target	Ti
Process gas	Ar/N_2 = 30/100 SCCM
Pressure	0.67 Pa
Temperature	150 °C

Table 13

Etching gas	BCl_3/Cl_2 = 60/90 SCCM
Pressure	2 Pa
RF power	1.2 kW

According to the process for the production of a semiconductor device, provided by the present invention, the first electrically conductive layer which works as a seed layer is formed in the concave portion by an electroless plating method, so that the first electrically conductive layer can be uniformly formed with excellent step coverage. And, the second electrically conductive layer can be formed on the first electrically conductive layer which works as a seed layer, by an electroplating method, so as to have a sufficient thickness. Even when the concave portion has a high aspect ratio, therefore, the concave portions can be filled excellently and can be filled highly accurately, so that the failure in filling the concave portions can be prevented. There can be therefore obtained connection holes, a trench wiring or a combination of a trench wiring with connection holes in which concave portions are completely filled with the second electrically conductive layer. Moreover, when the second electrically conductive layer is constituted of, for example, copper (Cu), the second electrically conductive layer has a low specific resistance and excellent durability against electromigration, so that highly reliable semiconductor devices operable at a high speed can be produced at high yields.

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WHAT IS CLAIMED IS:

1. A process for the production of a semiconductor device, comprising the steps of

(A) forming a concave portion in an insulating interlayer formed on a substrate so that part of the substrate is exposed in a bottom of the concave portion,

(B) forming a first electrically conductive layer on the insulating interlayer including an inside of the concave portion, by an electroless plating method, and

(C) forming a second electrically conductive layer on the first electrically conductive layer by an electroplating method, to fill the concave portion with the second electrically conductive layer.

2. The process according to claim 1, wherein the first electrically conductive layer is formed to have a thickness equal to, or greater than, the thickness of a mono-molecular layer of atoms constituting the first electrically conductive layer.

3. The process according to claim 2, wherein the first electrically conductive layer is formed to have a thickness of 100 nm or less.

4. The process according to claim 3, wherein the first electrically conductive layer is formed to have a thickness of 5 nm to 100 nm.

5. The process according to claim 4, wherein the first electrically conductive layer is formed to have a thickness of 5 nm to 50 nm.

6. The process according to claim 1, wherein the first electrically conductive layer and the second electrically conductive layer are constituted of the

same material.

7. The process according to claim 1, wherein the first electrically conductive layer and the second electrically conductive layer are constituted of different materials.

8. The process according to claim 1, wherein the first electrically conductive layer is constituted of a material selected from the group consisting of Cu, Ni, Ni-based alloy, Pt, Ti, Cr, Co, Co-based alloy, Pd, Ag, Au, Zn, Sn, Rh, TiN/Ti, TiN/Rh and TiN/Pt.

9. The process according to claim 1, wherein the second electrically conductive layer is constituted of a material selected from the group consisting of Cu, Ag and Pt.

10. The process according to claim 1, which further comprises the step of forming, prior to the formation of the first electrically conductive layer, an anti-diffusion layer on the insulating interlayer including the inside of the concave portion for preventing the diffusion of atoms constituting the first electrically conductive layer and/or atoms constituting the second electrically conductive layer into the insulating interlayer.

11. The process according to claim 10, wherein the anti-diffusion layer is constituted of a material selected from the group consisting of TiN, TiN/Ti, Ta, TaN, TaN/Ta and Ta/TaN/Ta.

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