

FEFET DEVICE, SYSTEM, AND METHOD OF MANUFACTURING

BACKGROUND

Relevant Field

[0001] The present disclosure relates to transistors with ferroelectric materials. In particular, the present disclosure relates to ferroelectric transistor devices, systems, and methods of manufacture.

Description of Related Art

[0002] Field-effect transistors (“FETs”) are transistors that utilize an electric field to control or modify current flowing between a source terminal and a drain terminal. The electric field is generated by a voltage applied to a gate terminal of the FET. FETs use electrons and/or holes as charge carriers to achieve this effect. FETs can be predominantly majority-charge-carrier devices or minority-charge-carrier devices. The voltage applied to the gate of the FET creates an active channel through which the charge carriers flow from the source terminal to the drain terminal. The non-linear impedance through this channel can be varied by applying different voltages to the gate terminal relative to the source and/or drain terminals. However, these characteristics are ephemeral because as soon as the voltage is no longer applied, the FET quickly returns to its original, resting state.

[0003] Ferroelectric field-effect transistors (“FeFETs”) are FETs that include a ferroelectric material. Ferroelectric materials are materials that have electric polarization (or polarization density). The electric field polarization of the ferroelectric material can be used to create an active channel within the FeFET. By utilizing this property of the ferroelectric material, the electric field polarization in the ferroelectric material may be used to retain the FeFET’s state in the absence of any electrical bias. That is, the FeFET can retain information in the ferroelectric material without having any external power applied to it. This feature makes FeFETs suitable for non-volatile memory applications that involve discrete or continuous values.

SUMMARY

[0004] A system of one or more computers can be configured to perform particular operations or actions by virtue of having software, firmware, hardware, or a combination of them installed on the system that in operation causes or cause the system to perform the actions. One or

more computer programs can be configured to perform particular operations or actions by virtue of including instructions that, when executed by data processing apparatus, cause the apparatus to perform the actions.

[0005] In one general aspect, an integrated circuit device may include a first layer having a semiconductor substrate. The integrated circuit device may also include a second layer disposed parallel to the first layer. The second layer has an insulating layer and a transistor disposed on the insulating layer. The transistor having: a source electrode disposed on the insulating layer along a first length parallel to the insulating layer; a drain electrode disposed on the insulating layer parallel to the source electrode, the drain electrode disposed a predetermined distance from the source electrode; a channel structure having a first portion, a second portion, and a third portion, the first portion is disposed parallel to the source electrode along the first length, the second portion disposed parallel to the insulating layer and adjacent to the first portion, the third portion disposed parallel to the drain electrode and adjacent to the second portion; a ferroelectric structure having a first portion, a second portion, and a third portion, the first portion of the ferroelectric structure disposed parallel to the first portion of the channel structure, the second portion of the ferroelectric structure disposed parallel to the second portion of the channel structure, the third portion of the ferroelectric structure disposed parallel to the third portion of the channel structure, where the ferroelectric structure is configured to have at least one polarization; and a gate structure disposed within a space defined by the first, second, and third portions of the ferroelectric structure.

[0006] Implementations may include one or more of the following features. The first layer may be a front-end-of-line layer. The second layer may be a back-end-of-line layer. The second layer may include a three-dimensional stack of memory cells including the transistor. The transistor may be configured to store a Neuromorphic value. The ferroelectric structure may be configured to have a selectable polarization such that the polarization corresponds to a stored value. The stored value may be a discrete value or a continuous value. The second insulating layer can be disposed on the first and third portions of the channel structure, on the first and second portions of the ferroelectric structure, and on the gate structure. The source electrode may have a height defined by a second length extending orthogonally from the insulating layer such that the source electrode has a thickness defined by a third length orthogonal to the first length and the second length. A computer system may include an integrated circuit configured as an artificial intelligence accelerator.

[0007] In one general aspect, a method of manufacturing an integrated circuit may include forming an insulating layer. The method may also include forming a source electrode disposed

parallel to the insulating layer along a first length parallel to the insulating layer. The method may furthermore include forming a drain electrode disposed parallel to the insulating layer and parallel to the source electrode, the drain electrode disposed a predetermined distance from the source electrode. The method may in addition include forming a channel structure having a first portion, a second portion, and a third portion where the first portion is disposed parallel to the source electrode along the first length, the second portion is disposed along the insulating layer adjacent to the first portion, and the third portion is disposed parallel to the drain electrode and adjacent to the second portion. The method may moreover include forming a ferroelectric structure having a first portion, a second portion, and a third portion where the first portion of the ferroelectric structure is disposed parallel to the first portion of the channel structure, the second portion of the ferroelectric structure is disposed parallel to the second portion of the channel structure, and the third portion of the ferroelectric structure is disposed parallel to the third portion the channel structure. The ferroelectric structure is configured to have at least one polarization. The method may also include forming a gate structure disposed within a space defined by the first, second, and third portions of the ferroelectric structure. Other embodiments of this aspect include corresponding computer systems, apparatus, and computer programs recorded on one or more computer storage devices, each configured to perform the actions of the methods.

[0008] Implementations may include one or more of the following features. The method where the act of forming the channel structure includes depositing the channel structure using atomic layer deposition. The method where the act of forming the ferroelectric structure includes depositing the ferroelectric structure using atomic layer deposition. The method where the act of forming the gate structure may include: depositing the gate structure including an excess gate structure using atomic layer deposition; and removing the excess gate structure using chemical-mechanical planarization. The method may include: forming a second insulating layer; and forming at least one cooperation with at least one of: the source electrode, the drain electrode, and the gate structure. Implementations of the described techniques may include hardware, a method or process, or a computer tangible medium.

[0009] In one general aspect, an integrated circuit device may include an insulating layer. The integrated circuit device may also include a plurality of parallel electrodes each extending along a first direction parallel to the insulating layer where the plurality of parallel electrodes is arranged in spaced relation to each other to thereby have a predetermined space interposed between each adjacent pair of the plurality of parallel electrodes defining a plurality of spaces between each

adjacent pair of the plurality of parallel electrodes. The integrated circuit may furthermore include a plurality of channel structures each disposed within a space of the plurality of spaces where each channel structure is in cooperation with both of the adjacent pair of the plurality of parallel electrodes and the insulating layer. The integrated circuit may in addition include a plurality of ferroelectric structures each disposed adjacent to a respective one of the plurality of channel structures where each of the ferroelectric structures is configured to include a respective channel. The integrated circuit may moreover include a plurality of gate structures each disposed within the respective channel of the plurality of ferroelectric structures.

[0010] Implementations may include one or more of the following features. The integrated circuit may have at least one of the plurality of parallel electrodes is a drain-or-source electrode. A computer system may have a central processing unit; a memory in operative communication with the central processing unit; and an integrated circuit where the integrated circuit is configured as an artificial intelligence accelerator.

[0011] In one general aspect, a method of manufacture may include forming an insulating layer. The method may also include forming a plurality of parallel electrodes each extending along a first direction parallel to the insulating layer where the plurality of parallel electrodes are arranged in spaced relation to each other to thereby have a predetermined space interposed between each adjacent pair of the plurality of parallel electrodes defining a plurality of spaces between each adjacent pair of the plurality of parallel electrodes. The method may furthermore include forming a plurality of channel structures each disposed within a space of the plurality of spaces, each channel structure in cooperation with both of the adjacent pair of the plurality of parallel electrodes and the insulating layer. The method may in addition include forming a plurality of ferroelectric structures each disposed adjacent to a respective one of the plurality of channel structures where each of the ferroelectric structures is configured to include a respective channel. The method may moreover include forming a plurality of gate structures each disposed within the respective channel of the plurality of ferroelectric structures. Other embodiments of this aspect include corresponding computer systems, apparatus, and computer programs recorded on one or more computer storage devices, each configured to perform the actions of the methods.

[0012] Implementations may include one or more of the following features. The method may include the act of depositing an electrode using atomic layer deposition. The method may include the act of forming the plurality of channel structures includes depositing a channel structure using atomic layer deposition. The method may include the act of depositing a ferroelectric structure

using atomic layer deposition. The method may include: depositing a gate structure including an excess gate structure using atomic layer deposition; and removing the excess gate structure using chemical-mechanical planarization. The method may include: forming a second insulating layer; and forming at least one contact with at least one of a gate structure of the plurality of gate structures and an electrode of the plurality of parallel electrodes. Implementations of the described techniques may include hardware, a method or process, or a computer tangible medium.

BRIEF DESCRIPTION OF THE DRAWINGS

[0013] These and other aspects will become more apparent from the following detailed description of the various embodiments of the present disclosure with reference to the drawings wherein:

[0014] Fig. 1 shows a block diagram of an artificial intelligence accelerator that utilizes FeFET memory in accordance with an embodiment of the present disclosure;

[0015] Fig. 2 shows a diagram of a memory cell utilizing a FeFET transistor in accordance with an embodiment of the present disclosure;

[0016] Fig. 3 illustrates operating characteristics of the FeFET of Fig. 2 when used to store binary states in accordance with an embodiment of the present disclosure;

[0017] Fig. 4 illustrates operating characteristics of the FeFET of Fig. 2 when used to store a continuous value, such as a weight of a neuromorphic cell, in accordance with an embodiment of the present disclosure;

[0018] Fig. 5 shows a memory array utilizing FeFET transistors in accordance with an embodiment of the present disclosure;

[0019] Figs. 6-7 show FeFET transistors configured for miniaturization on a back-end-of-line portion of an integrated circuit semiconductor in accordance with an embodiment of the present disclosure;

[0020] Fig. 8 shows an array of bit cells formed by a plurality of FeFETs of Figs. 5-7 in accordance with an embodiment of the present disclosure;

[0021] Figs. 9A-9E illustrate a manufacturing process to manufacture the array of bit cells of Fig. 8 in accordance with an embodiment of the present disclosure;

[0022] Fig. 10 shows a flow chart diagram of a method to manufacture the array of bit cells as illustrated in Figs. 9A-9E in accordance with an embodiment of the present disclosure;

[0023] Figs. 11A-11F illustrate another manufacturing process to manufacture the array of bit cells of Fig. 8 in accordance with an embodiment of the present disclosure; and

[0024] Fig. 12 shows a flow chart diagram of a method to manufacture the array of bit cells illustrated in Figs. 11A-11F in accordance with an embodiment of the present disclosure.

DETAILED DESCRIPTION

[0025] Fig. 1 shows a block diagram of an Artificial Intelligence (“AI”) accelerator 100 that utilizes FeFET memory 112 in accordance with an embodiment of the present disclosure. The AI accelerator 100 may be implemented on a semiconductor device, a custom integrate circuit, an application-specific integrated circuit (“ASIC”), a graphics processing unit (“GPU”), a field-programmable gate array (“FPGA”), any device known to one of ordinary skill in the art, or some combination thereof. The AI accelerator 100 includes a processing element (“PE”) array 102 that performs the majority of AI computation. The PE array 102 performs the AI computations using a plurality of processing elements 110. These processing elements 110 may form a manycore processor where each processing element 110 performs AI calculations in parallel with the other processing elements 110. Additionally or alternatively, the processing elements 110 may include an arithmetic logic unit, a neuromorphic computation element, a processor, a multicore processor, a manycore processor, a reduced instruction set computer (“RISC”) processor, and/or other computation device known to one of ordinary skill in the relevant art.

[0026] The processing elements 110 may each be part of a neuromorphic circuit; for example, the processing elements 110 may each form a portion of an artificial neural network where each accompanying memory 112 is an analog memory configured to act as parameters for artificial neurons (e.g., weights), in some specific embodiments. Each processing element 110 and its respective memory 112 may form an in-memory processing architecture, e.g., to enable efficient and parallel execution of multiply-accumulate operations, in yet additional embodiments.

[0027] The memories 112 are implemented using FeFETs described in further detail below. The memories 112 may store binary data and/or may store analog data in some specific embodiments. Additionally or alternatively, the memories 112 may store a combination of binary and analog data in some embodiments.

[0028] The AI accelerator 100 may also include a shared memory 108. Computations computed by the PE array 102 may be stored and/or instructed by information stored on a shared memory 104 internal to the AI accelerator and/or shared memory 108 stored off of the AI accelerator 100. The shared memory 104 and/or the shared memory 108 may utilize the FeFET memory cells

as described herein. The AI accelerator 100 also includes a Network-on-Chip 106 for communicating with other devices, e.g., via TCP/IP, Ethernet, Wifi, etc.

[0029] Fig. 2 shows a diagram of a memory cell 200 utilizing a FeFET 202 in accordance with an embodiment of the present disclosure. The memory cell 200 also includes a program-signal circuit 206 and a sense circuit 204. The program-signal circuit 206 may apply one or more positive-voltage pulse signals or negative-voltage pulse signals to program the FeFET 202. The FeFET 202 includes a drain 210, a source 212, and a gate 208. However, because of the symmetry of the FeFET 202, the operation of the drain 210 and source 212 may be reversed.

[0030] The FeFET 202 may be powered by a Vread voltage that is relative to a voltage SL. The Vread voltage may be a ground, may be a fixed voltage, may be a programmable voltage, may be a variable voltage, may be coupled to a ground or a voltage source via another transistor (not shown), etc. Similarly, the SL reference may be a ground, may be a fixed voltage, may be a programmable voltage, may be a variable voltage, may be coupled to a ground or a voltage source via another transistor (not shown), etc. For example, the voltage Vread and the voltage SL may be predetermined values to enable a fixed voltage between the drain 210 and the source 212, for example, intermittently or continuously, etc. In other embodiments, the voltage Vread and the voltage SL may be set to enable a constant current from the drain 210 to the source 212, for example intermittently or continuously, etc.

[0031] The voltages applied to the gate 208 of the FeFET 202 by the program-signal circuit 206 can cause the ferroelectric material in the FeFET 202 to form an electric polarization. The ferroelectric polarization can remain (or substantially remains) long after the voltage applied to the gate 208 of the FeFET 202 is removed if the voltage was of sufficient magnitude and duration to change the state of the ferroelectric material. This is a result of a stable electric polarization in the ferroelectric material. The ferroelectric material is an insulator in which the electric polarization induced by an applied electric field from a voltage applied to the gate 208 remains after removal of that voltage.

[0032] Positive voltage biases (or pulses) from the program-signal circuit 206 applied to the gate 208 of the FeFET 202 results in a reduction in the threshold voltage of the FeFET 202 and brings the channel of the FeFET 202 into accumulation mode. And negative voltage bias (or pulses) from the program-signal circuit 206 applied to the gate 208 of the FeFET 202 results in an increase in the threshold voltage of the FeFET 202 and brings the channel of the FeFET 202 into depletion

mode. The first state may correspond to a 0-value and the second state may correspond to a 1-value, or visa-versa.

[0033] Referring to Figs. 2-3: Fig. 3 illustrates operating characteristics of the FeFET 202 of Fig. 2 in a graph 300 when used to store binary states in accordance with an embodiment of the present disclosure. The graph 300 shows an axis 302 that shows a current, I_{ds} , that is the current from the drain 210, through the FeFET 202, and through the source 212 to ground. The current I_{ds} passes through a channel of the FeFET 202 where the channel has characteristics based upon the polarization of the ferroelectric material. The graph 300 also includes an axis 304 that shows the voltage at the gate 208 of Fig. 2. The V_g values applied to the gate 208 may be within a range of voltages to determine the state of the FeFET without significantly disturbing the ferroelectric material's polarization.

[0034] Fig. 3 illustrates the relationship between the I_{ds} and V_g based upon the state of the FeFET 202 in accordance with an embodiment of the present disclosure. A first curve 306 shows the FeFET 202 in a first state because it has a first threshold voltage 308. A second curve 308 shows the FeFET 202 in a second state because it has a second threshold voltage 312. The states of the FeFET 202 may be programmed by the program-signal circuit 206 to change the electric polarization of the ferroelectric material in the FeFET 202. These states may be detected by the sense circuit 302. In some embodiments, no V_g voltage needs to be applied to the FeFET 202 to determine the state; however, in other embodiments, a sufficient voltage needs to be applied to the gate 208 to determine the state of the FeFET, but without programming the FeFET 202.

[0035] Referring to Figs. 2 and 4: Fig. 4 illustrates operating characterizes of the FeFET 202 of Fig. 2 in a graph 400 when the FeFET 202 is used to store a continuous value, such as a weight of a neuromorphic cell, in accordance with an embodiment of the present disclosure.

[0036] The graph 400 shows an axis 402 for a current I_{ds} . I_{ds} is the current from the drain 210 through the FeFET 202 and through the source 212 to ground. The current I_{ds} passes through a channel of the FeFET 202 where the channel has characteristics based upon the polarization of the ferroelectric material. The graph 400 also includes an axis 404 that shows the voltage at the gate 208 of Fig. 2. The V_g values applied to the gate 208 may be within a range of voltages to determine the state of the FeFET without significantly disturbing the ferroelectric material's polarization.

[0037] Fig. 4 illustrates the relationship between the I_{ds} and V_g based upon the polarization of the FeFET 202 in accordance with an embodiment of the present disclosure. As the polarization changes, the characteristic curve shifts as indicated by arrow 408. These shifting curves cause the

threshold voltages 406 to shift as well. These values may be mapped to a weight of an artificial neural network. For example, an arithmetic logic unit may read these values for computation within a processing element of Fig. 1. In some embodiments, the memory is used as in-memory-computing, and along with other analog circuit, can perform the calculations of an artificial neural net in accordance with the mapped value corresponding to a weight of a neural network cell, e.g., neuron. During a neural network training phase, the AI accelerator 100 may use the program-signal circuit 206 to change the electric polarization of the ferroelectric material in the FeFET 202 to correspond to a neuron weight. These threshold voltages 406 may be detected by the sense circuit 204. In some embodiments, no V_g voltage needs to be applied to the FeFET 202 to determine its state; however, in other embodiments, a voltage is applied to the gate 208.

[0038] Fig. 5 shows a memory array 500 utilizing FeFET transistors 514 in accordance with an embodiment of the present disclosure. The FeFET transistors 514 each have a polarization state. An interface circuit (not shown) can select one of the word lines 502, 504, or 506, to activate a column of FeFET transistors 514. These activated FeFETs 514 coupled to the activated word line, e.g., 504, causes each of the bit lines 508, 510, 512 to output the state (or value) that corresponds to the ferroelectric's electric polarization in each respective one of the FeFETs 514. One of ordinary skill in the art will appreciate that the array of FeFETs 514 can be increased to have a target memory size. Additionally, one of ordinary skill in the relevant art will appreciate that programming circuitry may be added to the memory array 500.

[0039] The FeFET transistors 512 may be powered by a voltage from the bit lines 502, 504, 506 that is relative to the voltages SL. The SL references may be a ground, may be a fixed voltage, may be a programmable voltage, may be a variable voltage, may be coupled to a ground or a voltage source via another transistor (not shown), etc.

[0040] Figs. 6-7 show FeFETs 600, 700 configured for scaling on a back-end-of-line ("BEOL") portion of an integrated circuit semiconductor in accordance with an embodiment of the present disclosure. Fig. 6 shows a FeFET 600 which may be a BEOL FeFET which is not constructed in a silicon substrate, but instead sits at the BEOL between different metal layers. Some of the layers shown in the FeFETs 600, 700 may be formed, in some specific embodiments, using atomic layer deposition ("ALD") where the layer thicknesses can be as thin as 2nm to 10nm. However, other deposition techniques, different thicknesses, or technologies may be used as well.

[0041] The FeFET 600 includes source-or-drain terminals 602. Because of symmetry, the terminals 602 may be used to introduce I_{ds} in either direction of current flow and hence may operate

as a source or a drain. The terminals 602 may be formed with metals, such as Pd, Mo, Al/Ti, W, Cu, TiN, Pt, etc.

[0042] The FeFET 600 includes a channel structure 604 having a first portion 606, a second portion 608, and a third portion 610. The first portion 606 is disposed adjacent to the terminal 602, the second portion 608 is disposed on top of an insulating layer, which may be an insulating layer laid down on a BEOL of the integrated circuit. The third portion 610 is disposed adjacent to the terminal 602. The channel material may be n-type such as: ITO, IGZO, IZO, AZO, a-Si, ZnO, a-Ge, polysilicon or poly-Si, poly-Ge, or poly-III-V like InAs, etc. In some embodiments, the channel material may be p-type such as: a-Si, ZnO, a-Ge, polysilicon, poly germanium, poly-III-V like InAs, CuO, SnO, etc. The channel structure 604 may, in some specific embodiments, have a channel length of 5nm to 100nm. However, other lengths may be used. Also, in some specific embodiments, the channel structure's 604 width may be any width as known to one of ordinary skill in the relevant art.

[0043] The FeFET 600 also includes a ferroelectric structure 612 that includes a first portion 614, a second portion 616, and a third portion 618. The first portion 614 is disposed adjacent to the first portion 606 of the channel structure 604. The second portion 616 of the ferroelectric structure 616 is disposed adjacent to the second portion 608 of the channel structure 604. The third portion 618 of the ferroelectric structure 618 is disposed adjacent to the third portion 610 of the channel structure 604. The ferroelectric material may be made from one or more of lead zirconate titanate (PZT), hafnium zirconium oxide (HZO), barium titanate (BaTiO₃), lead titanate (PbTiO₃), and doped hafnium dioxide (HfO₂). The doped HfO₂ may include one or more of silicon doped HfO₂, yttrium-doped HfO₂, and aluminum-doped HfO₂.

[0044] The FeFET 600 also includes a gate structure 620, which corresponds to the gate 208 shown in Fig. 2. The gate structure 620 may be made of any suitable material, such as a metal, an alloy, W, Cu, Al, TiN, some combination thereof, etc. The gate structure 620 may have a positive or negative voltage applied to it, e.g., a positive or negative voltage relative to ground or relative to terminal 602. The voltage applied to the gate structure 620 may be of a voltage and duration to change, reverse, or modify the electric polarization of the ferroelectric material in the ferroelectric structure 612.

[0045] The FeFET 700 of Fig. 7 is similar to the FeFET 600 of Fig. 6, but with a smaller gate length L₂. That is, the FeFET 600 has a gate length L₁, which is larger than the FeFET's 700 gate length L₂. These different gate lengths (L₁ vs. L₂) are to illustrate the scaling process that may

occur during a design of an integrated circuit. Please note that as the device footprint decreases (e.g., from L1 to L2), the density achievable by including additional FeFETs increases. Additionally, the FeFET 700 can be further scaled without reduction of the polarization magnitude because the FE layer area undergoing polarization will mainly be between the gate structure 620 and the source-or-drain walls 601 or 601 (in the width of the FeFET). Additionally, the structure of the FeFET 700 allows for increased height of the device to increase the FE area, which increases the grain density, which in turn results in a higher polarization magnitude within the ferroelectric material without increasing the device's footprint. That is, the footprint of the FeFET 700 is partially separated from the polarizable ferroelectric area because some of the ferroelectric structure 612 is placed in a separate plane. This compact device arrangement of the FeFETs 600, 700, is such that the gate 620 overlap of source or drain (e.g., two terminals of 602) sits in another dimension and orthogonal to the direction of the channel length, allowing for an increase in ferroelectric layer area 612 without having to increase the FeFETs 600, 700 footprint and overall area. Furthermore, the FeFETs' 600, 700 design allows for suitable control of the ferroelectric, channel and source-or-drain layers' interfaces, dimensions and interactions as will be readily apparent to one of ordinary skill in the relevant art.

[0046] Fig. 8 shows an array 800 of bit cells 802a-802c formed by a plurality of FeFETs of Figs. 5-7 in accordance with an embodiment of the present disclosure. These FeFETs can be arranged in a linear fashion as shown in the array 800 such that between each pair of terminals 602 sits a channel structure 610, a ferroelectric structure 612, and a gate structure 620 which forms a bit, e.g., bits 1-3 as shown in Fig. 8. These bits may extend an arbitrary length beyond the three bits shown in Fig. 8.

[0047] Referring now to Figs. 9A-9E and 10, which together illustrates a manufacturing process to manufacture the array of bit cells of Fig. 8 in accordance with an embodiment of the present disclosure. One such method of manufacturing is described in Fig. 10, which shows a flow chart diagram of a method 1000 of manufacture of the array of bit cells as is illustrated in Figs. 9A-9E.

[0048] The method 1000 includes acts 1002-1012. Act 1002 forms an insulating layer, e.g., the insulating layer 900 of Figs. 9A-9E. The insulating layer 900 may be formed as part of the formation of the BEOL layer. Act 1004 forms a plurality of parallel electrodes 902 (e.g., source and drain electrodes) as is shown in Fig. 9A. These electrodes 902 may be formed utilizing deposition, patterning, and/or a combination of deposition and patterning. Act 1006 forms a

plurality of channel structures 904 by depositing a channel layer and performing a planarization which results in the structure shown in Fig. 9B. The planarization may be done by chemical-mechanical polishing, chemical etching, mechanical polishing (e.g., abrasive polishing), or some combination thereof. Act 1008 forms a plurality of ferroelectric structures 906 by depositing a ferroelectric layer and performing a planarization which results in the configuration shown in Fig. 9C. Act 1010 forms a plurality of gate structures 908 by depositing a gate layer and performing a planarization as is shown in Fig. 9D. The plurality of FeFET transistors is now complete as shown in Fig. 9D; however, metal needs to be connected to the different terminals of the transistors. Act 1012 forms an insulating 912 and routing layer 910 (e.g., metal connectors) for routing the electric connections to the gates, sources, and drain electrodes.

[0049] Referring now to Figs. 12 and 11A-11F: Fig. 12 shows a flow chart diagram illustrating a method 1200 to manufacture the array of bit cells of Fig. 8 using stages shown in Figs. 11A-11F in accordance with an embodiment of the present disclosure.

[0050] The method 1200 includes Acts 1202-1214. Act 1202 forms an insulating layer 1100 as shown in Figs. 11A-11F. The insulating layer 1110 may be formed as part of the formation of the BEOL layer. Act 1204 forms a plurality of parallel electrodes 1102 (e.g., source and drain electrodes) resulting in the structure shown in Fig. 11A. Act 1206 forms a plurality of channel structures by depositing a channel layer 1104 as shown in Fig. 11B. Act 1208 forms a plurality of ferroelectric structures by depositing a ferroelectric layer 1106 as shown in Fig. 11C. Act 1210 forms a plurality of gate structures by depositing a gate layer 1108 as shown in Fig. 11D. Act 1212 planarizes the channel structure, the ferroelectric structure, and the gate structure as shown in Fig. 11E. Act 1214 forms an insulating and routing layer 1110 for routing the electric connections to the gates, sources, and drain electrodes as shown in Fig. 11F.

[0051] Various alternatives and modifications can be devised by those skilled in the art without departing from the disclosure. Accordingly, the present disclosure is intended to embrace all such alternatives, modifications and variances. Additionally, while several embodiments of the present disclosure have been shown in the drawings and/or discussed herein, it is not intended that the disclosure be limited thereto, as it is intended that the disclosure be as broad in scope as the art will allow and that the specification be read likewise. Therefore, the above description should not be construed as limiting, but merely as exemplifications of particular embodiments. And, those skilled in the art will envision other modifications within the scope and spirit of the claims appended hereto. Other elements, steps, methods and techniques that are insubstantially different from those

described above and/or in the appended claims are also intended to be within the scope of the disclosure.

[0052] The embodiments shown in the drawings are presented only to demonstrate certain examples of the disclosure. And, the drawings described are only illustrative and are non-limiting. In the drawings, for illustrative purposes, the size of some of the elements may be exaggerated and not drawn to a particular scale. Additionally, elements shown within the drawings that have the same numbers may be identical elements or may be similar elements, depending on the context.

[0053] Where the term "comprising" is used in the present description and claims, it does not exclude other elements or steps. Where an indefinite or definite article is used when referring to a singular noun, e.g., "a," "an," or "the," this includes a plural of that noun unless something otherwise is specifically stated. Hence, the term "comprising" should not be interpreted as being restricted to the items listed thereafter; it does not exclude other elements or steps, and so the scope of the expression "a device comprising items A and B" should not be limited to devices consisting only of components A and B. This expression signifies that, with respect to the present disclosure, the only relevant components of the device are A and B.

[0054] Furthermore, the terms "first," "second," "third," and the like, whether used in the description or in the claims, are provided for distinguishing between similar elements and not necessarily for describing a sequential or chronological order. It is to be understood that the terms so used are interchangeable under appropriate circumstances (unless clearly disclosed otherwise) and that the embodiments of the disclosure described herein are capable of operation in other sequences and/or arrangements than are described or illustrated herein.

What is claimed is:

1. An integrated circuit device, comprising:
 - a first layer having a semiconductor substrate; and
 - a second layer disposed parallel to the first layer, the second layer having an insulating layer and a transistor disposed on the insulating layer, the transistor comprising:
 - a source electrode disposed on the insulating layer along a first length parallel to the insulating layer;
 - a drain electrode disposed on the insulating layer parallel to the source electrode, the drain electrode disposed a predetermined distance from the source electrode;
 - a channel structure having a first portion, a second portion, and a third portion, the first portion is disposed parallel to the source electrode along the first length, the second portion disposed parallel to the insulating layer and adjacent to the first portion, the third portion disposed parallel to the drain electrode and adjacent to the second portion;
 - a ferroelectric structure having a first portion, a second portion, and a third portion, the first portion of the ferroelectric structure disposed parallel to the first portion of the channel structure, the second portion of the ferroelectric structure disposed parallel to the second portion of the channel structure, the third portion of the ferroelectric structure disposed parallel to the third portion of the channel structure, wherein the ferroelectric structure is configured to have at least one polarization; and
 - a gate structure disposed within a space defined by the first, second, and third portions of the ferroelectric structure.
2. The device according to claim 1, wherein the first layer is a front-end-of-line layer.

3. The device according to claim 1, wherein the second layer is a back-end-of-line layer.
4. The device according to claim 1, wherein the second layer includes a three-dimensional stack of memory cells including the transistor.
5. The device according to claim 1, wherein the transistor is configured to store a Neuromorphic value.
6. The device according to claim 1, wherein the ferroelectric structure is configured to have a selectable polarization, wherein the polarization corresponds to a stored value.
7. The device according to claim 6, wherein the stored value is a discrete value.
8. The device according to claim 6, wherein the stored value is a continuous value.
9. The device according to claim 1, further comprising a second insulating layer disposed on the first and third portions of the channel structure, on the first and second portions of the ferroelectric structure, and on the gate structure.
10. The device according to claim 1, the source electrode having height defined by a second length extending orthogonally from the insulating layer, the source electrode having a thickness defined by a third length orthogonal to the first length and the second length.
11. A computer system comprising:

a central processing unit;
a memory in operative communication with the central processing unit; and
an integrated circuit according to claim 1, wherein the integrated circuit is configured as an artificial intelligence accelerator.

12. A method of making an integrated circuit, the method comprising:

forming an insulating layer;
forming a source electrode disposed parallel to the insulating layer along a first length parallel to the insulating layer;
forming a drain electrode disposed parallel to the insulating layer and parallel to the source electrode, the drain electrode disposed a predetermined distance from the source electrode;
forming a channel structure having a first portion, a second portion, and a third portion, the first portion is disposed parallel to the source electrode along the first length, the second portion disposed along the insulating layer adjacent to the first portion, the third portion disposed parallel to the drain electrode and adjacent to the second portion;
forming a ferroelectric structure having a first portion, a second portion, and a third portion, the first portion of the ferroelectric structure disposed parallel to the first portion the channel structure, the second portion of the ferroelectric structure disposed parallel to the second portion the channel structure, the third portion of the ferroelectric structure disposed parallel to the third portion the channel structure, wherein the ferroelectric structure is configured to have at least one polarization; and
forming a gate structure disposed within a space defined by the first, second, and third portions of the ferroelectric structure.

13. The method according to claim 12, wherein the act of forming the channel structure includes depositing the channel structure using atomic layer deposition.
14. The method according to claim 12, wherein the act of forming the ferroelectric structure includes depositing the ferroelectric structure using atomic layer deposition.
15. The method according to claim 12, wherein the act of forming the gate structure comprises:
depositing the gate structure including an excess gate structure using atomic layer deposition; and
removing the excess gate structure using chemical-mechanical planarization.
16. The method according to claim 12, further comprising:
forming a second insulating layer; and
forming at least one contact with at least one of: the source electrode, the drain electrode, and the gate structure.
17. An integrated circuit device, the device comprising:
an insulating layer;
a plurality of parallel electrodes each extending along a first direction parallel to the insulating layer, wherein the plurality of parallel electrodes is arranged in spaced relation to each other to thereby have a predetermined space interposed between each adjacent pair of the plurality of parallel electrodes defining a plurality of spaces between each adjacent pair of the plurality of parallel electrodes;

a plurality of channel structures each disposed within a space of the plurality of spaces, each channel structure in cooperation with both of the adjacent pair of the plurality of parallel electrodes and the insulating layer;

a plurality of ferroelectric structures each disposed adjacent to a respective one of the plurality of channel structures, wherein each of the ferroelectric structures is configured to include a respective channel; and

a plurality of gate structures each disposed within the respective channel of the plurality of ferroelectric structures.

18. The device according to claim 17, wherein at least one of the plurality of parallel electrodes is a drain-or-source electrode.

19. A computer system, comprising:

a central processing unit;

a memory in operative communication with the central processing unit; and

an integrated circuit according to claim 17, wherein the integrated circuit is configured as an artificial intelligence accelerator.

20. A method of making an integrated circuit, the method comprising:

forming an insulating layer;

forming a plurality of parallel electrodes each extending along a first direction parallel to the insulating layer, wherein the plurality of parallel electrodes are arranged in spaced relation to each other to thereby have a predetermined space interposed between each adjacent pair of the plurality

of parallel electrodes defining a plurality of spaces between each adjacent pair of the plurality of parallel electrodes;

forming a plurality of channel structures each disposed within a space of the plurality of spaces, each channel structure in cooperation with both of the adjacent pair of the plurality of parallel electrodes and the insulating layer;

forming a plurality of ferroelectric structures each disposed adjacent to a respective one of the plurality of channel structures, wherein each of the ferroelectric structures is configured to include a respective channel; and

forming a plurality of gate structures each disposed within the respective channel of the plurality of ferroelectric structures.

21. The method according to claim 20, wherein the act of forming the plurality of parallel electrodes includes depositing an electrode using atomic layer deposition.

22. The method according to claim 20, wherein the act of forming the plurality of channel structures includes depositing a channel structure using atomic layer deposition.

23. The method according to claim 20, wherein the act of forming the plurality of ferroelectric structures includes depositing a ferroelectric structure using atomic layer deposition.

24. The method according to claim 20, wherein the act of forming the plurality of gate structures comprises:

depositing a gate structure including an excess gate structure using atomic layer deposition;
and

removing the excess gate structure using chemical-mechanical planarization.

25. The method according to claim 20, further comprising:
- forming a second insulating layer; and
 - forming at least one contact with at least one of a gate structure of the plurality of gate structures and an electrode of the plurality of parallel electrodes.