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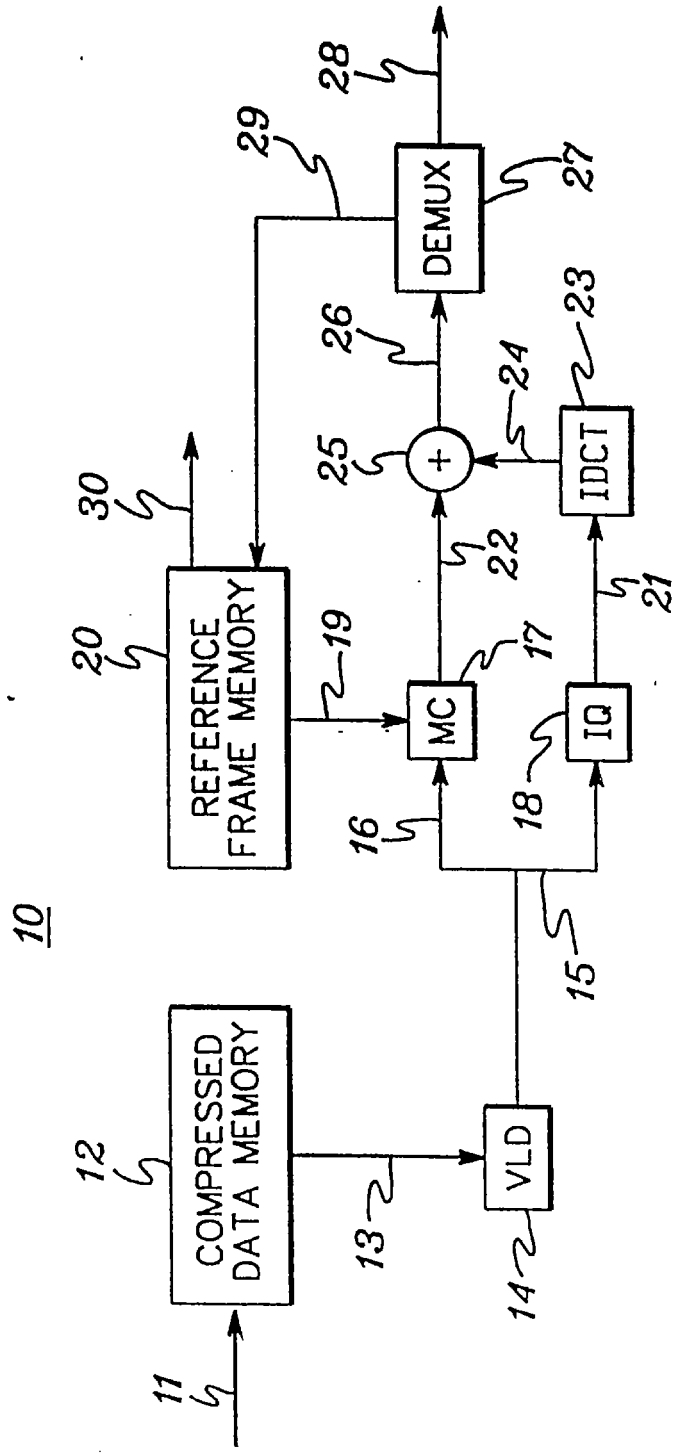


fig. 1

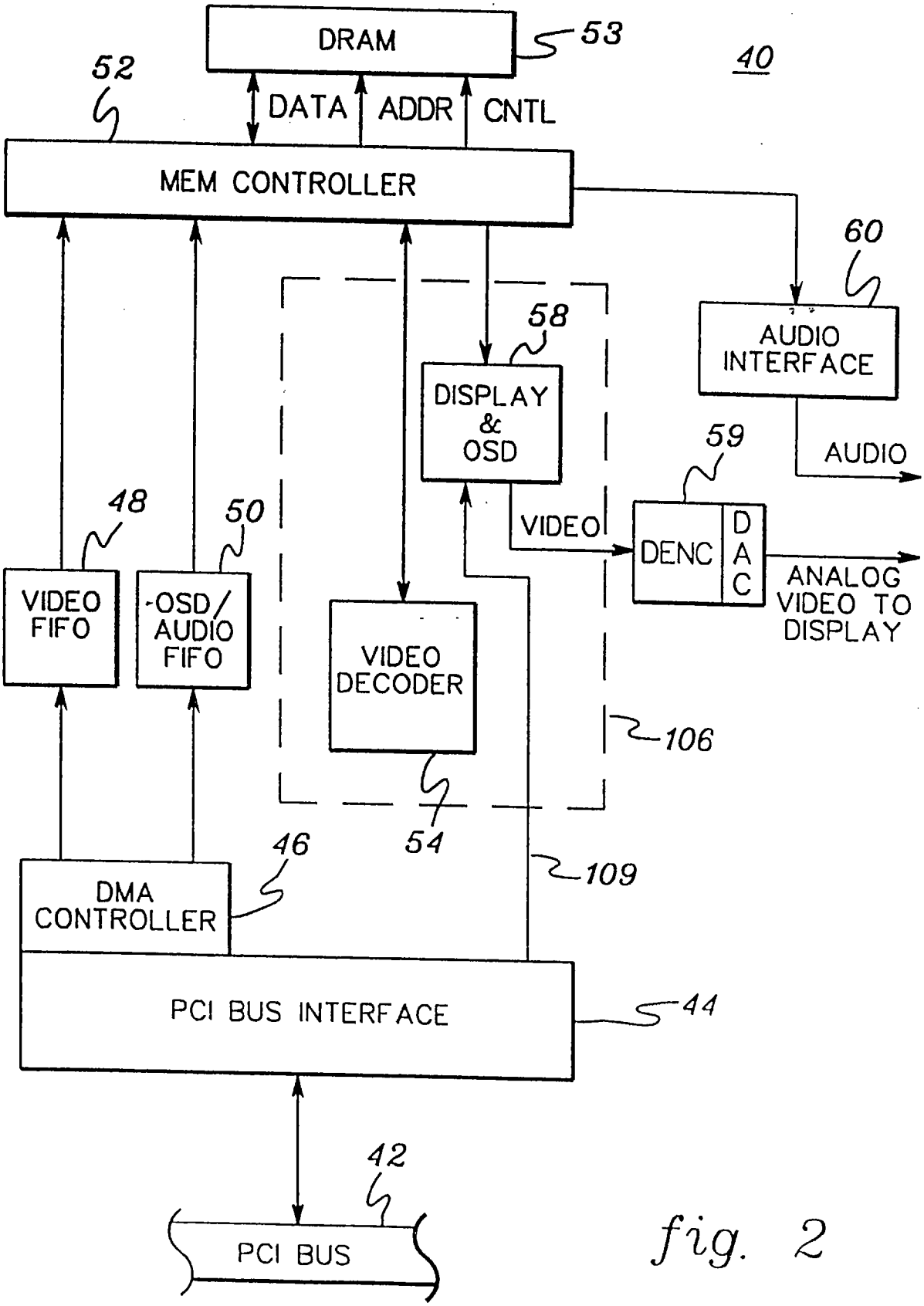

DRAM
53
40
52
DATA
ADDR
CNTL
MEM CONTROLLER
60
58
AUDIO INTERFACE
DISPLAY & OSD
59
AUDIO
48
50
VIDEO
DENC
D A C
VIDEO FIFO
OSD/ AUDIO FIFO
ANALOG VIDEO TO DISPLAY
VIDEO DECODER
106
54
46
109
DMA CONTROLLER
PCI BUS INTERFACE
44
42
PCI BUS

fig. 2

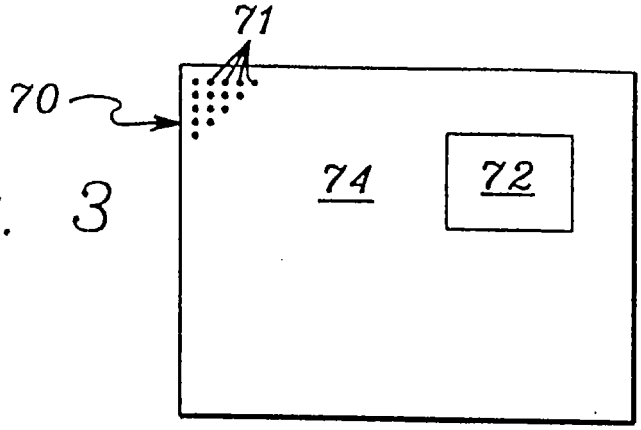


fig. 3

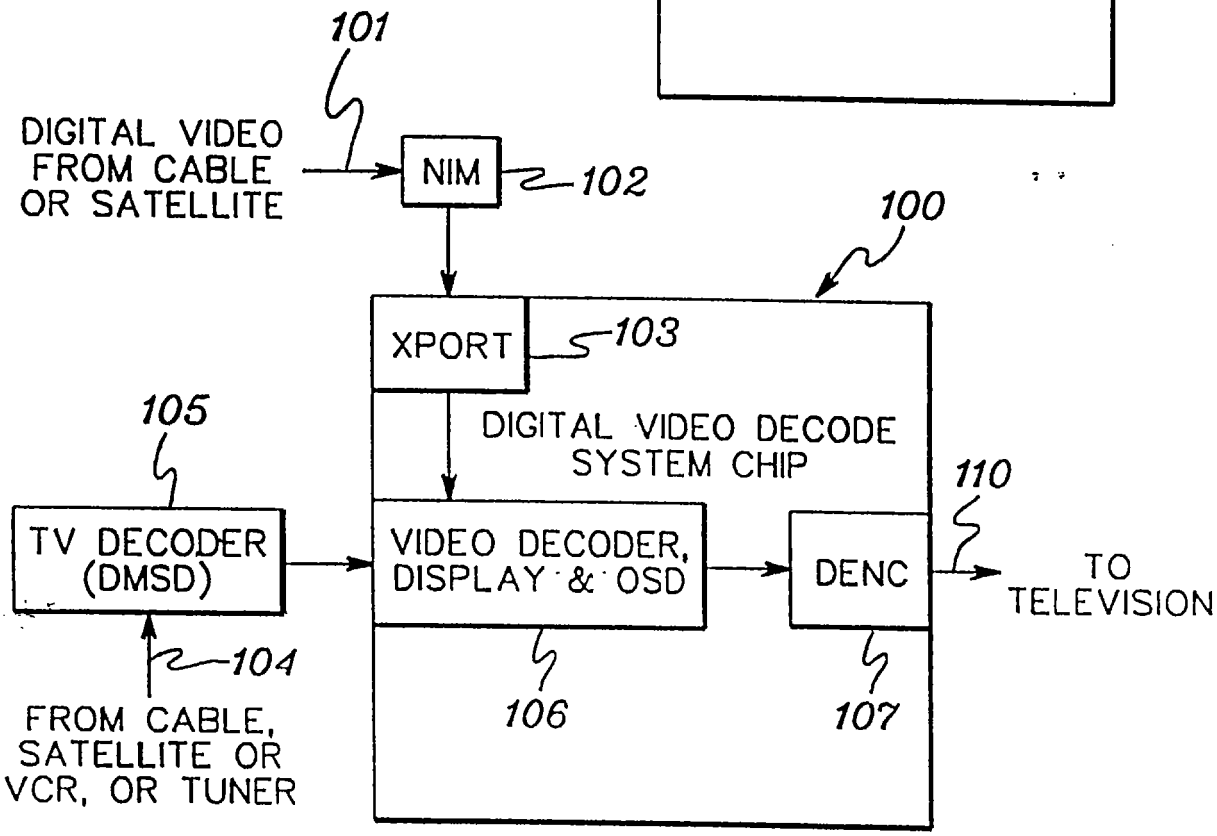


fig. 4

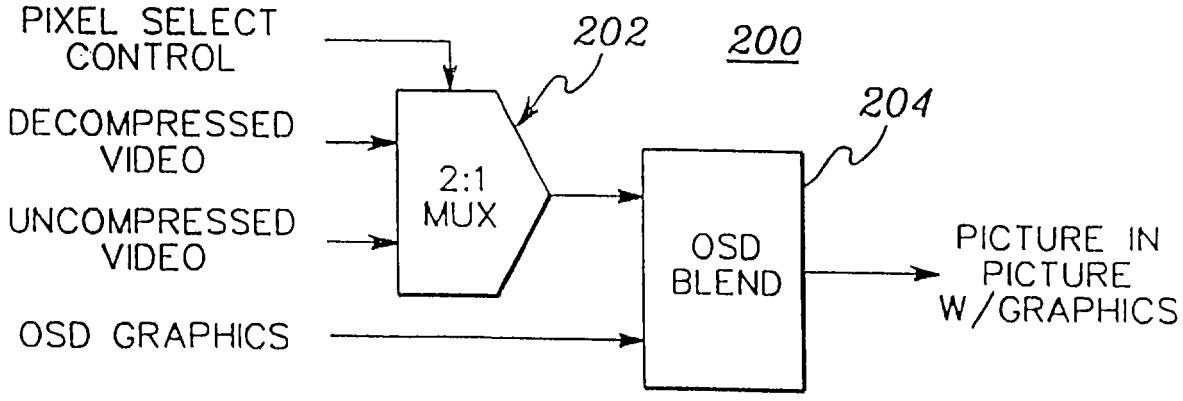


fig. 5

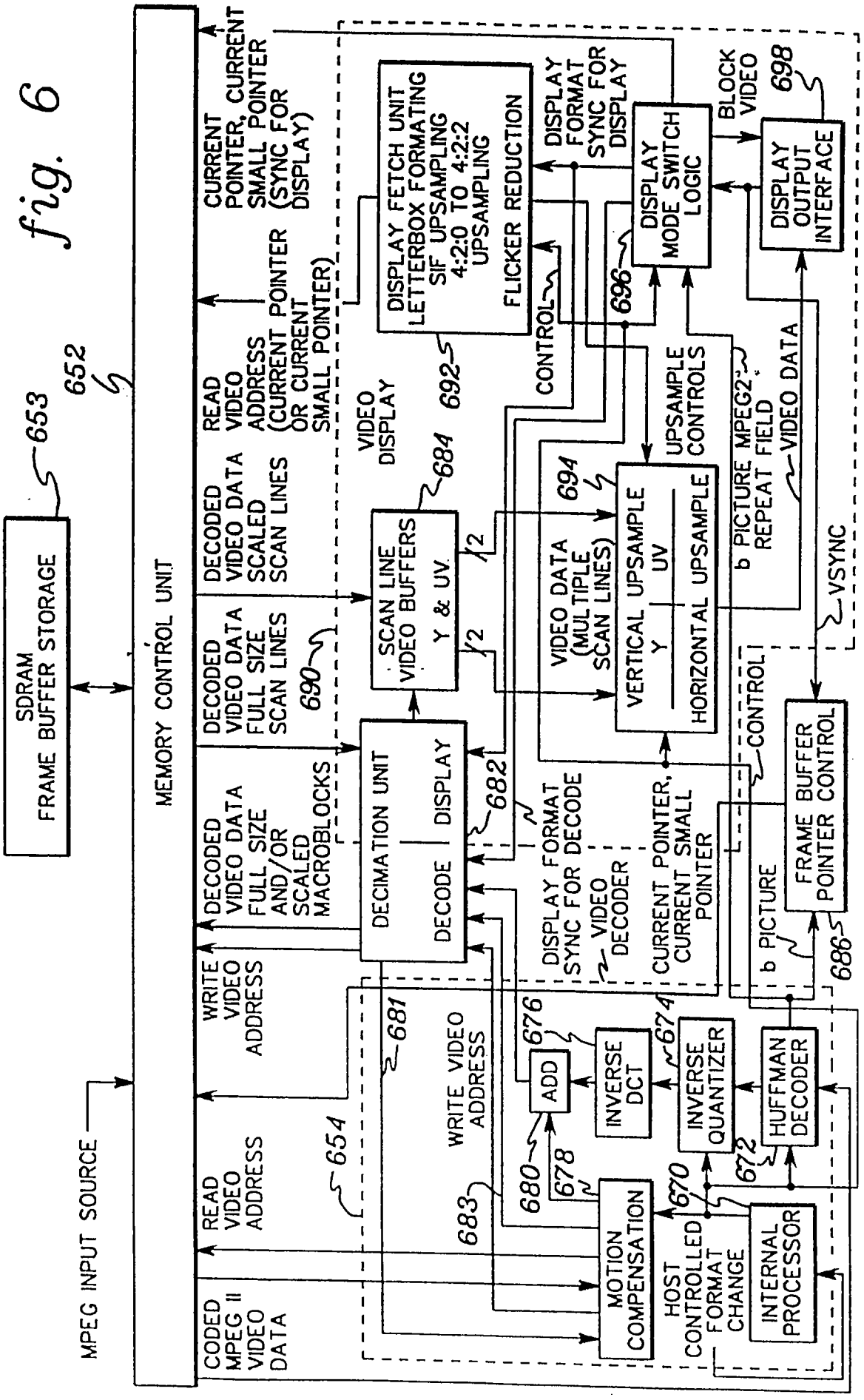

MPEG INPUT SOURCE
SDRAM FRAME BUFFER STORAGE
653
652
MEMORY CONTROL UNIT
CODED MPEG II VIDEO DATA
READ VIDEO ADDRESS
654
WRITE VIDEO ADDRESS
681
DECODED VIDEO DATA FULL SIZE AND/OR SCALED MACROBLOCKS
DECIMATION UNIT
DECODE
DISPLAY
682
DECODED VIDEO DATA FULL SIZE SCAN LINES
690
DECODED VIDEO DATA SCALED SCAN LINES
SCAN LINE VIDEO BUFFERS
Y & UV
1/2
1/2
684
VIDEO DISPLAY
READ VIDEO ADDRESS (CURRENT POINTER OR CURRENT SMALL POINTER)
CURRENT POINTER, CURRENT SMALL POINTER (SYNC FOR DISPLAY)
DISPLAY FETCH UNIT LETTERBOX FORMATING SIF UPSAMPLING 4:2:0 TO 4:2:2 UPSAMPLING
692
FLICKER REDUCTION
DISPLAY FORMAT SYNC FOR DISPLAY
CONTROL
696
DISPLAY MODE SWITCH LOGIC
BLOCK VIDEO
698
DISPLAY OUTPUT INTERFACE
VIDEO DATA (MULTIPLE SCAN LINES)
694
VERTICAL UPSAMPLE
Y
UV
HORIZONTAL UPSAMPLE
UPSAMPLE CONTROLS
b PICTURE MPEG2 REPEAT FIELD
VIDEO DATA
VSYNC
CONTROL
DISPLAY FORMAT SYNC FOR DECODE
VIDEO DECODER
CURRENT POINTER, CURRENT SMALL POINTER
b PICTURE
FRAME BUFFER POINTER CONTROL
686
WRITE VIDEO ADDRESS
683
676
ADD
680
678
INVERSE DCT
674
INVERSE QUANTIZER
672
HUFFMAN DECODER
670
MOTION COMPENSATION
HOST CONTROLLED FORMAT CHANGE
INTERNAL PROCESSOR

fig. 6

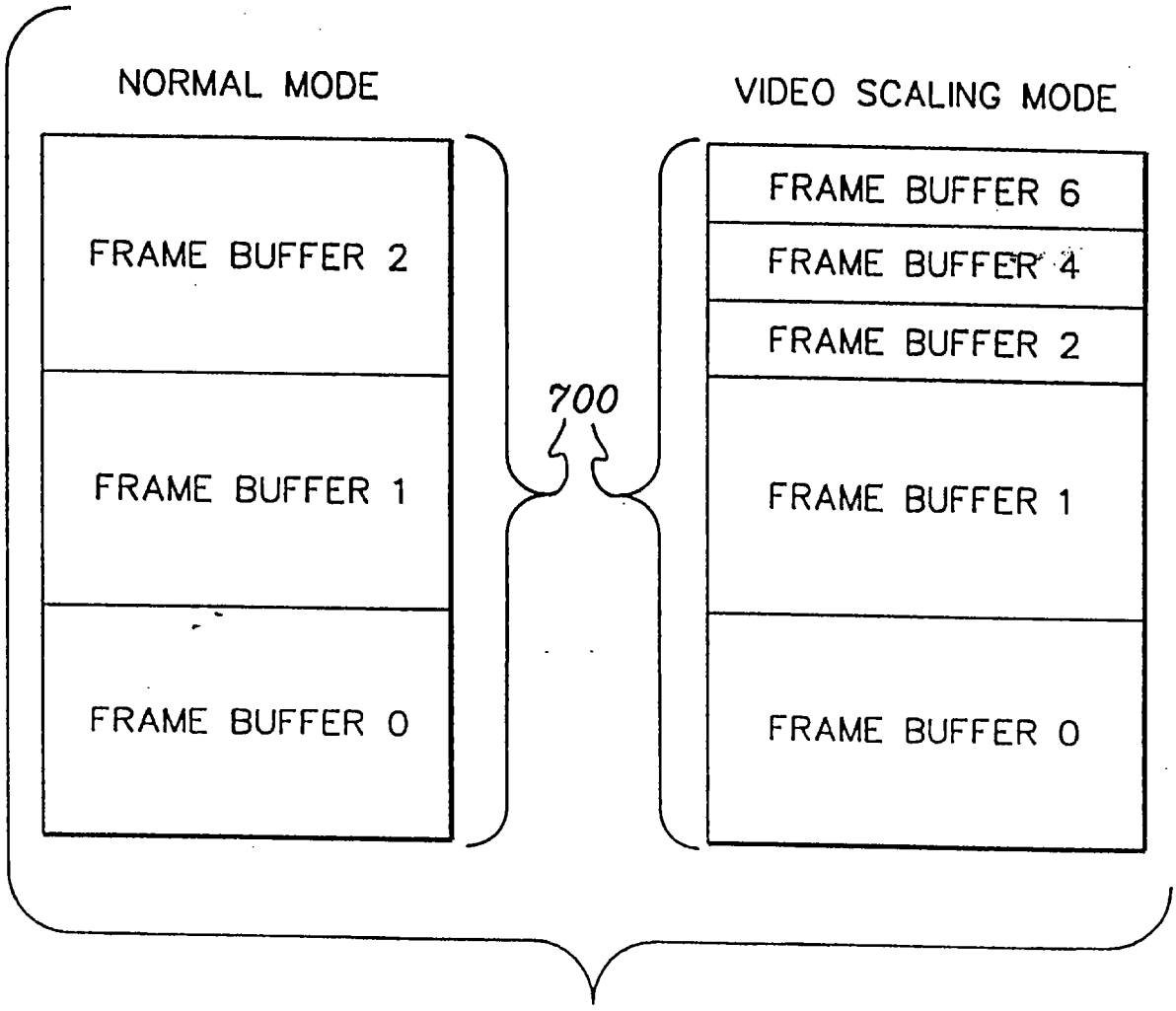

NORMAL MODE
FRAME BUFFER 2
FRAME BUFFER 1
FRAME BUFFER 0
700
VIDEO SCALING MODE
FRAME BUFFER 6
FRAME BUFFER 4
FRAME BUFFER 2
FRAME BUFFER 1
FRAME BUFFER 0

fig. 6A

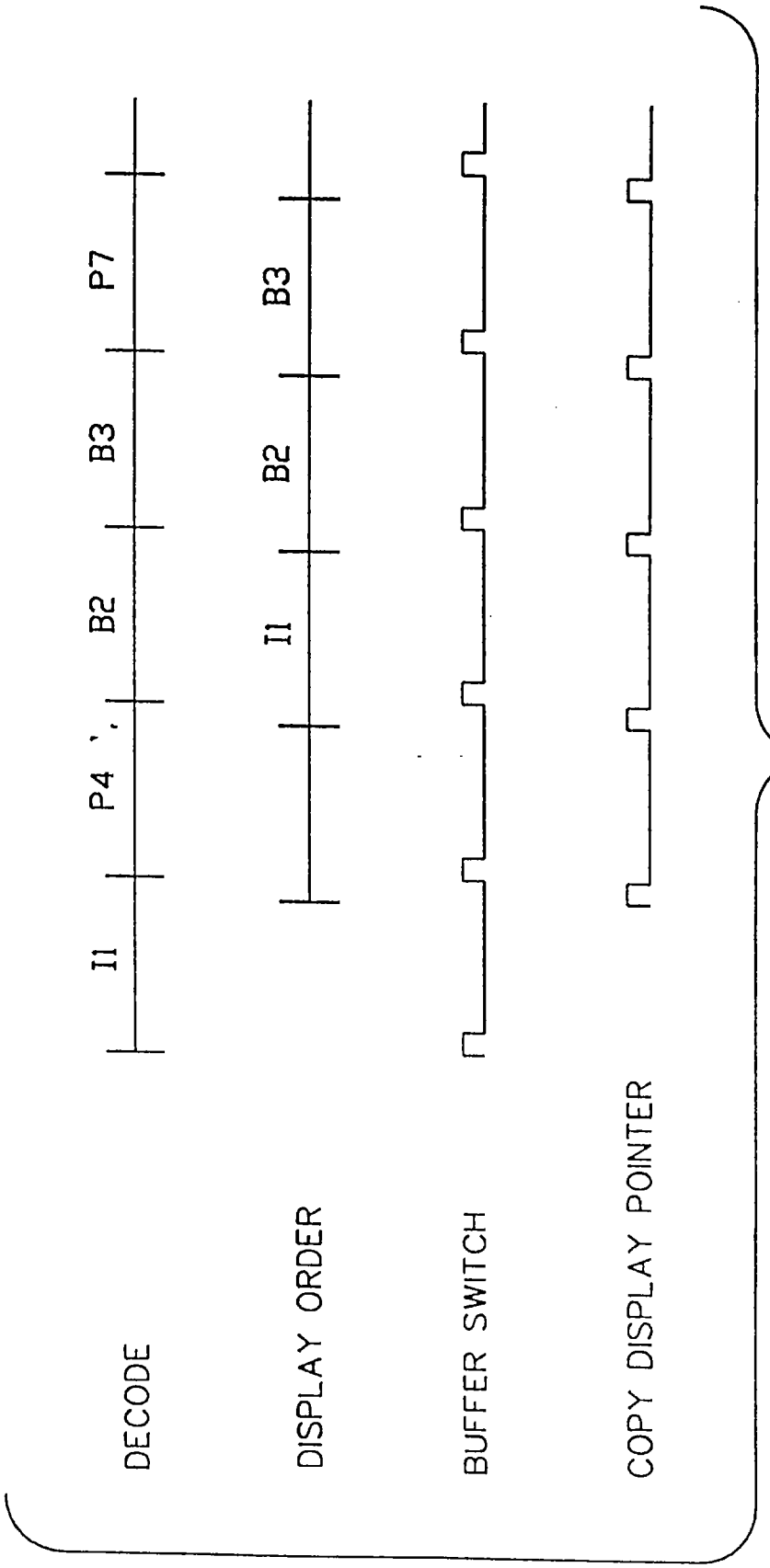

DECODE
I1
P4
B2
B3
P7
DISPLAY ORDER
I1
B2
B3
BUFFER SWITCH
COPY DISPLAY POINTER

fig. 7A

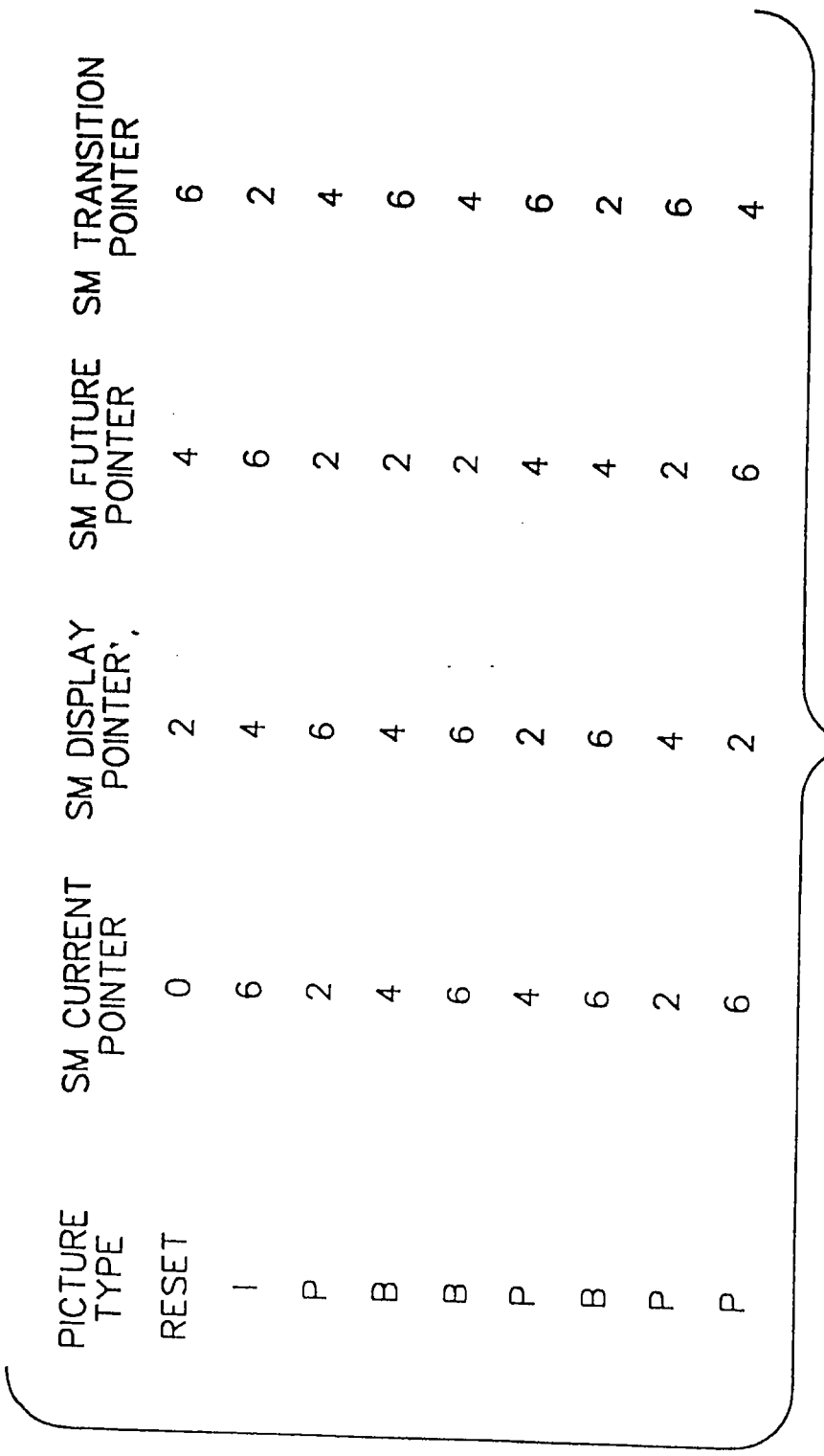

PICTURE TYPE
SM CURRENT POINTER
SM DISPLAY POINTER'
SM FUTURE POINTER
SM TRANSITION POINTER
RESET
0
2
4
6
I
6
4
6
2
P
2
6
2
4
B
4
4
2
6
B
6
6
2
4
P
4
2
4
6
B
6
6
4
2
P
2
4
2
6
P
6
2
6
4

fig. 7B

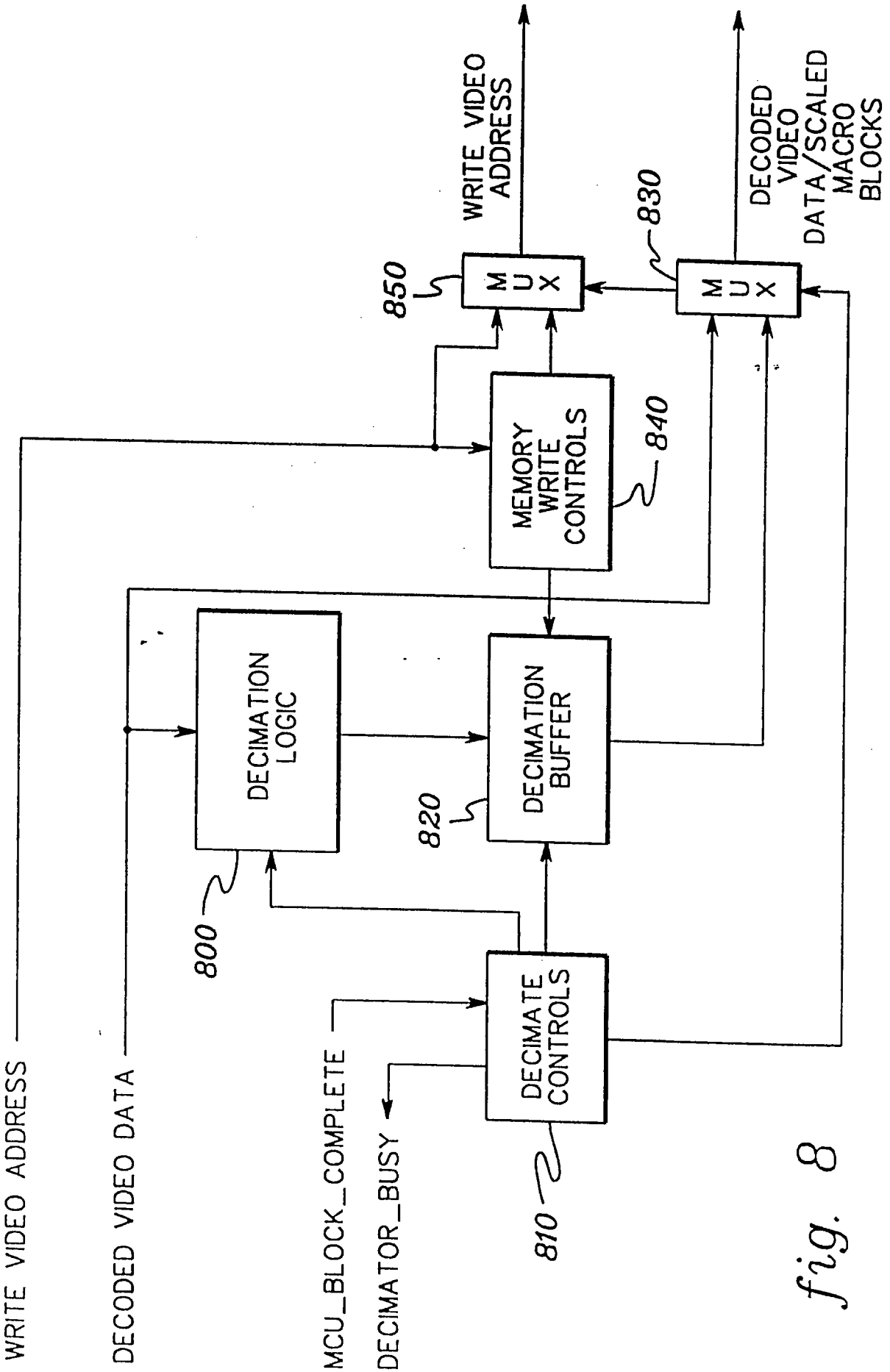

WRITE VIDEO ADDRESS
DECODED VIDEO DATA
MCU_BLOCK_COMPLETE
DECIMATOR_BUSY
DECIMATE CONTROLS
DECIMATION LOGIC
DECIMATION BUFFER
MEMORY WRITE CONTROLS
MUX
MUX
WRITE VIDEO ADDRESS
DECODED VIDEO DATA/SCALED MACRO BLOCKS
800
810
820
830
840
850

fig. 8

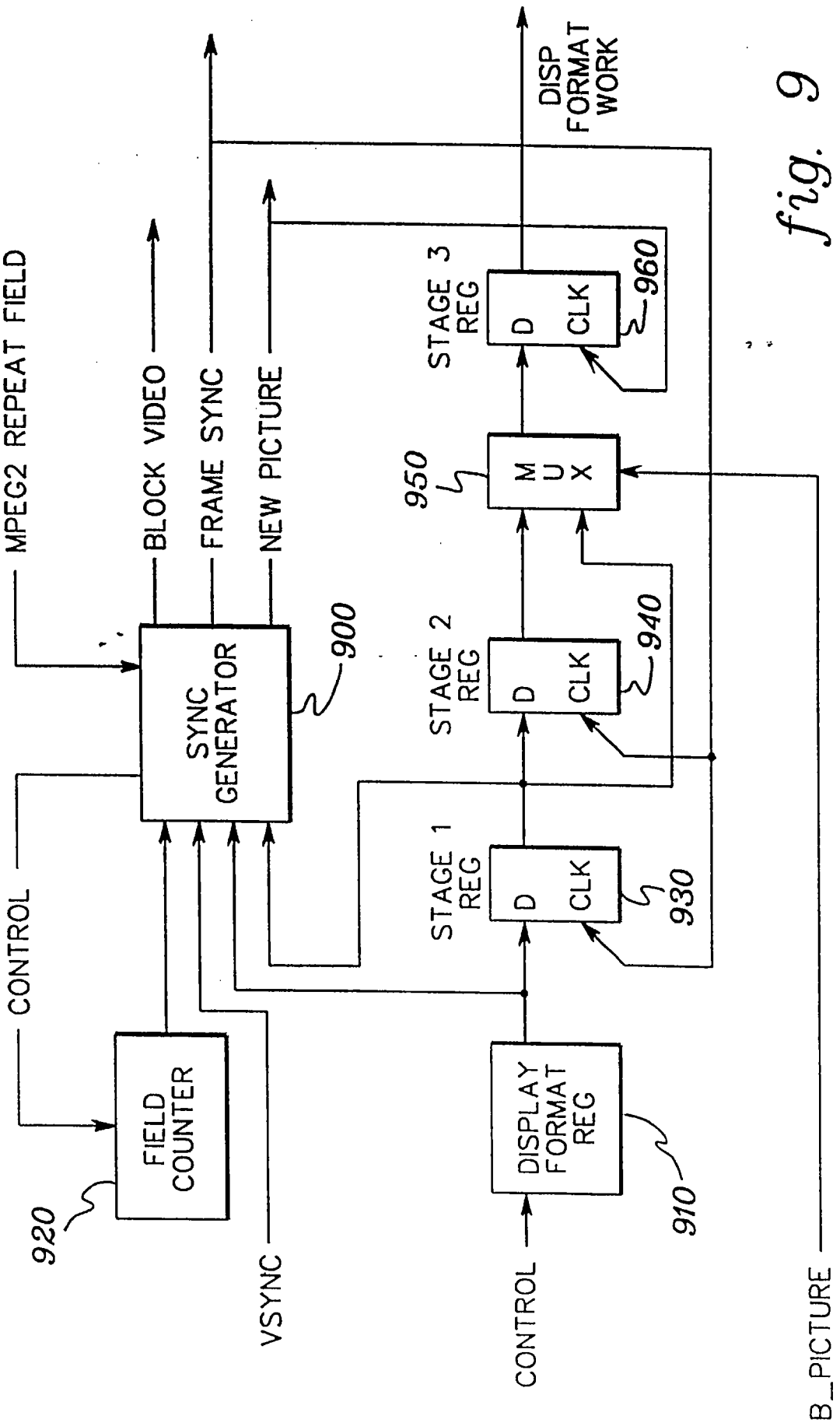

MPEG2 REPEAT FIELD
BLOCK VIDEO
FRAME SYNC
NEW PICTURE
DISP FORMAT WORK
SYNC GENERATOR
900
STAGE 3 REG
D
CLK
960
950
M U X
STAGE 2 REG
940
STAGE 1 REG
930
CONTROL
FIELD COUNTER
920
VSYNC
DISPLAY FORMAT REG
910
CONTROL
B_PICTURE

fig. 9

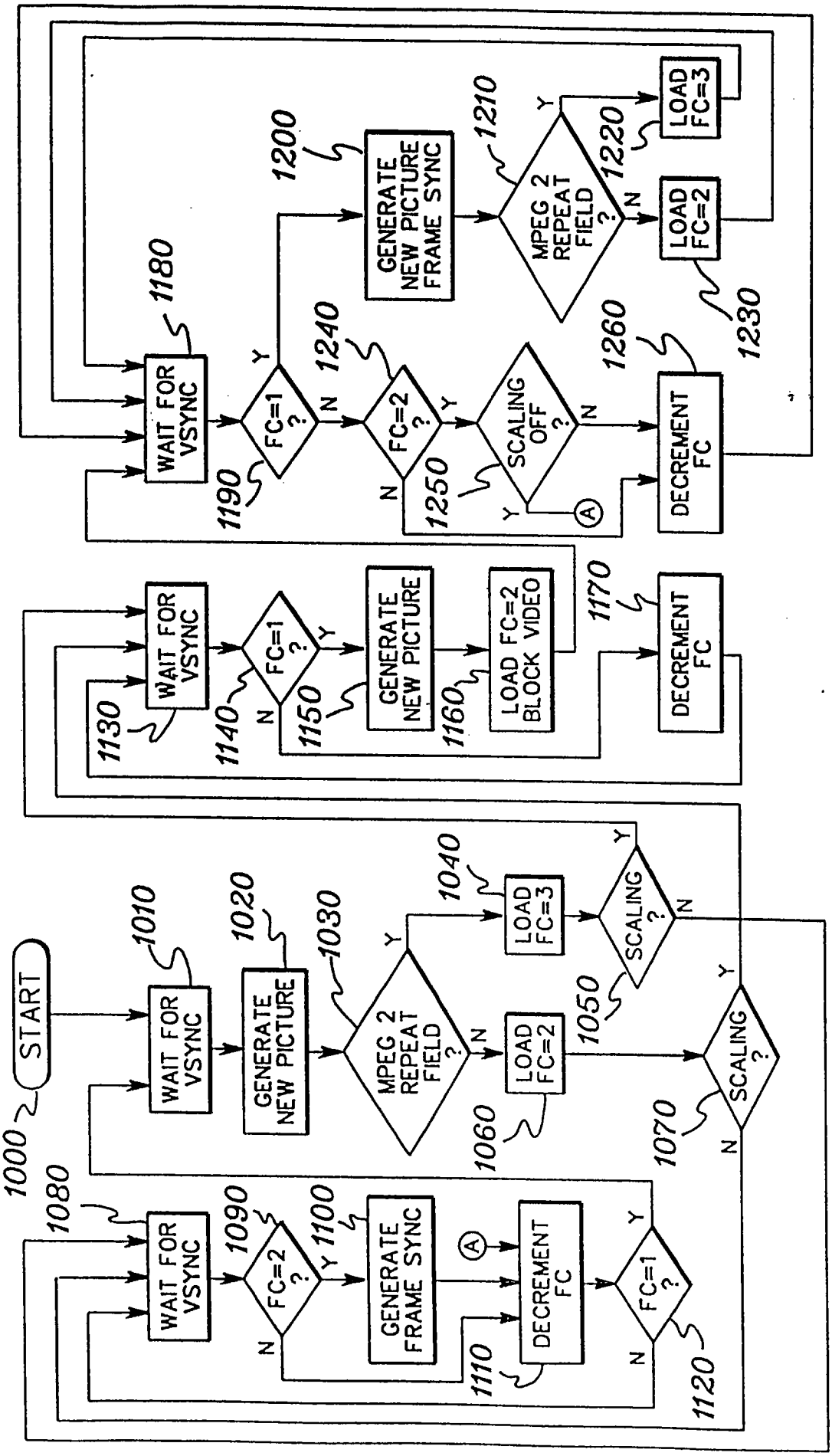

START
1000
WAIT FOR VSYNC
1010
GENERATE NEW PICTURE
1020
MPEG 2 REPEAT FIELD ?
1030
LOAD FC=3
1040
SCALING ?
1050
LOAD FC=2
1060
SCALING ?
1070
WAIT FOR VSYNC
1080
FC=2 ?
1090
GENERATE FRAME SYNC
1100
DECREMENT FC
1110
FC=1 ?
1120
WAIT FOR VSYNC
1130
FC=1 ?
1140
GENERATE NEW PICTURE
1150
LOAD FC=2 BLOCK VIDEO
1160
DECREMENT FC
1170
WAIT FOR VSYNC
1180
FC=1 ?
1190
GENERATE NEW PICTURE FRAME SYNC
1200
MPEG 2 REPEAT FIELD ?
1210
LOAD FC=3
1220
LOAD FC=2
1230
FC=2 ?
1240
SCALING OFF ?
1250
DECREMENT FC
1260
A
Y
N

fig. 10