

Abstract:

Current divider and integrated circuit comprising a plurality of current dividers.

A current divider for linearly dividing a first signal current (I_{i10}) into a second and a third signal current (I_{o11} , I_{o12}) comprises a first terminal (I_{10}) for the passage of the first signal current (I_{i10}), a second terminal (O_{11}) for the passage of the second signal current (I_{o11}) and for receiving a first potential, a third terminal (O_{12}) for the passage of the third signal current (I_{o12}) and for receiving a second potential, a first MOS transistor (M_1) having a control electrode and a main current path, and a second MOS transistor (M_2) having a control electrode and a main current path, the control electrodes of the first and the second MOS transistor (M_1 , M_2) being coupled to a first reference terminal (R_{10}) for receiving a first reference voltage (R_{v10}) to realise a conductive state of the first and the second MOS transistor (M_1 , M_2) during a first active state of the current divider, the main current path of the first MOS transistor (M_1) being coupled between the first terminal (I_{10}) and the second terminal (O_{11}), and the main current path of the second MOS transistor (M_2) being coupled between the first terminal (I_{10}) and the third terminal (O_{12}). The current divider effect a current division such that the dimensions of the MOS transistors used dictate the proportion of the respective signals currents realised by the current divider.

(Figure 1)

This Sheet Has Been Replaced

