WHAT IS CLAIMED IS:

1. A method comprising:

providing a first chip, the first chip having a substrate and a plurality of dielectric layers disposed on a front side of the substrate, the plurality of dielectric layers having metallization layers formed therein;

bonding a first surface of the plurality of dielectric layers of the first chip to a surface of a second chip, the first surface of the plurality of dielectric layers and the front side of the substrate facing the surface of the second chip;

forming an anti-reflection coating layer over a backside of the substrate;

forming a first trench extending through the anti-reflection coating layer and into the backside of the substrate;

forming a plurality of liners along sidewalls and a bottom of the first trench, wherein forming the plurality of liners comprises:

depositing a first liner of the plurality of liners in physical contact with a semiconductor material of the substrate and the anti-reflection coating layer; and

depositing a second liner of the plurality of liners on the first liner of the plurality of liners;

forming a second trench extending from the bottom of the first trench through the plurality of dielectric layers to a metallization layer in the second chip;

forming a barrier layer along sidewalls and a bottom of the second trench;

forming a conductive material in the first trench and the second trench, a topmost surface of the second liner of the plurality of liners being level with a topmost surface of the first liner of the plurality of liners.

forming a cap layer over the conductive material and the backside of the substrate, the cap layer and the barrier layer comprising different materials, the conductive material being interposed between the cap layer and the second chip.

2. The method of claim 1, wherein a subset of the plurality of liners extend over a backside of the first chip, and wherein the cap layer extends over the subset of the plurality of liners.

3. The method of claim 1, wherein the second trench extends to and between conductive pads in the plurality of dielectric layers on the substrate and to a conductive pad formed in a dielectric layer of the second chip.

4. A method comprising:

forming a bonded structure having a first substrate bonded to a second substrate, the first substrate having one or more first dielectric layers disposed thereon and a first conductive interconnect is disposed in the one or more first dielectric layers, the second substrate having one or more second dielectric layers disposed thereon and a second conductive interconnect is disposed in the one or more second dielectric layers, the first substrate being bonded to the second substrate such that the first dielectric layers face the second dielectric layers;

forming a first opening extending through the first substrate;

forming a plurality of third dielectric layers along sidewalls and a bottom of the first opening, wherein forming the plurality of third dielectric layers comprises:

forming a first one of the plurality of third dielectric layers along the sidewalls and the bottom of the first opening, the first one of the plurality of third dielectric layers being in physical contact with a semiconductor material of the first substrate; and

forming a second one of the plurality of third dielectric layers over the first one of the plurality of third dielectric layers, the second one of the plurality of third dielectric layers being in physical contact with the first one of the plurality of third dielectric layers;

after the forming the plurality of third dielectric layers, etching a second opening extending from the first opening to a first pad formed in at least one of the first dielectric layers and a second pad formed in at least one of the second dielectric layers, the second opening having a width less than a width of the first opening, wherein etching the second opening comprises partially etching the first pad;

forming a conductive plug in the first opening and the second opening, a topmost surface of the conductive plug being level with a topmost surface of the first one of the plurality of third dielectric layers and a topmost surface of the second one of the plurality of third dielectric layers; and

after the forming the conductive plug, forming a cap layer over a backside of the first substrate, the cap layer being in physical contact with the topmost surface of the conductive plug, the topmost surface of the first one of the plurality of third dielectric layers, and the topmost surface of the second one of the plurality of third dielectric layers.

5. The method of claim 4, further comprising, prior to the forming the conductive plug, forming a liner along sidewalls of the first opening and the second opening.

6. The method of claim 4, wherein less than all of the plurality of third dielectric layers extend over the backside of the first substrate.

7. The method of claim 4, wherein the first one of the plurality of third dielectric layers comprises a nitride layer, and wherein the second one of the plurality of third dielectric layers comprises an oxide layer.

8. A method comprising:

bonding a first semiconductor chip to a second semiconductor chip, wherein the first semiconductor chip comprises a first substrate, a plurality of first dielectric layers and a plurality of first metal lines formed in the first dielectric layers over the first substrate, wherein the second semiconductor chip comprises a second substrate, a plurality of second dielectric layers and a plurality of second metal lines formed in the second dielectric layers over the second substrate;

forming a first opening in the first substrate, the first opening having a first width;

forming a second opening extending from a bottom of the first opening through the plurality of first dielectric layers and into the plurality of second dielectric layers, the second opening comprising:

a first portion having a second width less than the first width, wherein the first portion extends from the first substrate to one of the plurality of first metal lines; and

a second portion having a third width less than the second width, wherein the second portion extends from the first portion to one of the plurality of second metal lines, and wherein a single patterning mask is used to etch both the first portion and the second portion of the second opening;

forming a plurality of liners along a bottom and sidewalls of the first opening, wherein forming the plurality of liners comprises:

depositing a first liner layer along the bottom and the sidewalls of the first opening, the first liner layer being in physical contact with a semiconductor material of the first substrate;

depositing a second liner layer over the first liner layer, the second liner layer being in physical contact with the first liner layer; and

removing a portion of the second liner layer to expose a topmost surface of the first liner layer;

forming a conductive plug in the first opening and the second opening, at least one of the plurality of liners not extending between a sidewall of the conductive plug and sidewalls of the plurality of first dielectric layers; and

after forming the conductive plug, forming a cap layer over the conductive plug, the cap layer comprising a dielectric material, the cap layer contacting a topmost surface of the conductive plug and a topmost surface of at least one of the plurality of liners.

9. The method of claim 8, wherein the cap layer extends over the plurality of liners.

10. The method of claim 8, wherein a subset of the plurality of liners extends over a backside of the first substrate.

11. The method of claim 8, wherein the conductive plug extends between two of the plurality of first metal lines in the first semiconductor chip.

12. The method of claim 8, further comprising forming at least one diffusion barrier layer between the conductive plug and one or more of the plurality of first dielectric layers.

13. The method of claim 8, wherein the plurality of liners includes an oxide layer and a nitride layer.

14. The method of claim 8, wherein the conductive plug electrically couples one of the plurality of first metal lines in the first semiconductor chip to the one of the plurality of second metal lines in the second semiconductor chip.

15. The method of claim 14, wherein the one of the plurality of first metal lines in the first semiconductor chip has a recess.

16. The method of claim 1, wherein forming the second trench comprises etching a metallization feature in the plurality of dielectric layers.

17. The method of claim 1, wherein a sidewall of the first liner of the plurality of liners and a sidewall of the second liner of the plurality of liners are coplanar.

18. The method of claim 17, wherein the sidewall of the first liner of the plurality of liners and the sidewall of the second liner of the plurality of liners physically contact the barrier layer.

19. The method of claim 5, wherein the liner comprises a diffusion barrier layer.

20. The method of claim 8, wherein the topmost surface of the conductive plug is level with the topmost surface of the at least one of the plurality of liners.