ABSTRACT

GAP FILLING PROCESS IN INTEGRATED CIRCUITS USING LOW DIELECTRIC CONSTANT MATERIALS

It is the general object of the present invention to provide an improved method of fabricating semiconductor integrated circuit devices, specifically by describing an improved process of fabricating multilevel metal structures using low dielectric constant materials. The present invention relates to an improved processing method for stable and planar intermetal dielectrics, with low dielectric constants. The first embodiment uses a stabilizing adhesion layer between the bottom, low dielectric constant layer and the top dielectric layer. The advantages are: (i) improved adhesion and stability of the low dielectric layer and the top dielectric oxide (ii) over all layer thickness of the dielectric layers can be reduced, hence lowering the parasitic capacitance of these layers. In the second embodiment, the method uses a multi-layered "hard mask" on metal interconnect lines with a silicon oxynitride DARC, dielectric anti-reflective coating on top of metal. A double coating scheme of low dielectric constant insulators are used in this application. The third embodiment uses a hard mask stack over the interconnect metal lines, with a silicon oxynitride DARC coating on top of metal, and an adhesion layer between the low dielectric material and the top dielectric layer.

(FIGURE 2a IS SUGGESTED FOR PUBLICATION)