CLAIMS

1. A semiconductor structure, comprising:

a substrate and a conductive structure located above the substrate, wherein

the substrate comprises a device area, and a first connection area and a second connection area that are respectively arranged on two sides of the device area;

the conductive structure comprises a plurality of first conductive structures and second conductive structures that are spaced apart from each other and extend in a first direction; and lengths of the first conductive structures vary in steps and lengths of the second conductive structures vary in steps;

the first conductive structures are located above the device area and extend to the first connection area, and the second conductive structures are located above the device area and extend to the second connection area; and the lengths of the first conductive structures located above the first connection area vary in steps, and the lengths of the second conductive structures located above the second connection area vary in steps;

wherein each first conductive structure and each second conductive structure above the device area surround a plurality of channel structures spaced apart from each other; and dielectric layers are arranged between the first conductive structure and the channel structures, and between the second conductive structure and the channel structures;

wherein each first conductive structure above the first connection area surrounds a first active layer, and a first insulation layer is arranged between the first conductive structure and the first active layer;

each second conductive structure above the second connection area surrounds a second active layer, and a second insulation layer is arranged between the second conductive structure and the second active layer.

2. The semiconductor structure of claim 1, wherein the lengths of the first conductive structures close to the substrate are greater than the lengths of the first conductive structures away from the substrate, such that the lengths of the plurality of first conductive structures vary in steps; and

the lengths of the second conductive structures close to the substrate are greater than the lengths of the second conductive structures away from the substrate, the lengths of the plurality of second conductive structures vary in steps.

3. The semiconductor structure of claim 1, wherein the plurality of first conductive structures and the plurality of second conductive structures are alternately arranged and spaced apart from each other in a second direction.

4. The semiconductor structure of claim 1, further comprising: a plurality of contact plugs spaced apart from each other, wherein the contact plugs comprise first contact plugs and second contact plugs;

a plurality of first contact plugs are in one-to-one correspondence with and electrically connected to the plurality of first conductive structures; and a plurality of second contact plugs are in one-to-one correspondence with and electrically connected to the plurality of second conductive structures.

5. The semiconductor structure of claim 4, wherein the plurality of first contact plugs and the plurality of second contact plugs extend in a second direction; and lengths of the plurality of first contact plugs and lengths of the plurality of second contact plugs vary in steps.

6. The semiconductor structure of claim 4, wherein the first contact plugs and the second contact plugs comprise first conductive portions and second conductive portions arranged on the first conductive portions; and sizes of the first conductive portions are less than sizes of the second conductive portions.

7. The semiconductor structure of claim 1, wherein the first active layer and the plurality of channel structures corresponding to a same first conductive structure are arranged at a same layer; and the second active layer and the plurality of channel structures corresponding to a same second conductive structure are arranged at a same layer.

8. A memory, comprising:

a substrate, comprising a device area, a first connection area and a second connection area; the device area is located between the first connection area and the second connection area;

a device layer, located above the device area, and comprising a plurality of channel structures spaced apart from each other;

a Word Line (WL) structure, comprising a plurality of WLs spaced apart from each other and extending in a first direction, wherein lengths of the plurality of WLs vary in steps;

a Bit Line (BL) structure, comprising a plurality of BLs spaced apart from each other and extending in a second direction, wherein

the WLs penetrate the device layer and surround the channel structures; the BLs penetrate the device layer and are electrically connected to the channel structures; and the channel structures are further electrically connected to storage nodes;

the lengths of the plurality of WLs located above the first connection area vary in steps; and the lengths of the plurality of WLs located above the second connection area vary in steps;

wherein each WLs above the first connection area surrounds a first active layer; each WLs above

the second connection area surrounds a second active layer.

9. The memory of claim 8, wherein each BL is connected to first ends of the plurality of channel structures spaced apart from each other in the second direction, and second ends of the channel structures are connected to the storage nodes.

10. The memory of claim 8, wherein the substrate located in the device area is spaced apart from the substrate located between the first connection area and the second connection area.

11. A method for manufacturing a semiconductor structure, comprising:

providing a substrate;

wherein the substrate comprises a device area, a first connection area and a second connection area that are respectively arranged on two sides of the device area;

forming a conductive structure above the substrate, wherein the conductive structure comprises a plurality of first conductive structures and second conductive structures that are spaced apart from each other and extend in a first direction; and lengths of the first conductive structures vary in steps and lengths of the second conductive structures vary in steps;

the first conductive structures are located above the device area and extend to the first connection area, and the second conductive structures are located above the device area and extend to the second connection area; and the lengths of the first conductive structures located above the first connection area vary in steps, and the lengths of the second conductive structures located above the second connection area vary in steps;

wherein each first conductive structure and each second conductive structure above the device area surround a plurality of channel structures spaced apart from each other; and dielectric layers are arranged between the first conductive structure and the channel structures, and between the second conductive structure and the channel structures;

wherein each first conductive structure above the first connection area surrounds a first active layer, and a first insulation layer is arranged between the first conductive structure and the first active layer;

each second conductive structure above the second connection area surrounds a second active layer, and a second insulation layer is arranged between the second conductive structure and the second active layer.

12. The manufacturing method of claim 11, wherein the forming a conductive structure above the substrate comprises:

respectively forming a first laminated structure, a second laminated structure, and a third laminated

structure in the device area, the first connection area, and the second connection area of the substrate, wherein the first laminated structure comprises first sacrificial layers and device layers that are alternately stacked, the second laminated structure comprises second sacrificial layers and first active layers that are alternately stacked, the third laminated structure comprises third sacrificial layers and second active layers that are alternately stacked, a plurality of first active layer are in one-to-one correspondence with the device layers of a first portion, and a plurality of second active layers are in one-to-one correspondence with the device layers of a second portion;

removing the first sacrificial layer and parts of the device layers, such that each device layer forms a plurality of channel structures spaced apart from each other;

removing parts of the first active layers and parts of the second active layers away from the channel structures, such that lengths of the remaining first active layers and the second active layers vary in steps; and

forming a first conductive structure on the first active layers and the channel structures corresponding to the first active layers, and forming a second conductive structure on the second active layers and the channel structures corresponding to the second active layers.

13. The manufacturing method of claim 12, wherein the plurality of first active layers and the device layers at odd layers correspond to each other and are arranged at a same layer, and the plurality of second active layers and the device layers at even layers correspond to each other and are arranged at a same layer.

14. The manufacturing method of claim 12, wherein before forming the first conductive structure on the first active layers and the channel structures corresponding to the first active layers, and forming the second conductive structure on the second active layers and the channel structures corresponding to the second active layers, the manufacturing method further comprises:

depositing an insulation material on the first active layers, the second active layers, and the channel structures, wherein the insulation material located on the first active layers forms a first insulation layer, the insulation material located on the channel structures forms a dielectric layer, the insulation material located on the second active layers forms a second insulation layer, and the first insulation layer, the dielectric layer, and the second insulation layer are spaced apart from each other.

15. The manufacturing method of claim 11, wherein after forming the conductive structure above the substrate, the manufacturing method further comprises:

forming a plurality of contact plugs spaced apart from each other, wherein the contact plugs comprise first contact plugs and second contact plugs; a plurality of first contact plugs are in one-to-one correspondence with and electrically connected to the plurality of first conductive structures; a plurality of second contact plugs are in one-to-one correspondence with and electrically connected to the plurality of second conductive

structures; lengths of the plurality of second contact plugs vary in steps and the plurality of first contact plugs vary in steps.