

SEMICONDUCTOR-INTEGRATED-CIRCUIT SRAM-**CELL ARRAY WITH SINGLE-ENDED CURRENT-SENSING****Field of Invention**

This invention relates to semiconductor-integrated-circuit memory circuitry and more particularly to semiconductor static random access memory ("SRAM") cell cross-point arrays -- i.e., arrays of cells in which each of the cells is
5 located at a crossing of a row line with a column line.

Background of Invention

A semiconductor-integrated-circuit SRAM cell is a memory cell, in the form of electrical circuitry integrated in a semiconductor body, that retains its binary digital memory storage state (i.e., a 0 or a 1: a low or a high) for as long a
10 time as dc electrical power is applied to the cell or until it is written again with a different binary digital signal (i.e., a 1 or a 0, respectively). In one design, such a cell is formed by a pair of cross-coupled transistors, each of the transistors being connected in series with a separate load device. Each of these load devices can
15 simply be a resistor such as provided by suitably connected transistor (diode). In another design, such a cell is formed by electrical circuitry comprising two pairs of cross-coupled transistors connected in series with each other--one pair comprising a pair of cross-coupled n-channel MOS (Metal Oxide Semiconductor) transistors, and the other pair comprising a pair of cross-coupled p-channel MOS transistors. In
20 any event, the semiconductor body in which a cross-point memory array is integrated is typically silicon, but it is known that similar arrays can be constructed in other semiconductor bodies such as compound Group III-V semiconductors like GaAs (gallium arsenide).

In some practical applications of SRAM cell arrays, a capability of reading one cell located on a given column and simultaneously (i.e., during a single
25 read-write cycle) writing another cell located on the same given column is desirable: this capability allows a desirably faster overall performance. This capability will be referred to as a "simultaneous read-write" capability.



To this end, a paper by H. Kadota et al published in IEEE Journal of Solid-State Circuits, Vol. SC-17, pp. 892 - 897 (1982) and entitled "A New Register-File Structure for the High-Speed Microprocessor" teaches circuitry for accessing an SRAM cross-point-memory-cell array. Also, a paper by Kevin J. O'Connor published in IEEE Journal of Solid-State Circuits, Vol. SC-22, pp. 712 - 719 (1987) and entitled "The Twin-Port Memory Cell" teaches [at Fig. 2(b)] circuitry for accessing such an array. The circuitry taught in those papers involved arrays of "dual-port" SRAM cells -- i.e., SRAM cells in which electrical access to (and hence selection of) each cell is provided by four column lines per column of cells (a pair of column lines located on either side of the cell) while each column line of a given pair carried the opposite binary digital signal from the other. In addition, access to (and hence selection of) each cell located on a given row was controlled by a pair of row lines (one such pair for each such row of cells): one of the pair controlled the reading while the other of the pair independently controlled the writing of the cells located on the row. Detection of the 0 vs. 1 memory state of a selected cell was accomplished by means of a voltage sensing device, such as an amplifier and flip-flop circuitry. Such dual-port cells, when located in an array having more than a single row, thus achieved the above-mentioned simultaneous read-write capability. In addition, such dual port cells (as a result of being dual port, i.e., having two pairs of column bit lines associated with each cell) enjoyed the advantage of not requiring boosted (higher-applied-voltage) row lines.

The circuitry taught in the above-described prior art, however, required a total of four column lines plus two column power lines for each column of cells, in addition to two row lines, whereby an undesirable amount of added precious semiconductor area was needed to accommodate the total of six column lines plus the two row lines. It would therefore be desirable to an SRAM cross-point-memory-cell array having fewer than six column lines per column of cells while retaining the above-mentioned read-write capability.

Summary of Invention

The inventive circuitry is set forth in claim 1. Preferred forms of the circuitry are set forth in the dependent claims.

In this way, a total of only four column lines and two row lines are required or, in the alternative a total of only three column lines and three row lines are required.

Brief Description of the Drawings

5 FIG. 1 is a block diagram of SRAM integrated circuitry with single-ended electrical current sensing, according to a specific embodiment of the invention;

FIG. 2 is a circuit schematic of an SRAM cell that can be used in the block diagram of FIG. 1, according to a specific embodiment of the invention; and

10 FIG. 3 is a block diagram of SRAM integrated circuitry with single-ended electrical current sensing, in accordance with another specific embodiment of the invention.

Detailed Description

15 As indicated in FIG. 1, SRAM circuitry with single-ended electrical sensing comprises an array 100 of SRAM cells, labeled $C_{i,j}$ and so forth. The first index i refers to the row; the second index j , to the column. The array may contain only a single column of cells. All cells have the same internal construction (FIG. 2) and typically are integrated in a silicon semiconductor chip, as known in the art.

20 More specifically, as shown in FIG. 2, the (illustrative) cell 200 (which is identical to a cell like $C_{i,j}$) has a pair of cross coupled NMOS transistors MN1 and MN2 respectively connected in series with a pair of cross-coupled PMOS transistors MP1 and MP2, as known in the art. Output terminals (or "nodes") N1 and N2 are respectively located between the transistors MN1 and MP1 and between
25 the transistors MN2 and MP2. Access NMOS transistors MW1 and MW2 respectively connect, via their respective high-current-carrying terminals, the output nodes N1 and N2 to complementary column bit lines B_j and $\bar{B}_j$, as known in the art. A row write line PW_i is separately connected to a control terminal (gate



electrode) of each of the access transistors MW1 and MW2, as known in the art. One end of a column power line VDD is connected to a voltage source 101, as known in the art; another end is connected to a node N3. This node N3 is connected to one of a pair of high-current-carrying terminals of both the transistors MP1 and MP2, as known in the art. A node N4 connects together the other of the pair of high-carrying terminals of the transistors MN1 and MN2, also as known in the art.

A row *read* line RR_i is connected to a control terminal of an auxiliary reading-transistor MR1. A pair of high-current-carrying terminals of this reading-transistor MR1 connects the node N3 to the node N1 (alternatively to the node N2). Finally the node N4 is connected to a column detector line D_j that terminates in an electrical current sensor S_j (FIG. 1), advantageously only one such current sensor S_j per column. Each such current sensor S_j typically can take the form of a current sense amplifier comprising (not shown) a resistor with a voltmeter connected across it. The voltmeter advantageously comprises a CMOS flip-flop detector, arranged to form a current sense amplifier with input level shifting as known in the art. In any event, the resistance of the resistor is advantageously significantly lower than that of the voltmeter, so that the RC time constant of the current sensor is suitably low. On the other hand, the resistance of the auxiliary transistor MR1 is sufficiently high, so as not to draw undue amounts of current from the power line VDD and hence so as not to cause undue amounts of power consumption.

As known in the art, during electrical operations the cell 200 can have two memory states: in the one state MP1 is OFF, MN1 is ON, MP2 is ON, and MN2 is OFF; in the other state MP1 is ON, MN1 is OFF, MP2 is OFF, and MN2 is ON. The purpose of the auxiliary reading transistor MR1 is to provide a desired low-resistance current path from VDD to the detector line D_j (and hence to the current sensor S_j) via the cell 200 if and only if the cell 200 is in the one memory state but not in the other memory state. More simply, the auxiliary reading transistor MR1 provides a low-resistance path from the node N3 to the node N4 if and only if the cell is in the one memory state but not in the other. More specifically, if the cell 200 is in the memory state in which MP1 is OFF and

MN1 is ON (MP2 is ON and MN2 is OFF), then if it is desired to read the cell 200, a HIGH level signal is applied to the row *read* line RR_i to turn ON the auxiliary reading transistor MR1 -- whereby a low resistance path through the cell 200 exists through MR1 and MN1, so that the current sensor S_j will indicate a
5 HIGH current . On the other hand, if the cell 200 is in the memory state in which MP1 is ON and MN1 is OFF (MP2 is OFF and MN2 is OFF), then even if the auxiliary transistor MR1 is turned ON, no such low resistance path through the cell 200 can exist: if MN1 is OFF, since MP2 is then necessarily OFF (owing to the cross-coupling connections of the transistors in the cell 200) there is therefore
10 no way such a low-resistance path can exist. Thus the auxiliary reading transistor MR1 indeed serves to enable reading of the cell 200.

On the other hand, writing of the cell 200 is accomplished as in prior art: a HIGH level signal is applied to the row *write* line RW_i , whereby the access transistors MW1 and MW2 are turned ON so that the column bit lines B_j and $\bar{B}_j$
15 can be connected to the nodes N1 and N2, respectively, in order to write the cell 200, as known in the art. Moreover, if desired, one cell on a given column can be written while another cell on the same column can be read: for example, a cell such as $C_{i,j}$ can be written while a cell such as $C_{i+2,j}$ can simultaneously (i.e., during a single read-write cycle) be read.

20 In order to implement such a simultaneous writing of one cell and reading of another cell (both cells located on the j 'th column) -- specifically to write the cell $C_{i,j}$ and to read the cell $C_{i+2,j}$ -- a HIGH level signal is applied to the row *write* line RW_i while a HIGH level signal is applied to the row *read* line RR_{i+2} . At the same time, a LOW level signal is applied to all the other row *read* and row
25 *write* lines. In this way, insofar as the j 'th column is concerned, only the cell $C_{i,j}$ can be written (by means of complementary HIGH or LOW signals applied to the column bit lines B_j and $\bar{B}_j$, respectively, depending upon the desired memory state to be written), and at the same time only the cell $C_{i+2,j}$ can be read because of the low-resistance path from VDD to the detector line D_j and thus to the current sensor
30 S_j through the cell $C_{i+2,j}$ (i.e., from the node N3 to the node N4). However, no such low-resistance path will then exist through any other cell located on the j 'th

column, as is desired for reading one cell without having another cell delivering a confusing current signal.

As indicated in FIG. 1, between adjacent cells located on a given row, the row *read* line RR_i and the row *write* line RW_i are parallel. Between adjacent cells located on a given column, the power line VDD and the column-detector line D_j are parallel to the column bit lines B_j and $\bar{B}_j$. In this way, the circuitry shown in FIG. 1 entails a total of four (electrically conductive) column lines (VDD, B_j , $\bar{B}_j$, D_j) per column and two (electrically conductive) row lines (RW_i , RR_i) per row.

In accordance with another specific embodiment of the invention, in an array 300 (Fig. 3) the same cells $C_{i,j}$ *et cetera* are used as were used in the circuitry 100 shown in FIG. 1. On the other hand, the power line VDD is arranged such that, between adjacent cells, it runs parallel to the row lines RW_i and RR_i rather than parallel to the column lines B_j and $\bar{B}_j$. In this way, as indicated in FIG. 3, the circuitry can be arranged so that there are a total of three column lines (B_j , $\bar{B}_j$, D_j) per column and three row lines (VDD, RW_i , RR_i) per row.

Although the invention has been described in detail with reference to specific embodiments, various modifications can be made without departing from the scope of the invention. For example, instead of being an NMOS transistor the auxiliary reading transistor MR1 can be a PMOS transistor. Instead of being connected across the transistor MP1, the transistor MR1 can be connected across the transistor MN1, MP2, or MN2. Instead of more than two rows, there can be as few as two rows, and instead of more than one column there can be as few as only a single column -- whereby, during a single read-write cycle, the cell located on the one row can be written while the cell located on the other row can be read. Also, instead of the cross-coupled PMOS transistors MP1 and MP2, resistive load devices can be used such as thin film resistors or polysilicon resistors, provided that they have sufficiently high resistance so that the current flowing through them is significantly smaller than the current flowing through the auxiliary reading transistor MR1 in its ON condition.

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Claims:**1. Semiconductor integrated circuitry comprising:**

- (a) a row-column array including a plurality of SRAM cells integrated in a semiconductor body, each of the cells having a separate power terminal, a separate detector terminal, and separate first and second access transistors, each of the access transistors having a pair of high current carrying terminals and a control terminal, the plurality including first and second SRAM cells located at an intersection of first and second rows, respectively, with a first column;
- (b) first and second electrically conductive column lines located adjacent to the first column, a first and a second output terminal of each of the first and second SRAM cells being connected to the first and second column lines, respectively, through the high current carrying terminals of the first and second access transistors, respectively, of the first and second cells, respectively;
- (c) a first pair of electrically conductive row lines located adjacent to the first row, and a second pair of electrically conductive row lines located adjacent to the second row;
- (d) first and second electrical conductors connecting one of the row lines of the first and second pairs of row lines to the control terminals of both of the access transistors of the first and second cells, respectively;
- (e) a power line connected to the power terminal of both of the cells;
- (f) first and second auxiliary transistors located in the first and second cells, respectively, and having a control terminal that is separately connected to the other row line of the first and second pairs, respectively, and having first and second high current carrying terminals respectively connected to

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the power line and to the first output terminal of the first and second cells, respectively; and

(g) a current sensing device connected to the detector line.

5 2. Circuitry according to claim 1 in which each of the cells comprises a pair of cross-coupled transistor drivers that are separately connected in series with a separate load device.

10 3. Circuitry according to claim 1 in which each of the cells comprises a pair of cross-coupled n-channel transistors separately connected in series with a pair of cross-coupled p-channel transistors.

15 4. Circuitry according to claim 3 in which the n-channel transistors are NMOS transistors, the p-channel transistors are PMOS transistors, the auxiliary transistor is an NMOS transistor, and the first power terminal is connected to a high current carrying terminal of both of the PMOS transistors.

5. Circuitry according to claim 1 in which the second power line runs essentially parallel to the first and second column lines.

20 6. Circuitry according to claim 1, 2, 3, or 4, in which between the first and second cells the first power line runs essentially parallel to the first and second column lines.

25 7. Circuitry according to claim 1 in which the second power line runs, within the array, essentially parallel to the row lines.

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