(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
17 June 2004 (17.06.2004)

PCT

(10) International Publication Number
WO 2004/051753 A1

(51) International Patent Classification[7]: H01L 29/792

(21) International Application Number:
PCT/US2003/021676

(22) International Filing Date: 10 July 2003 (10.07.2003)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
10/306,252 27 November 2002 (27.11.2002) US

(71) Applicant: ADVANCED MICRO DEVICES, INC. [US/US]; One AMD Place, Mail Stop 68, Sunnyvale, CA 94088-3453 (US).

(72) Inventors: RANDOLPH, Mark, W.; 3673 Kendra Way, San Jose, CA 95130 (US). CHANG, Chi; 342 Lakeview Way, Redwood City, CA 94062 (US). HE, Yi; 3919 Riverbend Terrace, Fremont, CA 94555 (US). ZHENG, Wei; 2726 Estella Drive, Santa Clara, CA 95051 (US). RUNNION, Edward, F.; 801 Creekside Place, Santa Clara, CA 95051 (US).

(74) Agent: COLLOPY, Daniel, R.; Advanced Micro Devices, Inc., One AMD Place, Mail Stop 68, Sunnyvale, CA 94088-3453 (US).

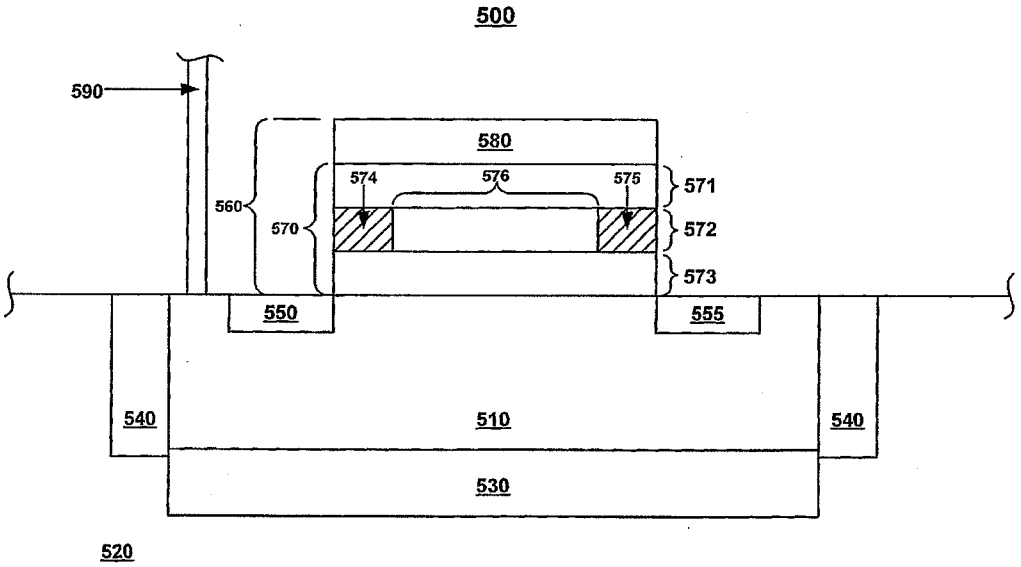
(81) Designated States *(national)*: AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DZ, EC, EE, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, MZ, NO, NZ, OM, PH, PL, PT, RO, RU, SC, SD, SE, SG, SK, SL, TJ, TM, TN, TR, TT, TZ, UA, UZ, VC, VN, YU, ZA, ZM, ZW.

(84) Designated States *(regional)*: ARIPO patent (GH, GM, KE, LS, MW, MZ, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European patent (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HU, IE, IT, LU, MC, NL, PT, RO, SE, SI, SK, TR), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

Published:
— *with international search report*

For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

(54) Title: SILICON NITRADE CHARGE TRAPPING MEMORY DEVICE



(57) Abstract: The present invention is a method and system for erasing a nitride memory device. In one embodiment of the present invention, an isolated P-well (510) is formed in a semiconductor substrate (529). A plurality of N-type impurity concentrations (550, 555) are formed in the isolated P-well (510) and a nitride memory cell (560) is fabricated between two of the N-type impurity concentrations (550, 555). Finally, an electrical contact (590) is coupled to the isolated P-well (510).

WO 2004/051753 A1