

COLUMN ADDRESS COUNTER WITH MINUS 2 SUBTRACTOR FOR ADDRESS COMPARE

Abstract of the Disclosure

The present invention is a method and apparatus method and circuit for providing a burst address counter with a fast burst-done signal. In a preferred embodiment, a synchronous memory device includes a counter for producing a sequence of burst addresses, based on an external address. In addition, the counter drives the burst-done signal to indicate completion of the burst sequence. The counter includes a register for receiving the external address, an incrementor for incrementing the external address to produce the next address of the sequence of burst addresses, a minus-two subtractor for determining a second-to-last burst address of the burst sequence, and a comparator. By utilizing the minus-two subtractor, the comparator can determine the end of the burst sequence earlier than conventional counters. This is because the minus-two subtractor determines the next-to-last address of the sequence, which allows the comparator to start asserting the burst-done signal at an earlier time.

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