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(54) Title: DATA CACHE WITH DATA STORAGE AND TAG LOGIC WITH DIFFERENT CLOCKS

(57) Abstract

A processor (210) includes a cache memory with a data storage unit (310) operating at a first clock frequency, and a tag unit and hit/miss logic operating at a second clock frequency different than the first clock frequency. The data storage unit (310) may advantageously be clocked faster than the tag unit and hit/miss logic, such as 2 times (2X) faster. This cache structure may advantageously be used as an L0 data cache in a microprocessor, especially in one which has plural execution core sections operating at the different clock frequencies. The processor (210) may utilise speculative data and has a "replay" function when the speculative data read from the cache turns out to be invalid.

