(12)

PATENT SPECIFICATION (11) 1 550 834

1 550 834

(21) Application No. 31057/75 (22) Filed 24 July 1975
(23) Complete Specification filed 22 July 1976
(44) Complete Specification published 22 Aug. 1979
(51) INT CL² H01L 23/50
(52) Index at acceptance
H1K 4C3E 4C5K 4C8 4F11G 4F11S 4F14A 4F15 4F1C 4F20 4F21 4F30 4F6 4F7A 4F7B 4F7C 4F8A 4F8B 4F9 RA
C7A A237 A239 A23Y A241 A243 A245 A247 A249 A24X A259 A25Y A260 A263 A28X A28Y A30Y A313 A316 A319 A320 A323 A326 A329 A337 A339 A33Y A340 A341 A343 A345 A347 A349 A35Y A362 A364 A366 A369 A389 A390 A394 A396 A398 A39Y A400 A402 A404 A406 A409 A40Y A41Y A432 A435 A437 A439 A459 A48Y A491 A493 A495 A497 A499 A49X A501 A503 A505 A507 A509 A50X A529 A539 A53Y A541 A543 A545 A547 A549 A54X A55Y A565 A568 A571 A574 A577 A579 A57Y A589 A58Y A591 A593 A595 A599 A59X A609 A617 A619 A61Y A621 A623 A625 A627 A629 A62X A671 A673 A675 A677 A679 A67X A681 A683 A685 A687 A689 A68X A693 A695 A697 A699 A69X A70X

(72) Inventors RODNEY VICTOR MAJOR and MICHAEL CHARLES MARTIN

(54) SEMICONDUCTOR DEVICES

(71) We, TELCON METALS LIMITED, a British Company of P.O. Box 12, Manor Royal, Crawley, Sussex RH10 2QH, do hereby declare the invention, for which we pray that a patent may be granted to us, and the method by which it is to be performed, to be particularly described in and by the following statement:—

This invention relates to semiconductor devices in which a plurality of metallic leads are attached in prearranged positions on a "chip" of silicon and primarily to the so-called integrated circuits. The practice is to form such devices by attaching the chip to a "lead frame" stamped from suitable metal sheet and comprising the required leads together with temporary bridging members securing them in prearranged positions to form an assembly that can be handled with reasonable facility before and during attachment of the chip thereto. Typically the chip is first secured to a support forming part of the lead frame (and in some cases constituting one of the leads), then the leads (or the remaining leads) are wired to the chip and the chip and the contiguous parts of the lead frame are subsequently encapsulated, after which the bridging portions can be cut away to separate the leads electrically from one another.

The standard procedure for securing the chip to the lead frame requires local heating at temperatures up to about 500°C, and it has therefore been the practice to use for the lead frame an alloy with a thermal expansion coefficient closely matched to that of the semiconductor chip (about 4.5×10^{-6} per C°); originally the assembly would have been encapsulated in glass with a thermal expansion coefficient also closely matched by that of the alloy, but more recently plastics materials have been used for encapsulation, relying on their resilience to avoid need for matching expansion coefficients.

The lead frame metal must also exhibit good stamping and bending properties and (both to simplify storage of material before stamping and stamped blanks before plating and also since any plating will be discontinuously in the finished semiconductor device where bridges have been cut) must have good corrosion resistance; it should also have adequate electrical and thermal conductivities.

Hitherto these requirements have necessitated use of alloys containing a large proportion of nickel, which is relatively expensive and, like all the less common metals, may be subject to shortages due to limited world production capacity at periods of peak demand.

We have now discovered that the very close matching of expansion coefficients hitherto practiced is not essential, especially when encapsulation is in resilient material, and that this enables certain alloys containing little or no nickel to be used.

In accordance with the invention, the leads of a silicon integrated circuit or other silicon semiconductor device are made of an alloy with a temperature coefficient of

expansion up to 13×10^{-6} per °C having the following composition, with or without a conductive metallic coating:

Chromium	8—14%
Molybdenum	0—1.5%
Cobalt	0—8%
Vanadium	0—6%
Manganese	0—1.5%
Carbon	0—0.3%
Silicon	0—1%
Niobium (Columbium)	0—2%
Nickel	0—2%
Tungsten	0—1%
Copper	0—1.5%
Aluminium	0—4%
Iron and impurities	balance,

the chip and part of each of the leads being encapsulated. Preferably at least one of molybdenum, cobalt, vanadium and manganese is present in the range indicated. Preferably the optional ingredients, other than molybdenum, cobalt, vanadium and manganese but together with impurities, are limited to an amount less than about 2.5% in all, and in most cases we prefer to limit all ingredients except chromium, molybdenum, cobalt, vanadium, manganese and iron to 0.75% in all, and usually to exclude them as far as possible.

The invention will be further described, by way of example, with reference to the accompanying drawings in which

Figure 1 is a plan view of a strip of lead frames, and

Figure 2 is a plan view, drawn on a larger scale, of a different design of lead frame attached and connected to a semiconductor chip and ready for encapsulation.

The stamping of Figure 1 is of indefinite length and comprises a series of identical lead frames 1 with short connecting links 2. Each lead frame comprises a number of lead members 3 (fourteen of them in this particular example) each including a body part 4, a pin part 5 (for eventual external connections) and a contact part 6 which extends into, and has a free end 7 within, a central area with an imaginary boundary 8. The lead members 3 are all connected together by bridging members 9 all of which are located outside the boundary 8 and some of which form a rectangular outer border 10. Tabs 11 on this outer border assist in mechanical handling of the frames in the early stages of manufacture of the semiconductor devices. The frame also includes a support member 12 which is displayed, say a millimetre or so, from the plane of the frame, and is secured in the frame by cranked links 13.

In the alternative design shown in Figure 2, equivalent parts have been given the same reference numerals; the lead frame has been bent into a channel section, so that the bridging members 9 are seen edge-on. A silicon semiconductor chip 14 is bonded by its underside to the support member 12 and each of the contact parts 6 is connected to an appropriate point on the face of the chip by a wire 15 soldered at each of its ends 16. The assembly as shown is ready for encapsulation in a body of resin 17 which will give mechanical support to the lead members 3, after which the bridging members 9 can be cut away to remove the unwanted electrical connections between the lead members.

Lead frames used in accordance with the invention will normally be plated with a metallic substance (metal or alloy) of good corrosion resistance and electrical conductivity, such as silver, gold, or solder after stamping but before attachment to the semiconductor chip.

Example 1

An alloy comprising 11.8% chromium, 4.3% cobalt, 0.26% manganese, 0.016% carbon, less than 0.05% silicon, 0.004% sulphur (impurity), balance iron was prepared by vacuum induction melting and cast into ingots. The ingots were hot-rolled into strip 3.0 mm (0.12 in) thick, descaled, annealed and cold rolled to 0.25 mm (0.010 in) with one or two intermediate anneals (at 1.14 mm (0.045 in) in both cases and at 0.3 mm (0.012 in) also in the latter case) to obtain a hard and half-hard temper respectively. Properties observed in the half-hard condition were as follows:

VPN Hardness, 200
Ultimate tensile strength, 550 MN/m² (81000 lbf/in²)
Elongation, 7%

Properties measured on annealed strip were as follows:

VPN Hardness, 120
Ultimate tensile strength, 400 MN/m² (58000 lbf/in²)
Elongation 30%
Expansion coefficient, 20—450°C, 11.4×10^{-6} per °C
Resistivity 0.57 $\mu\Omega$m.

A sample of half-hard material 0.89 mm (0.035 in) wide, cut transverse to the rolling direction, was subjected to a bending test using a load of 8.9 N (2 lbf). Various samples withstood from 6 to 8 bending cycles, which compares favourably with the current nickel bearing alloys.

The half-hard strip was stamped to form a strip of lead frames using conventional

tooling, and the strip was silver-plated using the following procedure:

1. Degrease by immersion for 1 minute in trichloroethylene at ambient temperature, wipe dry with paper tissue.

2. Etch by immersion for 1 minute in a solution comprising 1 volume 40% hydrofluoric acid in 10 volumes of water, at ambient temperature.

3. Rinse with distilled water at ambient temperature.

4. Cathodic clean for 1 minute at 1 kA/m² in an alkaline solution of 12.5 g/l sodium carbonate and 25 g/l trisodium phosphate, at ambient temperature.

5. Rinse with distilled water at ambient temperature.

6. Anodic clean for 1 minute at 1 kA/m² in an alkaline cyanide bath comprising 14 g/l sodium cyanide and 60 g/l sodium hydroxide at ambient temperature.

7. Rinse in distilled water at ambient temperature.

8. Immerse for 1 minute in a solution comprising equal volumes of hydrochloric acid (specific gravity 1.18) and water, at ambient temperature.

9. Rinse with de-ionised water at ambient temperature.

10. Strike coat with gold by passing a current of 80 A/m² in a proprietary gold strike solution, reference no. 3606, obtainable from Engelhard Industries Ltd., Chemical Division, Valley Road, Cinderford, Gloucestershire, Great Britain and from Engelhard Minerals and Chemicals Corp., 430 Mountain Avenue, Murray Hill, New Jersey 07974 USA. This is an aqueous solution containing about 14 g/l of gold as gold potassium cyanide ($KAu(CN)_2$ together with diammonium hydrogen orthophosphate and potassium dihydrogen orthophosphate, and operates at a pH in the range 5.2—5.8. For the present purpose, operation at ambient temperature is satisfactory, and there is no need to heat to around 70°C as advised by the manufacturer. This applies approximately 0.2 m of gold to the lead frame strip.

11. Rinse with distilled water at ambient temperature.

12. Silver plate by passing 1 kA/m² for 1 minute at ambient temperature in the proprietary bath known as the Lea-Ronal 3K system, obtainable from Lea-Ronal (UK) Ltd. Ashwood Dale Laboratories, Buxton, Derbyshire SK17 9TA and from Lea-Ronal Inc., Freeport, New York, USA. This solution comprises 36 g/l of silver as cyanide (though a higher silver content can be used if a high current density is desired) 112 g/l of potassium cyanide, 15 g/l of potassium carbonate, 5 ml/l of a wetting agent known as "Silver Glo TY" and 20 ml/l of an organic brightener known as "Silver Glo 3K". These proprietary additives are available separately for the same source, as they are required for make-up purposes (approximately 8 ml of wetting agent and 30 ml brightener being added per hundred grams of silver deposited).

After plating the strip of lead frames was rinsed and thoroughly dried. Sound adhesion of the plating was verified by heating a sample rapidly to 485°C and holding at this temperature for 2 minutes; no blistering was observed in this test.

The individual lead frames were now separated from the strip and each was bent, in the usual way, into a channel shape to provide for more convenient external connections. A silicon semiconductor chip was conventionally prepared and attached to the support member of the lead frame by a conventional eutectic alloy bonding technique. Electrical connections and encapsulation in resin also followed the conventional techniques of the industry, and finally the bridging members were cut away to provide a functional semiconductor device.

Example 2

The procedure was exactly as in Example 1 but the alloy consisted of 11.7% chromium, 7.6% cobalt, 0.29% manganese, 0.011% carbon, less than 0.05% silicon, 0.003% sulphur (impurity), balance iron. Properties of the annealed strip were as follows:

VPN Hardness 185
Ultimate tensile strength, 620 Mn/m² (90000 lbf/in²)
Elongation, 12%
Thermal Expansion coefficient (20—450°C), 11.1×10^{-6} per °C
Resistivity 0.62 $\mu\Omega$m.

Example 3

The procedure was again substantially the same, using an alloy comprising 12% chromium, 4% vanadium, 0.3% manganese, 0.008% carbon, less than 0.05% silicon, 0.005% sulphur (impurity), balance iron. Properties of the annealed strip were as follows:

VPN Hardness, 150
Ultimate tensile strength, 380 Mn/m² (55000 lbf/in²)
Elongation, 30%
Thermal Expansion coefficient (20—450°C), 11.1×10^{-6} per °C
Resistivity 0.47 $\mu\Omega$m

Examples of other suitable alloys, some of which are known and commercially available, include the following:

Example 4

12% Cr, 4% Co. balance Fe. Temperature coefficient 11.5×10^{-6} per °C.

Example 5

12% Cr, 8% Ct, balance Fe. Temperature coefficient 11.5×10^{-6} per °C.

Example 6

12% Cr, 4% V, balance Fe. Temperature coefficient 11.0×10^{-6} per °C.

This alloy has better mechanical properties than Examples 4—5 and a less critical annealing temperature range.

Examples 4—6 are minor variations for Examples 1—3 respectively.

Example 7

12% Cr, balance Fe. Temperature coefficient 12×10^{-6} per °C.

Example 8

12% Cr, 0.5% Mo, 0.35% V, 0.7 Mn, 0.1% C, 0.3% Si, 1.8% Ni, balance Fe.

Example 9

13% Cr, 1% Mo/, 0.25% V, 0.8% Mn, 0.23% C* 0.4% Si, 0.75 Ni, 1% W, balance Fe.

Example 10

11w- Cr, 0.6% Mo, 0.15% V, 1% Mn, 0.1% C, 0.5% Si, 0.8% Nb, balance Fe.

Example 11

12% Cr, 1% Mo, 3% V, 0.5w% Mn, 0.25% C, 0.5% Si, 0.5% Ni, balance Fe.

Example 12

13% Cr, 0.5% Mo, 0.5% Mn, 0.12% C, 0.3% Si, 0.5% Al, balance Fe.

Example 13

13.5% Cr, 0.35% Mo, 0.17% C, 0.5% Si, 1.0% Cu, balance Fe.

WHAT WE CLAIM IS:—

1. A silicon semiconductor device comprising a chip of silicon and leads made from an alloy with a thermal expansion coefficient up to 13×10^{-6} per °C and comprising

Chromium	8—14%
Molybdenum	0—1.5%
Cobalt	0—8%
Vanadium	0—6%
Manganese	0—1.5%
Carbon	0—0.3%
Silicon	0—1%
Niobium	0—2%
Nickel	0—2%
Tungsten	0—1%
Copper	0—1.5%
Aluminium	0—4%
Iron and impurities	balance,

the chip and part of each of the leads being encapsulated.

2. A semiconductor device as claimed in Claim 1 wherein the alloy includes at least one of the metals molybdenum, cobalt, vanadium and manganese.

3. A semiconductor device as claimed in Claim 1 or Claim 2 wherein the alloy contains less than 2.5% in all of carbon, silicon, niobium, nickel, tungsten, copper, aluminium and impurities.

4. A semiconductor device as claimed in Claim 1 or Claim 2 wherein the alloy contains less than 0.75% in all of carbon, silicon, niobium, nickel, tungsten, copper, aluminium and impurities.

5. A semiconductor device as claimed in Claim 1 or Claim 2 wherein the alloy consists substantially of 11.8% chromium, 4.3% cobalt, 0.26% manganese, 0.016% carbon less than 0.05% silicon, balance iron and impurities.

6. A semiconductor device as claimed in Claim 1 or Claim 2 wherein the alloy consists substantially of 11.7% chromium, 7.6% cobalt, 0.29% manganese, 0.011% carbon, less than 0.05% silicon, balance iron and impurities.

7. A semiconductor device as claimed in Claim 1 or Claim 2 wherein the alloy consists substantially of 12% chromium, 4% vanadium, 0.3% ma/nganese, 0.008% carbon, less than 0.05% silicon, balance iron and impurities.

8. A semiconductor device as claimed in Claim 1 or Claim 2 in which the alloy has substantially the composition specified in any one of Examples 4—13.

9. A semiconductor device as claimed in any one of the preceding claims wherein said leads are plated with a metallic substance of good corrosion resistance and electrical conductivity.

10. A semiconductor device as claimed in any one of the preceding claims wherein the chip and the said parts of the leads are encapsulated in plastics material.

11. A semiconductor device substantially as described with particular reference to Example 1.

12. A semiconductor device substantially as described with particular reference to

Example 4

12% Cr, 4% Co. balance Fe. Temperature coefficient 11.5×10^{-6} per °C.

Example 5

12% Cr, 8% Ct, balance Fe. Temperature coefficient 11.5×10^{-6} per °C.

Example 6

12% Cr, 4% V, balance Fe. Temperature coefficient 11.0×10^{-6} per °C.

This alloy has better mechanical properties than Examples 4—5 and a less critical annealing temperature range.

Examples 4—6 are minor variations for Examples 1—3 respectively.

Example 7

12% Cr, balance Fe. Temperature coefficient 12×10^{-6} per °C.

Example 8

12% Cr, 0.5% Mo, 0.35% V, 0.7 Mn, 0.1% C, 0.3% Si, 1.8% Ni, balance Fe.

Example 9

13% Cr, 1% Mo/, 0.25% V, 0.8% Mn, 0.23% C* 0.4% Si, 0.75 Ni, 1% W, balance Fe.

Example 10

11w- Cr, 0.6% Mo, 0.15% V, 1% Mn, 0.1% C, 0.5% Si, 0.8% Nb, balance Fe.

Example 11

12% Cr, 1% Mo, 3% V, 0.5w% Mn, 0.25% C, 0.5% Si, 0.5% Ni, balance Fe.

Example 12

13% Cr, 0.5% Mo, 0.5% Mn, 0.12% C, 0.3% Si, 0.5% Al, balance Fe.

Example 13

13.5% Cr, 0.35% Mo, 0.17% C, 0.5% Si, 1.0% Cu, balance Fe.

WHAT WE CLAIM IS:—

1. A silicon semiconductor device comprising a chip of silicon and leads made from an alloy with a thermal expansion coefficient up to 13×10^{-6} per °C and comprising

Chromium	8—14%
Molybdenum	0—1.5%
Cobalt	0—8%
Vanadium	0—6%
Manganese	0—1.5%
Carbon	0—0.3%
Silicon	0—1%
Niobium	0—2%
Nickel	0—2%
Tungsten	0—1%
Copper	0—1.5%
Aluminium	0—4%
Iron and impurities	balance,

the chip and part of each of the leads being encapsulated.

2. A semiconductor device as claimed in Claim 1 wherein the alloy includes at least one of the metals molybdenum, cobalt, vanadium and manganese.

3. A semiconductor device as claimed in Claim 1 or Claim 2 wherein the alloy contains less than 2.5% in all of carbon, silicon, niobium, nickel, tungsten, copper, aluminium and impurities.

4. A semiconductor device as claimed in Claim 1 or Claim 2 wherein the alloy contains less than 0.75% in all of carbon, silicon, niobium, nickel, tungsten, copper, aluminium and impurities.

5. A semiconductor device as claimed in Claim 1 or Claim 2 wherein the alloy consists substantially of 11.8% chromium, 4.3% cobalt, 0.26% manganese, 0.016% carbon less than 0.05% silicon, balance iron and impurities.

6. A semiconductor device as claimed in Claim 1 or Claim 2 wherein the alloy consists substantially of 11.7% chromium, 7.6% cobalt, 0.29% manganese, 0.011% carbon, less than 0.05% silicon, balance iron and impurities.

7. A semiconductor device as claimed in Claim 1 or Claim 2 wherein the alloy consists substantially of 12% chromium, 4% vanadium, 0.3% ma/nganese, 0.008% carbon, less than 0.05% silicon, balance iron and impurities.

8. A semiconductor device as claimed in Claim 1 or Claim 2 in which the alloy has substantially the composition specified in any one of Examples 4—13.

9. A semiconductor device as claimed in any one of the preceding claims wherein said leads are plated with a metallic substance of good corrosion resistance and electrical conductivity.

10. A semiconductor device as claimed in any one of the preceding claims wherein the chip and the said parts of the leads are encapsulated in plastics material.

11. A semiconductor device substantially as described with particular reference to Example 1.

12. A semiconductor device substantially as described with particular reference to

* C L M S *

any one of Examples 2—13 and to those parts of Example 1 that are consistent with it.

M. J. POOLE,
Chartered Patent Agent,
Agent for the Applicants.

Printed for Her Majesty's Stationery Office, by the Courier Press, Leamington Spa, 1979
Published by The Patent Office, 25 Southampton Buildings, London, WC2A 1AY, from which copies may be obtained.

* C L M S *