ABSTRACT

A NOVEL METHOD OF MAKING SELF-ALIGNED SILICIDE NARROW GATE ELECTRODES FOR FIELD EFFECT TRANSISTORS HAVING LOW SHEET RESISTANCE

A method for making low sheet resistance sub-quarter-micrometer gate electrode lengths on field effect transistors has been achieved. The method involves patterning gate electrodes on a silicon substrate from a conductively doped polysilicon layer having a silicon nitride layer on the surface. After forming the FET lightly doped drains (LDD), the sidewall spacers, and the heavily doped source/drain contact regions with titanium contacts, an insulating layer is chemically/mechanically polished back to the silicon nitride or silicon oxynitride on the gate electrode layer to form a planar self-aligning mask. A pre-amorphizing implantation is carried out, and a titanium silicide is selectively formed on the gate electrodes resulting in small grain sizes and much reduced sheet resistance. The self-aligned mask prevents ion implant damage to the shallow source/drain regions adjacent to the FET gate electrodes. A second embodiment uses the self-aligned mask to form selectively a cobalt silicide on the polysilicon gate electrodes for low sheet resistance, while preventing the cobalt silicide from reacting with the adjacent titanium silicide source/drain regions.

(FIGURE 1 IS SUGGESTED FOR PUBLICATION)