

Description

Background to the Invention

The present invention relates to a PLL (phase locked loop) frequency synthesizer, and more particularly to a frequency synthesizer for use in a battery-powered apparatus, such as a portable radio transmitter/receiver.

An embodiment employing a PLL frequency synthesizer having a charge pump circuit will be described in detail later. A charge pump circuit is used for electrically charging and discharging a loop filter which supplies a control voltage to a voltage-controlled oscillator (VCO).

The power voltage V_{cc} for the charge pump circuit is the output voltage of a voltage regulator, which is +5 V for instance in a battery-powered portable radio transmitter/receiver. For this reason, the control voltage supplied to the VCO is normally limited to within the range of 0 to 5 V, resulting in the dynamic range of the oscillation frequency being correspondingly limited. Further, with a low control voltage, there is the problem that the Q value of the variable capacitance diode of the VCO is low, resulting in a deterioration of the carrier-to-noise (C/N) ratio of the VCO output. Moreover, the loop filter would take a long time to be charged or discharged, and the frequency switching of the synthesizer would also be slow.

In WO-A-82/03477, there is described a frequency synthesized transceiver which employs a phase locked loop in which a divided down reference frequency from a stable reference oscillator is compared to a sub-multiple of voltage controlled oscillator frequency. There is no provision for enhancing the control voltage supplied to the voltage controlled oscillator.

An object of the present invention according to Claim 1, therefore, is to provide a PLL frequency synthesizer whose VCO has a broad dynamic range of oscillation frequency.

Another object of the invention is to provide a PLL frequency synthesizer whose variable capacitance diode has an increased Q value and in which the VCO output is improved in C/N ratio.

Still another object of the invention is to provide a PLL frequency synthesizer whose switching speed is increased.

In an embodiment to be described, a frequency synthesizer comprises a voltage-controlled oscillator (VCO) for generating an oscillation of a frequency varying responsive to a control voltage; a variable frequency divider for dividing the output frequency of the VCO in a ratio according to a control signal; a reference oscillator for supplying a reference signal having a predetermined frequency; a fixed frequency divider for dividing the frequency of the reference signal in a fixed ratio; a phase comparator for comparing the phases of the outputs of the fixed frequency divider and variable frequency divider to provide a control pulse corresponding to a phase difference between these outputs; a charge pump having a power supply terminal for generating a

charge/discharge voltage in response to the control pulse; a loop filter including a first capacitor supplied with the charge/discharge voltage for supplying to the VCO as the control voltage a voltage corresponding to said charge/discharge voltage; and a power supply circuit for generating a D.C. voltage by boosting the voltage of the output of said fixed frequency divider and supplying this D.C. voltage to the charge pump as power voltage.

Brief Description of the Drawings

The above and other objects, features and advantages of the present invention will be more apparent from the detailed description hereunder taken in conjunction with the accompanying drawings, wherein:

FIG. 1 is a block diagram illustrating a conventional PLL frequency synthesizer;

FIG. 2 is a block diagram illustrating a preferred embodiment of a PLL frequency synthesizer according to the invention;

FIG. 3 is a graph showing the relationship between the reverse voltage and the capacitance of a variable capacitance diode in a VCO;

FIG. 4 is a graph showing the relationship between the control voltage and the oscillation frequency of VCO; and

FIG. 5 is a diagram showing the rise time characteristic of the control voltage supplied to VCO.

Detailed Description of the Invention

The PLL frequency synthesizer illustrated in FIG. 1 has a voltage-controlled oscillator (VCO) 1, which varies the oscillation frequency according to a control voltage. The output of VCO 1 is supplied to one input terminal 301 of a phase comparator 3 through a variable frequency divider 2 which divides the input frequency in accordance with a control signal C_D . To the other input terminal 302 of the phase comparator 3 is supplied a signal resulting from the frequency division of the output of a quartz reference oscillator 5 by a fixed frequency divider 4. The phase comparator 3 detects a phase difference between the signals supplied to its input terminals 301 and 302, and feeds a charge pump 6 with a pulse train corresponding to the phase difference.

The polarity of the phase difference corresponds to the advance or delay of the output of VCO 1 with respect to the output of the reference oscillator 5. Based on the polarity, the pulse train appears at one of output terminals 303 and 304, which are connected to the charge pump 6 comprising transistors 61 and 62, resistors 63-68 and diodes 69 and 70. If the pulse train emerges at the terminal 303, a transistor 61 is supplied with a bias voltage through the resistors 65 and 67, and thereby actuated. A capacitor 72 of a loop filter 7 is charged by a power voltage V_{cc} through the resistor 63, the transistor 61 and a resistor 71. The charged voltage is applied to a control terminal 101 of VCO 1 as a control voltage V_{co} . If the pulse

train appears at the terminal 304, the transistor 62 is supplied with a bias voltage through resistors 68 and 66, and thereby actuated. The charged capacitor 72 is discharged through the transistor 62 and a resistor 64. The discharged voltage also becomes the control voltage V_{co} and is applied to the control terminal 101 of VCO 1. When VCO 1 reaches an oscillation frequency corresponding to the control voltage V_{co} applied to the control terminal 101, a phase locked loop (PLL) is locked.

As stated above, the power voltage V_{cc} supplied to the charge pump 6 is the output voltage of a voltage regulator, which is +5 V in a portable radio transmitter/receiver or the like. For this reason, in the frequency synthesizer of the prior art, the variable range of the control voltage V_{co} to be applied to the terminal 101 of VCO 1 is restricted to between zero volts and V_{cc} , i.e., 5 volts. FIG. 3 shows the relationship between the reverse voltage V_R and the capacitance C of a variable capacitance diode connected to the control terminal 101 of VCO 1. In the synthesizer of FIG. 1, the variance of the capacitance C is narrowly limited because the reverse voltage V_R can vary only up to V_{cc} . FIG. 4 shows the relationship between the control voltage V_{co} and the oscillation frequency f of VCO 1. In the conventional synthesizer, the oscillation frequency f varies only within range A. Further, FIG. 5 shows the rise time of the control voltage V_{co} , which in the prior art synthesizer takes a time t_2 to reach a prescribed voltage ΔV as curve 201 indicates.

In FIG. 2, the same symbols represent the same or equivalent constituents as in FIG. 1. The frequency synthesizer of FIG. 2 differs from that of FIG. 1 in that the D.C. voltage V_H of a power supply circuit 10 is supplied as power voltage for a charge pump 16. The power supply circuit 10 comprises a booster circuit 8 having a transformer 81 for boosting the output of the frequency divider 4, and a rectifier circuit 9 for rectifying the output voltage of the booster circuit 8 into a D.C. voltage. The rectifier circuit 9 includes bridge diodes 91 to 94 and a capacitor 95. The capacitance of the capacitor 95 is set greater than that of the capacitor 72 in the loop filter 7.

The frequency division output of the frequency divider 4, after being boosted by the transformer 81, is rectified by the bridge diodes 91 to 94, smoothed and held by the capacitor 95 and used as power to drive the charge pump 16. The power supplied to the charge pump 16 has to charge the capacitor 72 of the loop filter 7. The capacitor 72 can be charged by the capacitor 95 because the latter has a greater capacitance than the former.

Since the output voltage V_H of the power supply circuit 10 is substantially higher than the power voltage V_{cc} , a buffer transistor 161 is inserted between one end of a resistor 67 and the base of the transistor 61, both in the charge pump 16, to prevent the phase comparator 3 from destruction. To the base of the transistor 161 is applied the power voltage V_{cc} , so that no higher voltage than

the balance of subtraction of the base-emitter voltage (V_{BE}) of the transistor 161 from V_{cc} may be applied to the phase comparator 3.

When the PLL is locked, the control voltage V_{co} supplied to VCO 1 becomes constant, and only a little current flows to the charge pump 16. As a result, the insertion of the capacitor 95 enables the output current value of the transformer 81 to be made extremely small and, therefore, the transformer 81 can be miniaturized. Since the output voltage V_H of the power supply circuit 10 is higher than the power voltage V_{cc} , the capacitance C of the variable capacitance diode can be varied in a broader range, as shown in FIG. 3. Therefore, the Q value of the variable capacitance diode is increased, and the C/N ratio of the VCO 1 output is improved. Further, as shown in FIG. 4, the variable range of the oscillation frequency f of VCO 1 is extended to B. Moreover, the switching speed is so increased that, as indicated by curve 202 in FIG. 5, the prescribed voltage ΔV can be attained in only time t_1 , shorter than time t_2 required by a conventional frequency synthesizer.

Claims

1. A PLL frequency synthesizer including a voltage controlled oscillator (VCO) (1) for generating an oscillation at a frequency which varies in response to a control voltage, a first frequency divider (2) for dividing the output frequency on the VCO (1), a reference oscillator (5) for supplying a reference signal having a predetermined frequency, a second frequency divider (4) for dividing the frequency of the reference signal, and a phase comparator (3) for comparing the phases of the outputs of the first and second frequency dividers (2) (4) to provide a control pulse corresponding to a phase difference between these outputs, the first frequency divider (2) being a variable frequency divider for dividing the output frequency of the VCO (1) in a ratio according to a control signal, and the second frequency divider (4) being a fixed ratio divider, characterised in that there is provided a charge pump (16) having a power supply terminal for generating a charge/discharge voltage in response to the control pulse, a loop filter (7) including a first capacitor (72), to which the charge/discharge voltage is applied, for supplying to the VCO a control voltage corresponding to the charge/discharge voltage, and a power supply circuit (10) for producing a DC voltage by boosting the output of the second fixed frequency divider (4) to supply the D.C. voltage to the power supply terminal.

2. A PLL frequency synthesizer as claimed in Claim 1, characterised in that the power supply circuit (10) includes a booster circuit (8) for boosting the output of the second fixed frequency divider (4) and a rectifier and smoothing circuit (9) for rectifying the output of the booster circuit (8) and smoothing the rectified output.

3. A PLL frequency synthesizer as claimed in Claim 2, characterised in that the booster circuit



train appears at the terminal 304, the transistor 62 is supplied with a bias voltage through resistors 68 and 66, and thereby actuated. The charged capacitor 72 is discharged through the transistor 62 and a resistor 64. The discharged voltage also becomes the control voltage V_{co} and is applied to the control terminal 101 of VCO 1. When VCO 1 reaches an oscillation frequency corresponding to the control voltage V_{co} applied to the control terminal 101, a phase locked loop (PLL) is locked.

As stated above, the power voltage V_{cc} supplied to the charge pump 6 is the output voltage of a voltage regulator, which is +5 V in a portable radio transmitter/receiver or the like. For this reason, in the frequency synthesizer of the prior art, the variable range of the control voltage V_{co} to be applied to the terminal 101 of VCO 1 is restricted to between zero volts and V_{cc} , i.e., 5 volts. FIG. 3 shows the relationship between the reverse voltage V_R and the capacitance C of a variable capacitance diode connected to the control terminal 101 of VCO 1. In the synthesizer of FIG. 1, the variance of the capacitance C is narrowly limited because the reverse voltage V_R can vary only up to V_{cc} . FIG. 4 shows the relationship between the control voltage V_{co} and the oscillation frequency f of VCO 1. In the conventional synthesizer, the oscillation frequency f varies only within range A. Further, FIG. 5 shows the rise time of the control voltage V_{co} , which in the prior art synthesizer takes a time t_2 to reach a prescribed voltage ΔV as curve 201 indicates.

In FIG. 2, the same symbols represent the same or equivalent constituents as in FIG. 1. The frequency synthesizer of FIG. 2 differs from that of FIG. 1 in that the D.C. voltage V_H of a power supply circuit 10 is supplied as power voltage for a charge pump 16. The power supply circuit 10 comprises a booster circuit 8 having a transformer 81 for boosting the output of the frequency divider 4, and a rectifier circuit 9 for rectifying the output voltage of the booster circuit 8 into a D.C. voltage. The rectifier circuit 9 includes bridge diodes 91 to 94 and a capacitor 95. The capacitance of the capacitor 95 is set greater than that of the capacitor 72 in the loop filter 7.

The frequency division output of the frequency divider 4, after being boosted by the transformer 81, is rectified by the bridge diodes 91 to 94, smoothed and held by the capacitor 95 and used as power to drive the charge pump 16. The power supplied to the charge pump 16 has to charge the capacitor 72 of the loop filter 7. The capacitor 72 can be charged by the capacitor 95 because the latter has a greater capacitance than the former.

Since the output voltage V_H of the power supply circuit 10 is substantially higher than the power voltage V_{cc} , a buffer transistor 161 is inserted between one end of a resistor 67 and the base of the transistor 61, both in the charge pump 16, to prevent the phase comparator 3 from destruction. To the base of the transistor 161 is applied the power voltage V_{cc} , so that no higher voltage than

the balance of subtraction of the base-emitter voltage (V_{BE}) of the transistor 161 from V_{cc} may be applied to the phase comparator 3.

When the PLL is locked, the control voltage V_{co} supplied to VCO 1 becomes constant, and only a little current flows to the charge pump 16. As a result, the insertion of the capacitor 95 enables the output current value of the transformer 81 to be made extremely small and, therefore, the transformer 81 can be miniaturized. Since the output voltage V_H of the power supply circuit 10 is higher than the power voltage V_{cc} , the capacitance C of the variable capacitance diode can be varied in a broader range, as shown in FIG. 3. Therefore, the Q value of the variable capacitance diode is increased, and the C/N ratio of the VCO 1 output is improved. Further, as shown in FIG. 4, the variable range of the oscillation frequency f of VCO 1 is extended to B. Moreover, the switching speed is so increased that, as indicated by curve 202 in FIG. 5, the prescribed voltage ΔV can be attained in only time t_1 , shorter than time t_2 required by a conventional frequency synthesizer.

Claims

1. A PLL frequency synthesizer including a voltage controlled oscillator (VCO) (1) for generating an oscillation at a frequency which varies in response to a control voltage, a first frequency divider (2) for dividing the output frequency on the VCO (1), a reference oscillator (5) for supplying a reference signal having a predetermined frequency, a second frequency divider (4) for dividing the frequency of the reference signal, and a phase comparator (3) for comparing the phases of the outputs of the first and second frequency dividers (2) (4) to provide a control pulse corresponding to a phase difference between these outputs, the first frequency divider (2) being a variable frequency divider for dividing the output frequency of the VCO (1) in a ratio according to a control signal, and the second frequency divider (4) being a fixed ratio divider, characterised in that there is provided a charge pump (16) having a power supply terminal for generating a charge/discharge voltage in response to the control pulse, a loop filter (7) including a first capacitor (72), to which the charge/discharge voltage is applied, for supplying to the VCO a control voltage corresponding to the charge/discharge voltage, and a power supply circuit (10) for producing a DC voltage by boosting the output of the second fixed frequency divider (4) to supply the D.C. voltage to the power supply terminal.

2. A PLL frequency synthesizer as claimed in Claim 1, characterised in that the power supply circuit (10) includes a booster circuit (8) for boosting the output of the second fixed frequency divider (4) and a rectifier and smoothing circuit (9) for rectifying the output of the booster circuit (8) and smoothing the rectified output.

3. A PLL frequency synthesizer as claimed in Claim 2, characterised in that the booster circuit



(8) includes a transformer (81) of which the primary side is coupled to the output of the fixed frequency divider (4) and the secondary side is coupled to the output of the booster circuit (8), and in that the rectifier and smoothing circuit (9) includes bridge diodes (91 to 94) coupled to the secondary side of the transformer (81) and a second capacitor (95) connected to the outputs of the bridge diodes (91 to 94) and to the output of the rectifier circuit, the capacitance of the second capacitor (95) being greater than that of the first capacitor (72).

4. A PLL frequency synthesizer as claimed in Claim 1, characterised in that the phase comparator (3) supplies first and second outputs each according to the polarity of the phase difference, in that the charge pump (16) includes a first transistor (61) whose base, collector and emitter are coupled to the first output of the phase comparator (3); the input of the loop filter (7) and the output of the power supply circuit, respectively, and a second transistor (62) whose base, collector and emitter are coupled to the second output of said phase comparator (3), the input of the loop filter (7) and the ground, respectively, and in that the charge pump (16) further includes a third transistor (161) whose emitter and collector are connected between the first output of the phase comparator (3) and the base of the first transistor (61) and whose base is connected to a power voltage.

5. A PLL frequency synthesizer as claimed in Claim 5, characterised in that the power voltage is lower than the breakdown voltage of the phase comparator (3).

Patentansprüche

1. Frequenzsynthesator mit phasenverriegelter Schleife mit einem spannungsgesteuerten Oszillator (VCO) (1) zum Erzeugen einer Schwingung mit einer Frequenz, die sich in Abhängigkeit von einer Steuerspannung ändert, einem ersten Frequenzteiler (2) zum Teilen der Ausgangsfrequenz am VCO (1), einem Referenzoszillator (5) zum Liefern eines Referenzsignals mit einer vorbestimmten Frequenz, einem zweiten Frequenzteiler (4) zum Teilen der Frequenz des Referenzsignals, und einem Phasenkomparator (3) zum Vergleichen der Phasen der Ausgänge des ersten und zweiten Frequenzteilers (2, 4), um einen Kontrollimpuls entsprechend einer phasendifferenz zwischen diesen Ausgängen zur Verfügung zu stellen, wobei der erste Frequenzteiler (2) ein variabler Frequenzteiler ist, um die Ausgangsfrequenz des VCO (1) in einem Verhältnis entsprechend einem Steuersignal zu teilen, und der zweite Frequenzteiler (4) ein Festverhältnis-teiler ist, gekennzeichnet durch eine Ladungspumpe (16) mit einem Ausgangsanschluß zum Erzeugen einer Ladungs/Entladungsspannung entsprechend dem Steuerimpuls, einem Schleifenfilter (7) mit einem ersten Kondensator (72), an dem die Ladungs/Entladungsspannung anliegt, um dem VCO eine Steuerspannung entsprechend der

Ladungs/Entladungsspannung zu liefern, und einem Leistungsschaltkreis (10) zum Erzeugen einer Gleichspannung durch Erhöhen des Ausgangs des zweiten Festfrequenzteilers (4), um die Gleichspannung zum Ausgangsanschluß zu liefern.

2. Frequenzsynthesator mit phasenverriegelter Schleife nach Anspruch 1, dadurch gekennzeichnet, daß der Leistungsschaltkreis (10) aufweist: einen Spannungserhöhungsschaltkreis (8) zum Erhöhen des Ausgangs des zweiten Festverhältnisfrequenzteilers (4) und einen Gleichrichtungs- und Glättungsschaltkreis (9) zum Gleichrichten des Ausgangs des Spannungserhöhungsschaltkreises (8) und Glätten des gleichgerichteten Ausgangs.

3. Frequenzsynthesator mit phasenverriegelter Schleife nach Anspruch 2, dadurch gekennzeichnet, daß der Spannungserhöhungsschaltkreis (8) einen Transformator (81) aufweist, dessen Primärseite mit dem Ausgang des Festverhältnisfrequenzteilers (4) und dessen Sekundärseite mit dem Ausgang des Spannungserhöhungsschaltkreises (8) gekoppelt ist, und daß der Gleichrichtungs- und Glättungsschaltkreis (9) Brückendioden (91 bis 94), die mit der Sekundärseite des Transformators (81) gekoppelt sind, und einen zweiten Kondensator (95) aufweist, der mit den Ausgängen der Brückendioden (91 bis 94) und mit dem Ausgang des Gleichrichtungsschaltkreises verbunden ist, wobei die Kapazität des zweiten Kondensators (95) größer als die des ersten Kondensators (72) ist.

4. Frequenzsynthesator mit phasenverriegelter Schleife nach Anspruch 1, dadurch gekennzeichnet, daß der Phasenkomparator (3) erste und zweite Ausgänge liefert, wobei jeder der Polarität der Phasendifferenz entspricht, daß die Ladungspumpe (16) einen ersten Transistor (61), dessen Basis, Kollektor und Emitter mit dem ersten Ausgang des Phasenkomparators (3), dem Eingang des Schleifenfilters (7) bzw. dem Ausgang des Stromversorgungsschaltkreises gekoppelt sind, und einen zweiten Transistor (62) aufweist, dessen Basis, Kollektor und Emitter mit dem zweiten Ausgang des Phasenkomparators (3), dem Eingang des Schleifenfilters (7) bzw. der Erde gekoppelt sind, und daß die Ladungspumpe (16) einen dritten Transistor (161) aufweist, dessen Emitter und Kollektor zwischen den ersten Ausgang des Phasenkomparators (3) und der Basis des ersten Transistors (61) geschaltet sind und an dessen Basis eine Arbeitsspannung liegt.

5. Frequenzsynthesator mit phasenverriegelter Schleife nach Anspruch 4, dadurch gekennzeichnet, daß die Arbeitsspannung niedriger als die Durchbruchsspannung des Phasenkomparators (3) ist.

Revendications

1. Synthétiseur de fréquence à boucle verrouillée en phase, comportant un oscillateur piloté par tension (VCO) (1) pour produire une oscillation à une fréquence qui varie en réponse à une tension



de commande, un premier diviseur de fréquence (2) pour diviser la fréquence de sortie du VCO (1), un oscillateur de référence (5) pour fournir un signal de référence ayant une fréquence prédéterminée, un second diviseur de fréquence (4) pour diviser la fréquence du signal de référence, et un comparateur de phase (3) pour comparer les phases des sorties des premier et second diviseurs de fréquence (2) (4) pour fournir une impulsion de commande correspondant à une différence de phase entre ces sorties, le premier diviseur de fréquence (2) étant un diviseur de fréquence variable afin de diviser la fréquence de sortie du VCO (1) dans un rapport en conformité avec un signal de commande, et le second diviseur de fréquence (4) étant un diviseur à rapport fixe, caractérisé en ce qu'on fournit une pompe de charge (16) ayant une borne d'alimentation pour produire une tension de charge/décharge en réponse à l'impulsion de commande, un filtre en boucle (7) comportant un premier condensateur (72), auquel est appliquée la tension de charge/décharge, afin de fournir au VCO une tension de commande correspondant à la tension de charge/décharge, et un circuit d'alimentation (10) pour produire une tension à courant continu en amplifiant la sortie du second diviseur de fréquence fixe (4) pour fournir la tension à courant continu à la borne d'alimentation.

2. Synthétiseur de fréquence à boucle verrouillée en phase selon la revendication 1, caractérisé en ce que le circuit d'alimentation (10) comprend un circuit amplificateur (8) pour amplifier la sortie du second diviseur de fréquence fixe (4) et un circuit redresseur et écrêteur (9) pour redresser la sortie du circuit d'amplification (8) et écrêter la sortie redressée.

3. Synthétiseur de fréquence à boucle verrouil-

lée en phase selon la revendication 2, caractérisé en ce que le circuit amplificateur (8) comporte un transformateur (81) dont le côté primaire est relié à la sortie du diviseur de fréquence fixe (4) et le côté secondaire est accouplé à la sortie du circuit amplificateur (8), et en ce que le circuit redresseur et écrêteur (9) comporte des diodes en pont (91 à 94) reliées au côté secondaire du transformateur (81) et un second condensateur (95) connecté aux sorties des diodes en pont (91 à 94) et à la sortie du circuit redresseur, la capacité du second condensateur (95) étant supérieure à celle du premier condensateur (72).

4. Synthétiseur de fréquence à boucle verrouillée en phase selon la revendication 1, caractérisé en ce que le comparateur de phase (3) fournit les première et seconde sorties, chacune en conformité avec la polarité de la différence de phase, en ce que la pompe de charge (16) comporte un premier transistor (61) dont la base, le collecteur et l'émetteur sont reliés à la première sortie du comparateur de phase (3), à l'entrée du filtre en boucle (7) et à la sortie du circuit d'alimentation respectivement, et un second transistor (62) dont la base, le collecteur et l'émetteur sont accouplés à la seconde sortie du comparateur de phase (3), à l'entrée du filtre en boucle (7) et à la masse, respectivement, et en ce que la pompe de charge (16) comporte en outre un troisième transistor (161) dont l'émetteur et le collecteur sont montés entre la première sortie du comparateur de phase (3) et la base du premier transistor (61) et dont la base est reliée à une tension d'alimentation.

5. Synthétiseur de fréquence à boucle verrouillée en phase selon la revendication 4, caractérisé en ce que la tension d'alimentation est inférieure à la tension de claquage du comparateur de phase (3).