PARTITIONED THROUGH-LAYER VIA AND ASSOCIATED SYSTEMS AND METHODS

TECHNICAL FIELD

[0001] The present disclosure is related to metal vias, interconnects, and other types of patterned contacts formed on a substrate, such as a circuit board layer or a semiconductor wafer.

BACKGROUND

[0002] Many electronic systems include a circuit board having an arrangement of electronic components that are attached to the board and dedicated to performing specific electronic functions. For example, a personal computer includes a circuit board that has various types of memory for storing program instructions and a processor for executing the program instructions. In general, a circuit board typically includes a non-conductive layer that is laminated with one or more conductive metal layers. The metal layers include patterned contacts that attach to electrical components and patterned traces that route electrical signals between the patterned contacts.

[0003] As electronic systems become smaller and more compact, a large number of closely spaced electrical components are generally mounted to circuit boards. Inevitably, however, it becomes difficult to fit all of the necessary patterned contacts and traces between such closely spaced components. Many electronic systems accordingly use circuit boards that include layers of patterned traces located at multiple levels in the boards. Such multi-level circuit boards include metal vias routed through one or more layers and electrically coupled to one or more levels of the patterned traces. The metal vias can be difficult to locate because they need to avoid electrical contact with most of the patterned traces on a circuit board layer. If a via is not placed correctly, two or more individual traces can inadvertently be shorted together. Consequently, it can be difficult to design and manufacture a circuit board having stacked circuit board layers.

BRIEF DESCRIPTION OF THE DRAWINGS

[0004] Figure 1 is an isometric view of a circuit board substrate having a partitioned via configured in accordance with one embodiment of the disclosure.

[0005] Figures 2A and 2B are cross-sectional side views of the circuit board of Figure 1 taken along line 2A-2A and line 2B-2B, respectively.

[0006] Figure 3 is a cross-sectional side view of a dielectric layer having metal cladding layers attached at top and bottom sides.

[0007] Figure 4A is a cross-sectional side view of the dielectric layer of Figure 3 having a first hole that extends between the top and bottom sides.

[0008] Figure 4B is a top view of the dielectric layer of Figure 4A.

[0009] Figure 5 is a cross-sectional side view of the dielectric layer of Figure 4A having sidewalls of the first hole lined with a metal plating layer.

[0010] Figure 6A is a cross-sectional side view of the dielectric layer of Figure 5 having partitions cut into the first hole.

[0011] Figure 6B is a top view of the dielectric layer of Figure 6A.

[0012] Figures 7A and 7B are cross-sectional side views of the dielectric layer of Figure 6A having a via hole filled with a dielectric spacer material.

[0013] Figures 8A-8C are top views of embodiments of partitioned vias and partitioned lead lands.

[0014] Figure 9 is an isometric view of a circuit board layer having a partitioned via coupled to individual traces and sets of parallel traces.

[0015] Figure 10 is a cross-sectional side view of a stack of individual circuit board layers that includes individual partitioned vias.

[0016] Figure 11 is a schematic illustration of a system in which a partitioned via may be incorporated.

DETAILED DESCRIPTION

[0017] Various embodiments of partitioned vias, interconnects, and substrates that include such vias and interconnects are described below. The terms "via" and "interconnect" may encompass various types of metal structures that extend at least partially through a non-conductive layer and electrically couple together one or more metal contacts located at a surface of the non-conductive layer. Such metal contacts may be located on the non-conductive layer itself or at another layer that is above or below the non-conductive layer. The term "non-conductive layer" may encompass any of a variety of non-conductive materials (e.g., dielectric materials or semi-conductive materials), which may be included within a substrate. The term "substrate" can include a myriad of electronic and microelectronic structures (e.g., circuit boards or semiconductor wafers) that physically separate and electrically intercouple electronic or microelectronic components. Electronic and microelectronic components can include any of a wide variety of electrical devices (e.g., transistors, resistors, capacitors, etc.) or systems of such devices (e.g., a processor, a memory, etc.).

[0018] To avoid unnecessarily obscuring the description of the various embodiments, the detailed description describes embodiments of partitioned vias and interconnects in the context of circuit board substrates (e.g., a printed circuit board, an etched wiring board, or other type of non-conductive core layer that has been printed, laminated, or otherwise formed to have one or more surfaces of conductive leads, traces, or signal lines). However, alternative embodiments of substrates may comprise other types of semiconductor materials located within a semiconductor wafer (e.g., silicon, silicon dioxide, gallium arsenide, etc.). Likewise, alternative embodiments of vias include metal vias that are located within one or more passivation or inter-level dielectric layers of a microelectronic device. Such vias can also include through silicon vias (TSVs) for electrically intercoupling opposing sides of a silicon substrate. Other embodiments of vias, interconnects, and substrates in addition to or in lieu of the embodiments described in this section may have several additional features or may not include many of the features shown and described below with reference to Figures 1-11.

[0019] Turning now to the Figures, Figure 1 is an isometric view of an embodiment of a portion of a circuit board substrate 100 having a dielectric layer 102 and an embodiment of a

partitioned via 120. The dielectric layer 102 can have a top side 105, a bottom side 106, a via hole 108, and first and second interconnects 110-111 within the via hole 108. In many embodiments, the via hole 108 extends between the top and bottom sides 105-106 and includes a first sidewall section covered with a first metal wall plating 114 defining the first interconnect 110 and a second sidewall section covered with a second metal wall plating 115 defining the second interconnect 111. The first and second wall platings 114-115 can be formed from the same layer or "deposit" as explained in more detail below. The via hole 108 can also include first and second partitions 118-119 that bisect the via hole 108 and define a gap that electrically isolates the first wall plating 114 from the second wall plating 115. The first and second partitions 118-119 can have partition walls cut through a metal layer deposited along the sidewall and cut into the dielectric material at the sidewall. The via 120 can further include a dielectric plug 122 or spacer layer that fills the remainder of the via hole 108. The dielectric plug 122 can be attached to portions of the wall platings 114-115 and can also be attached to portions of the partitions 118-119. The dielectric plug 122, for example, can protect the via 120 during subsequent manufacturing (e.g., circuit board layer stacking) and can also provide electrical or mechanical isolation between the wall platings 114-115 and metal lead land portions (described below). In other embodiments, the dielectric plug 122 may be omitted and the via hole 108 can be filled or partially filled with a gas or other type of intermediary material.

[0020] In many embodiments, the via 120 is electrically coupled to metal contacts that are located on portions of the top side 105 or the bottom 106 side of the dielectric layer 102. For example, the circuit board 100 can include first and second metal lead lands 130-131, first metal traces 134 (identified individually by reference numbers 134a-b), and second metal traces 135 (identified individually by reference numbers 135a-b). The first lead land 130 and individual first and second traces 134a and 135a are attached at the top side 105 of the dielectric layer 102, and the second lead land 131 and individual first and second traces 134b and 135b are attached at the bottom side 106 of the dielectric layer 102. The lead lands 130-131 are coupled to the wall platings 114-115 of the via 120. More specifically, the first traces 134a-b are connected to the first interconnect 110 via the first and second lead lands 130-131, and the second traces 135a-b are similarly connected to the second interconnect 111 via the first and second lead lands 130-131. In several embodiments, the partitions 118-119 separate a first portion of the lead lands 130-131 that

are coupled to the first interconnect 110 from a second portion of the lead lands 130-131 that are coupled to the second interconnect 111. Accordingly, the first traces 134a-b and the second traces 135a-b intercouple opposite sides of the dielectric layer 102 through separate conduction paths that both pass through the via hole 108.

[0021] Figure 2A is a cross-section of Figure 1 along line 2A-2A illustrating the circuit board 100 and a plated portion of the via 120. This view shows the dielectric layer 102, the via 120, the lead lands 130-131, and the traces 134-135. The dielectric layer 102 can be plated with top- and bottom-side cladding layers 140-141 that are sandwiched between portions of the dielectric layer 102 and the interconnects 110-111. The cladding layers 140-141 and the interconnects 110-111 can have individual patterns that correspond to the shape of individual lead lands 130-131 (e.g., a ring) and individual traces 134-135 (e.g., a line). In several embodiments, the via 120, including the dielectric plug 122, has a general shape that corresponds to the shape of the via hole 108 (Figure 1). At a first lateral side 124, a portion of the first interconnect 110 (i.e., the first wall plating 114) is at one side of the dielectric plug 122. At a second lateral side 125, a portion of the second interconnect 111 (i.e., the second wall plating 115) is at another side of the dielectric plug 122. The plug 122 has partition regions that are defined by walls of the partitions 118-119 (drawn in phantom) that separate and electrically isolate the wall platings 114-115 from one another (described below).

[0022] Figure 2B is a cross-section of Figure 1 along line 2B-2B illustrating the circuit board 100 and a non-plated portion of the via 120. The dielectric layer 102 can include the partitions 118-119, which define lateral edges of first and second partition regions 150-151 (drawn in phantom) on the via 120, or more specifically, on the dielectric plug 122. In many embodiments, the partition regions 150-151 are also generally located between and electrically isolate portions of the lead lands 130-131 (also drawn in phantom).

[0023] In general, and in contrast to the partitioned via 120, conventional vias occupy a significant amount of surface area on a circuit board layer. Although the vias themselves do not necessarily take up a large area, the lead land that surrounds the via can create a substantial footprint. Each via typically needs to be surrounded by a lead land in order to accommodate an overlap tolerance with a metal contact (e.g., another via) on an above- or below-located circuit

board layer. Most conventional circuit board layers typically have design rules that require a minimum lead land diameter corresponding to this overlap tolerance. Such design rules can also establish a preferred spacing distance between individual traces (i.e., to conserve surface area). However, at the portion of the circuit board layer where the individual traces are routed through separate vias, the spacing between individual traces exceeds the preferred spacing because the required diameter of the lead land is much larger than the minimum allowable trace space elsewhere on the board. Consequently, individual traces cannot be routed as close together as desired. This is particularly problematic for electronic components that operate at data transfer rates in the Gigabit-per-second regime or higher because such components generally used differential data transmission techniques over pairs of metal traces that are aligned in parallel and spaced apart from one another. When the parallel traces route through a conventional via, they also divert, increasing their spacing distance. This produces a slight variation in signal path length, which creates a discontinuity in differential impedance.

[0024] Several embodiments of the via 120, however, can conserve surface area on a circuit board layer by coupling multiple traces through an individual via hole. For example, the via 120 allows two separate metal traces to be electrically coupled through the circuit board 100 while only occupying a single lead land area. In addition, in other embodiments, three or more metal traces can be routed through a partitioned via. For example, a via hole can be partitioned to have three or more separate sidewall portions that are individually plated with a metal layer. Further, in some embodiments, partitioned vias allow traces to be aligned in parallel without having to divert to separate vias. Such traces can be separated from each other by a fixed spacing distance and thus can allow electronic components to communicate differentially without impedance discontinuities (see, e.g., Figure 9).

[0025] Figures 3-7B illustrate stages of forming the partitioned via 120 in accordance with several embodiments of the disclosure. Figure 3 is a cross-sectional side view of the dielectric layer 102 and the cladding layers 140-141. In many embodiments, the dielectric layer 102 includes a core material (e.g., G10/FR4 or other type of epoxy or glass based material) and the cladding layers 140-141 include a conductive material (e.g., copper, gold, or other type of cladding material that can be plated, laminated, or otherwise bonded). In several embodiments, the dielectric

layer 102 can be part of a support base for a double-sided circuit board or be included in a stack of single- or double-sided circuit board layers. In other embodiments, and depending on how the dielectric layer 102 is used, one or more of the cladding layers 140-141 can be omitted (e.g., if the dielectric layer 102 is used as a single-sided circuit board layer).

[0026] Figure 4A is a cross-sectional side view of the dielectric layer 102 after forming a first hole 160, including a sidewall with first and second sidewall portions 164-165, by a first patterning process. Figure 4B is a top-view of the dielectric layer 102 showing a shape (i.e., a circle) of the first hole 160. The first patterning process removes dielectric material from the dielectric layer 102 and can include mechanical drilling, laser drilling, or mechanical stamping through the dielectric layer 102. Mechanical drilling processes use an automated drilling machine having a drill bit that forms holes in the dielectric layer at pre-programmed locations. Laser drilling processes pattern a dielectric layer in a similar fashion, but instead use a laser in lieu of a drill bit. The laser ablates portions of the dielectric layer and thus creates relatively smaller holes than mechanically drilled holes. Mechanical stamping processes can also be automated and include the use of a stamping machine or punch tool. The stamping machine punches out dielectric material from the dielectric layer 102, leaving a patterned void in the dielectric layer 102. Other patterning processes can include various types of wet or dry chemical etching techniques and corresponding lithographic patterning and development steps. For example, in embodiments that comprise semiconductor based substrates, the first patterning processes may incorporate the well developed chemical etching and lithography techniques of the semiconductor arts. Also, in other embodiments, the first patterning process can be omitted. The dielectric layer 102, for example, can be a substrate that has been pre-fabricated and includes individual pre-formed holes corresponding to the shape of the first hole 160.

[0027] Figure 5 is a cross-sectional side view of the dielectric layer 102 after forming a metal plating layer 170 that covers the sidewall portions 164-165 of the first hole 160. The plating layer 170 can be a material such as copper, aluminum, or an alloy of the two that is deposited onto the sidewall portions 164-165. The plating layer 170 can be formed using a process such as electroplating, electroless plating, or other types of thin film deposition techniques (e.g., physical and chemical vapor deposition). In several embodiments, the plating layer 170 also covers at least

one of the cladding layers 140-141. Stacked portions of the plating layer 170 and the cladding layers 140-141, for example, can be used to form the lead lands 130-131 and traces 134-135 (see, e.g., Figures 2A-B).

[0028] Figure 6A is a cross-sectional side view of the via hole 108 in the dielectric layer 102 formed by cutting the partitions 118-119 in the first hole 160 using a second patterning process. Figure 6B is a top view of the dielectric layer 102 showing a shape of the partitions 118-119 (e.g., rectilinear) of a partitioned via. The partitions 118-119 generally correspond to sections where the second patterning process has removed portions of the plating layer 170 from the first hole 160. In many embodiments, the second patterning process further removes dielectric material from the dielectric layer 102. The second patterning process can also remove portions of the plating layer 170 and the cladding layers 140-141 from top- and bottom-side portions of the dielectric layer 102 that are adjacent to the partitions 118-119. In several embodiments, the second patterning process can be similar to the first patterning process, but the second pattering process augments the first hole 160 to have a definable boundary between the sidewall portions 164-165. For example, any one of mechanical drilling, laser drilling, mechanical stamping, or chemical etching can be used to augment the first hole 160 by removing the portions of the plating layer 170 or dielectric material from the dielectric layer 102.

[0029] Figures 7A and 7B are cross-sectional side views of the dielectric layer 102 after filling the via hole 108 with a dielectric spacer material 190. The dielectric spacer material 190 may be a non-conductive ink that is held by surface tension to the plating layer 170 and the walls of the partitions 118-119. In other embodiments, the dielectric spacer material 190 is a conformal and non-conductive film that is deposited or otherwise formed in the via hole 108.

[0030] Returning to Figures 2A and 2B, after the via hole 108 has been filled, excess dielectric material 190 can be etched, compressed, planarized, or otherwise removed from top- or bottom-side surfaces of the dielectric layer 102. Also, the plating layer 170 and the cladding layers 140-141 can be patterned to form the lead lands 130-131 and the traces 134-135. The dielectric layer 102, for example, may be covered in a photolithographic film that is patterned, developed, and subsequently etched to create the shape of the leads lands 130-131 and the traces 134-135 (e.g., via a wet or dry etch).

[0031] Embodiments of the partitioned via 120 can have any of a wide variety of different shapes that can be adapted by modifying the shape of the via hole 108. Figure 8A is a top view of an embodiment of an elliptical via 220 having a plurality of elliptically segmented lead lands 230a-d. An elliptically shaped hole 260 and partition cuts using a cross-shaped cutting pattern 280 can form four separate partition regions 250-253 between the lead lands 230a-d. In this embodiment, the via 220 can route up to four separate electrical connections through a circuit board layer via the lead lands 230a-d. As another example, Figure 8B is top view of a via 320 having a plurality of lead land 330a-d that have a pentagon shape. A pentagon shaped hole 360 and a branched cutting pattern 380 can form five separate partition regions 350-354 electrically separating the lead lands 330a-e. Accordingly, the partition regions 350-354 allow up to five electrical connection to be routed through the via 320. In other embodiments, the vias and lead lands may have other types of circular, elliptical, polygonal shapes (e.g., a triangle, a square, a hexagon, etc.), or combinations thereof. In addition, different combinations of patterning processes can be used to create a desired hole shape or number of wall platings along the hole shape. For example, Figure 8C shows top views of a triangular hole 460, a square hole 560, and a pentagon hole 660 that have been formed by a mechanical stamping process. Using the same circular drill (e.g., mechanical or laser), a second patterning process can create a circular augmentation 480 that yields three separate wall platings 414-416 in the triangular hole 460, four separate wall platings 514-517 in the square hole 560, and five separate wall platings 614-618 in the polygon hole 660.

[0032] Embodiments of partitioned vias can also allow for a variety of configurations of traces, lead lands, and other contacts to be separately routed through a common via hole. For example, Figure 9 is an isometric view of a portion of a circuit board layer 700 having a dielectric layer 702 and an embodiment of a triangular shaped via 720. The dielectric layer 702 can include a star shaped via hole 708 that includes partitions 717-719. The via 720 can include metal wall platings 714-716 that are separated by individual partitions 717-719, and may further include a dielectric plug (not shown). The via 720 may also be at least partially surrounded by triangular shaped metal lead lands 730-731 that are located at opposite sides of the dielectric layer 702. In this example, the via 720 can electrically intercouple individual metal traces 734-735 and sets of parallel metal traces 737-738, which are separated from each by a fixed distances d_1. Notably, the fixed distance d_1 does not increase when the sets of traces 737-738 route through the via hole 708

(mitigating variations in differential impedance). Accordingly, two or more electronic components can be electrically coupled together in a single-ended fashion using the individual traces 731-732 or differentially using the sets of traces 737-738. The electronic components, for example, may be attached to opposite sides of the circuit board layer 702.

[0033] In other embodiments, an individual circuit board layer or a stacked system of such circuit board layers may include one or more embodiments of a partitioned via. Figure 10 is a cross-sectional side view of a circuit board system 800 having individual circuit board layers 801-805 or stacking layers that are intercoupled by one or more partitioned vias 820-823. The stacking layers 801-805 have individual surfaces that include traces, lead lands, and other metal contacts that are electrically coupled to an above- or below-located stacking layer through one or more of the vias 820-823. Individual vias can be formed, for example, by removing dielectric material from one or more of the stacking layers 801-805 and creating a via hole that extends through at least one of the stacking layers or towards one or more of the metal contacts located at any one of the stacking layers. For example, the vias 820-821 are "blind" vias that are aligned with metal contacts that are located at the circuit board layers 801 and 803, respectively. The via 822 is a "buried" via sandwiched between the circuit board layers 802 and 804. The via 823 is a "through-hole" via that electrically intercouples the top and bottom sides of the system 800. In several embodiments, the system 800 can further include dielectric laminating layers 870-871 at the top and bottom sides of the system. Portions of the laminating layers 870-871 may expose electrical contacts that can include a gold and/or nickel plating layer 850 (to prevent rapid oxidation of copper based cladding and plating layers). In many embodiments, a variety of electronic or microelectronic components are attached to the top or bottom sides of the system 800. An electronic component, for example, may have one or more contacts that are electrically coupled to any one of the exposed contacts of the system 800 (e.g., by wire bonding or soldering). In other embodiments, the system 800 includes more or fewer circuit board layers.

[0034] Any one of the partitioned vias or corresponding circuit board layers described above with reference to Figures 1-10 can be incorporated into any of a myriad of larger or more complex systems 990, a representative one of which is shown schematically in Figure 11. The system 990 can include a processor 991, a memory 992 (e.g., SRAM, DRAM, Flash, or other memory device),

input/output devices 993, or other subsystems or components 994. Electronic devices may be included in any of the components shown in Figure 11. The resulting system 990 can perform any of a wide variety of computing, processing, storage, sensor, imaging, or other functions. Accordingly, representative systems 990 include, without limitation, computers or other data processors, for example, desktop computers, laptop computers, Internet appliances, hand-held devices (e.g., palm-top computers, wearable computers, cellular or mobile phones, personal digital assistants), multi-processor systems, processor-based or programmable consumer electronics, network computers, and minicomputers. Other representative systems 990 include cameras, light or other radiation sensors, servers and associated server subsystems, display devices, or memory devices. Components of the system 990 may be housed in a single unit or distributed over multiple, interconnected units, e.g., through a communications network. Components can accordingly include local or remote memory storage devices and any of a wide variety of computer-readable media.

[0035] From the foregoing, it will be appreciated that specific embodiments have been described herein for purposes of illustration, but well-known structures and functions have not been shown or described in detail to avoid unnecessarily obscuring the description of the embodiments. Where the context permits, singular or plural terms may also include the plural or singular term, respectively. Moreover, unless the word "or" is expressly limited to mean only a single item exclusive from the other items in reference to a list of two or more items, then the use of "or" in such a list is to be interpreted as including (a) any single item in the list, (b) all of the items in the list, or (c) any combination of the items in the list. Additionally, the term "comprising" is used throughout to mean including at least the recited feature(s) such that any greater number of the same feature and/or additional types of other features are not precluded. It will also be appreciated that specific embodiments have been described herein for purposes of illustration but that various modifications may be made within the claimed subject matter. For example, many of the elements of one embodiment can be combined with other embodiments in addition to, or in lieu of, the elements of the other embodiments. Accordingly, the invention is not limited except as by the appended claims.

CLAIMS

I/We claim:

[c1] 1. A substrate, comprising:

a non-conductive layer having a top side, a bottom side, and a via hole extending between the top and bottom sides and including a sidewall having a first section and a second section; and

a partitioned via including a first metal interconnect within the via hole on the first section of the sidewall and a second metal interconnect within the via hole on the second section of the sidewall, wherein the second metal interconnect is electrically isolated from the first metal interconnect.

[c2] 2. The substrate of claim 1 wherein the first metal interconnect is separated from the second metal interconnect by a gap within the via hole.

[c3] 3. The substrate of claim 2 wherein the gap is at least partially filled with a dielectric material.

[c4] 4. The substrate of claim 2 wherein the gap is defined by at least two partitions cut through the sidewall of the via hole.

[c5] 5. The substrate of claim 4 wherein the first metal interconnect comprises a first portion of a metal layer and the second metal interconnect comprising a second portion of the metal layer.

[c6] 6. The substrate of claim 5 wherein the metal layer is further located on at least one of a top-side portion and a bottom-side portion of the non-conductive layer.

[c7] 7. The substrate of claim 6, further comprising a metal lead land formed in the metal layer and located on at least one of the top-side and bottom-side portions of the non-conductive layer, the metal lead land at least partially surrounding the via and having a first portion that is coupled to the first interconnect and a second portion that is coupled to the second interconnect, the first portion of the lead land being electrically isolated from the second portion of the lead land by the individual partitions.

[c8] 8. The substrate of claim 7, further comprising a metal trace formed in the metal layer and located on at least one of the top-side and bottom-side portions of the non-conductive layer, the metal trace coupled to the first portion of the lead land.

[c9] 9. The substrate of claim 7, further comprising a stacking layer having a metal contact that is attached to and substantially aligned with the lead land.

[c10] 10. The substrate of claim 1, further comprising a stacking layer attached to at least one of a top-side portion and a bottom-side portion of the non-conductive layer, the partitioned via further extending through at least a portion of the stacking layer.

[c11] 11. A circuit board comprising a partitioned via having:

a sidewall through a dielectric layer defining an opening;

a first metal interconnect within the opening; and

a second metal interconnect within the opening and electrically isolated from the first interconnect, wherein the first and second interconnects are formed from a common metal layer deposited onto the sidewall.

[c12] 12. The circuit board of claim 11 wherein the via further comprises a dielectric plug, and wherein the first and second interconnects contact separate portions of the dielectric plug.

[c13] 13. The circuit board of claim 12 wherein the plug includes a partition region that separates the first interconnect from the second interconnect.

[c14] 14. The circuit board of claim 13, further comprising a segmented metal lead land at least partially surrounding at least one of a top-side portion and a bottom-side portion of the via, wherein individual segments of the lead land are separated from each other by the partition region.

[c15] 15. A computing system, comprising a processor, a memory, and at least one of an input device and an output device, wherein the computing system includes the circuit board according to claim 11.

[c16] 16. An interconnect system, comprising:

a circuit board layer having a surface and a via hole that extends through the circuit board layer;

a metal contact at the surface of the circuit board layer, wherein the metal contact at least partially surrounds the via hole, and the metal contact is electrically coupled to an opposing surface of the circuit board layer through the via hole and has a first portion and a second portion electrically isolated from the first portion;

a first metal trace attached to the circuit board layer and coupled to the first portion of the metal contact; and

a second metal trace attached to the circuit board layer and coupled to the second portion of the metal contact.

[c17] 17. The interconnect system of claim 16 wherein the first and second metal traces are located on opposite sides of the circuit board layer.

[c18] 18. The interconnect system of claim 16 wherein the first and second metal traces are located on the same side of the circuit board layer and wherein the first metal trace is at least substantially parallel to the second metal trace.

[c19] 19. The interconnect system of claim 16, further comprising a metal plating layer that at least partially covers a sidewall of the via hole, is electrically coupled to the first portion of the metal contact, and is electrically isolated from the second portion of the metal contact.

[c20] 20. A method for manufacturing a substrate, the method comprising:

forming a hole through a non-conductive layer, the hole including a sidewall;

depositing a conductive layer on at least a portion of the sidewall; and

forming partitions within the hole that separate the conductive layer into a first interconnect within the hole and a second interconnect within the hole that is electrically isolated form the first interconnect.

[c21] 21. The method of claim 20 wherein the non-conductive layer comprises at least one of a dielectric core layer of a circuit board and a semiconductor layer of a semiconductor wafer.

[c22] 22. The method of claim 20 wherein forming the hole and the partitions comprises removing conductive material from the conductive layer using a patterning process that includes at least one of chemical etching, mechanical drilling, laser drilling, and mechanical stamping.

[c23] 23. The method of claim 20, further comprising at least partially filling the hole with a dielectric spacer material.

[c24] 24. The method of claim 20 furthering comprising:

depositing the conductive layer on at least one of a top-side and a bottom-side of the non-conductive layer; and

forming a lead land on at least one of a top-side portion and a bottom-side portion of the conductive layer, the lead land at least partially surrounding the hole and including first and second segmented portions, the first segmented portion being electrically coupled to the first interconnect and the second segmented portion being electrically coupled to the second interconnect and electrically isolated from the first interconnect.

[c25] 25. The method of claim 24 further comprising forming a first trace on at least one of the top-side andbottom-side portions of the conductive layer, the first trace being electrically coupled to the first segmented portion of the lead land.

[c26] 26. The method of claim 25 further comprising forming a second trace on at least one of the top-side and bottom-side portions of the conductive layer, the second trace being electrically coupled to the second segmented portion of the lead land.

[c27] 27. The method of claim 26 wherein the first and second traces are located on the same side of the non-conductive layer and are substantially parallel to one another.

[c28] 28. The method of claim 20 wherein forming the hole further includes forming the hole through a portion of a stacking layer that is attached to the non-conductive layer.

[c29] 29. A method for electrically routing component contacts of one or more electronic components using a circuit board system of one or more circuit board layers, the method comprising:

coupling a first contact of a component to a first exposed contact of a circuit board layer associated with a circuit board system, the first exposed contact being coupled to a first signal path of the circuit board system routed through a via hole in at least one dielectric layer of the circuit board system; and

coupling a second contact of the component to a second exposed contact of the circuit board layer, the second exposed contact being coupled to a second signal path of the circuit board system routed through the via hole and electrically isolated from the first signal path.

[c30] 30. The method of claim 29 wherein the via hole includes a first sidewall section covered with a first wall plating and a second sidewall section covered with a second wall plating that is electrically isolated from the first wall plating, the first signal path including the first wall plating and the second signal path including the second wall plating.

[c31] 31. The method of claim 29 wherein the circuit board system includes at least one set of parallel metal traces that route the first and second signal paths towards the via hole.

[c32] 32. The method of claim 31 wherein the first and second component contacts are associated with an electronic component that is attached to the circuit board layer.

[c33] 33. The method of claim 32 wherein the electronic component is configured to transmit a differential signal over the set of parallel traces.

[c34] 34. The method of claim 29 wherein the first component contact is associated with a first electronic component attached to the circuit board layer and the second component contact is associated with a second electronic component attached to the circuit board layer.