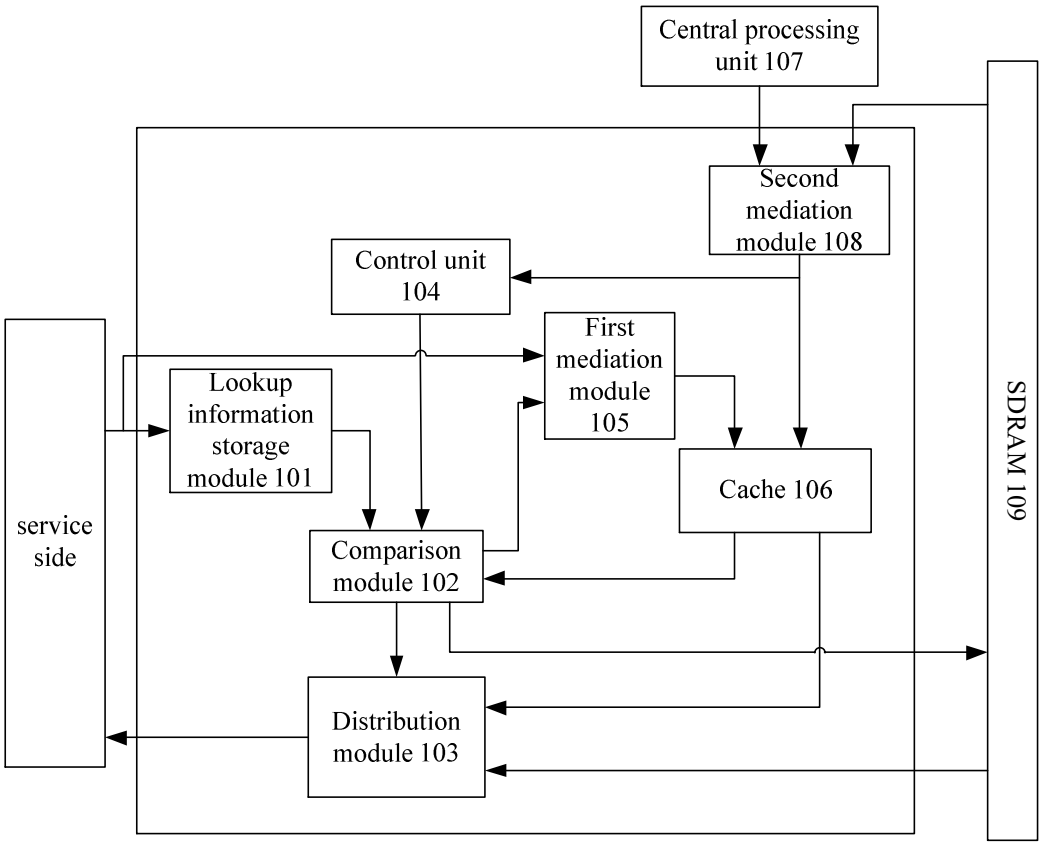
Central processing unit 107
Second mediation module 108
Control unit 104
First mediation module 105
Lookup information storage module 101
Cache 106
service side
Comparison module 102
Distribution module 103
SDRAM 109

FIG. 1

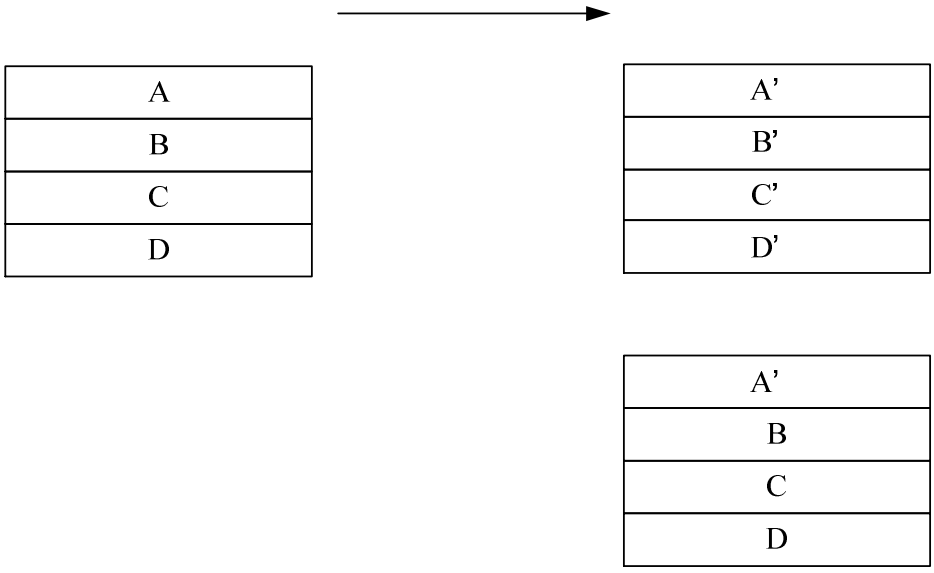

FIG. 2

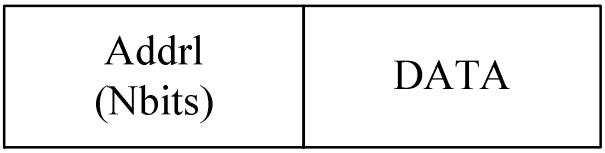

FIG. 3

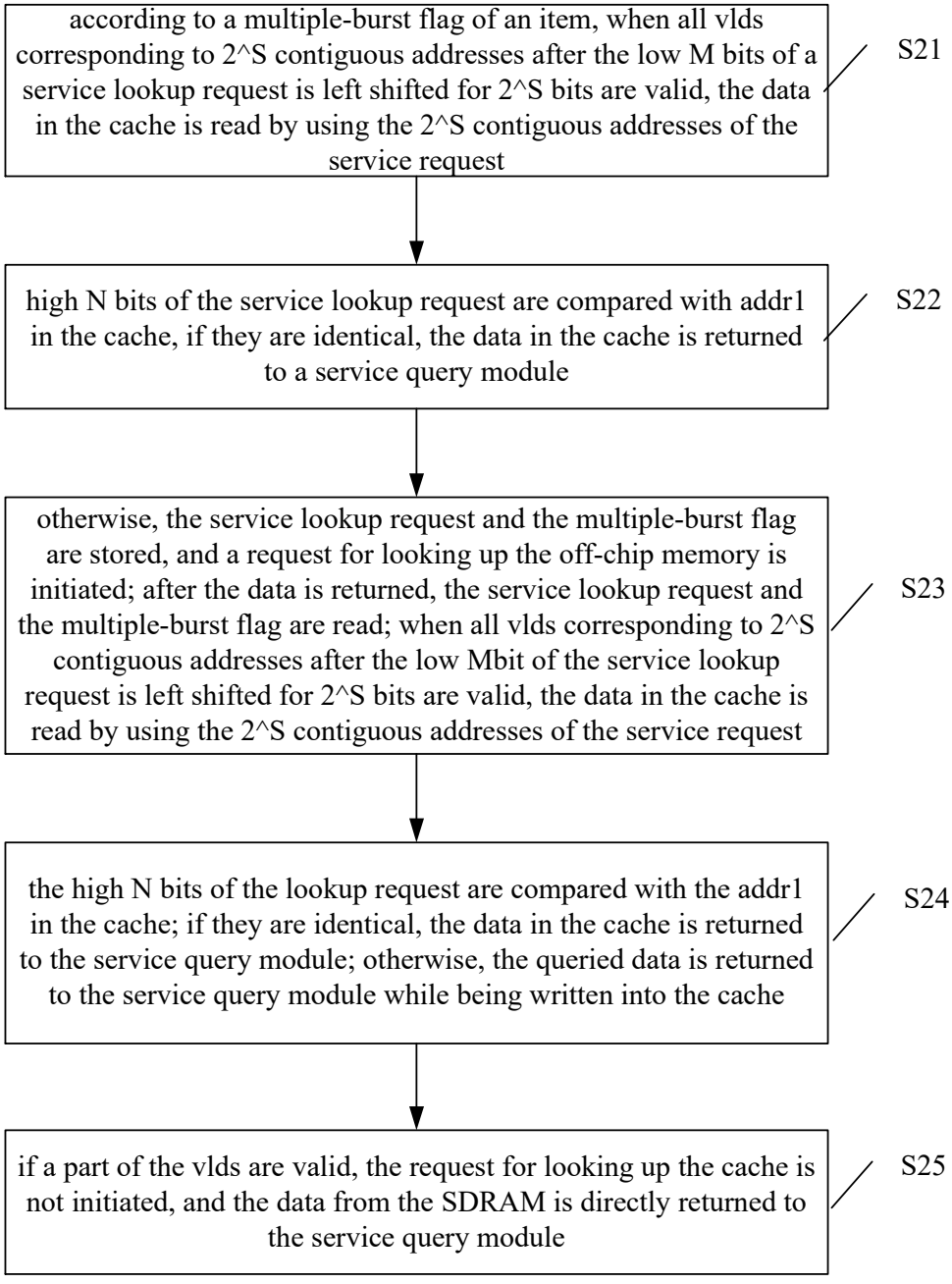
according to a multiple-burst flag of an item, when all vlds corresponding to 2^S contiguous addresses after the low M bits of a service lookup request is left shifted for 2^S bits are valid, the data in the cache is read by using the 2^S contiguous addresses of the service request
S21
high N bits of the service lookup request are compared with addr1 in the cache, if they are identical, the data in the cache is returned to a service query module
S22
otherwise, the service lookup request and the multiple-burst flag are stored, and a request for looking up the off-chip memory is initiated; after the data is returned, the service lookup request and the multiple-burst flag are read; when all vlds corresponding to 2^S contiguous addresses after the low Mbit of the service lookup request is left shifted for 2^S bits are valid, the data in the cache is read by using the 2^S contiguous addresses of the service request
S23
the high N bits of the lookup request are compared with the addr1 in the cache; if they are identical, the data in the cache is returned to the service query module; otherwise, the queried data is returned to the service query module while being written into the cache
S24
if a part of the vlds are valid, the request for looking up the cache is not initiated, and the data from the SDRAM is directly returned to the service query module
S25

FIG. 4

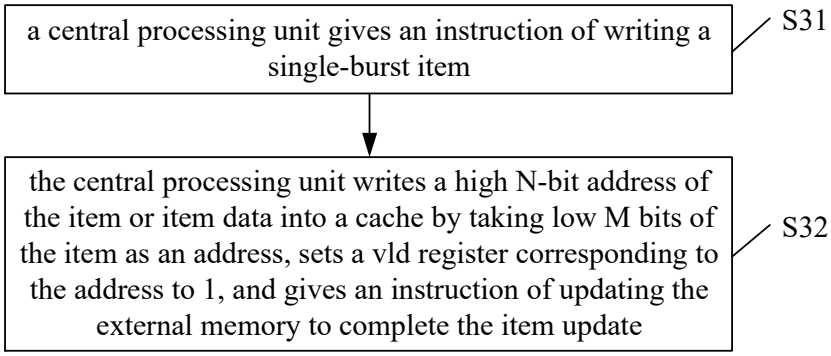
a central processing unit gives an instruction of writing a single-burst item
S31
the central processing unit writes a high N-bit address of the item or item data into a cache by taking low M bits of the item as an address, sets a vld register corresponding to the address to 1, and gives an instruction of updating the external memory to complete the item update
S32

FIG. 5

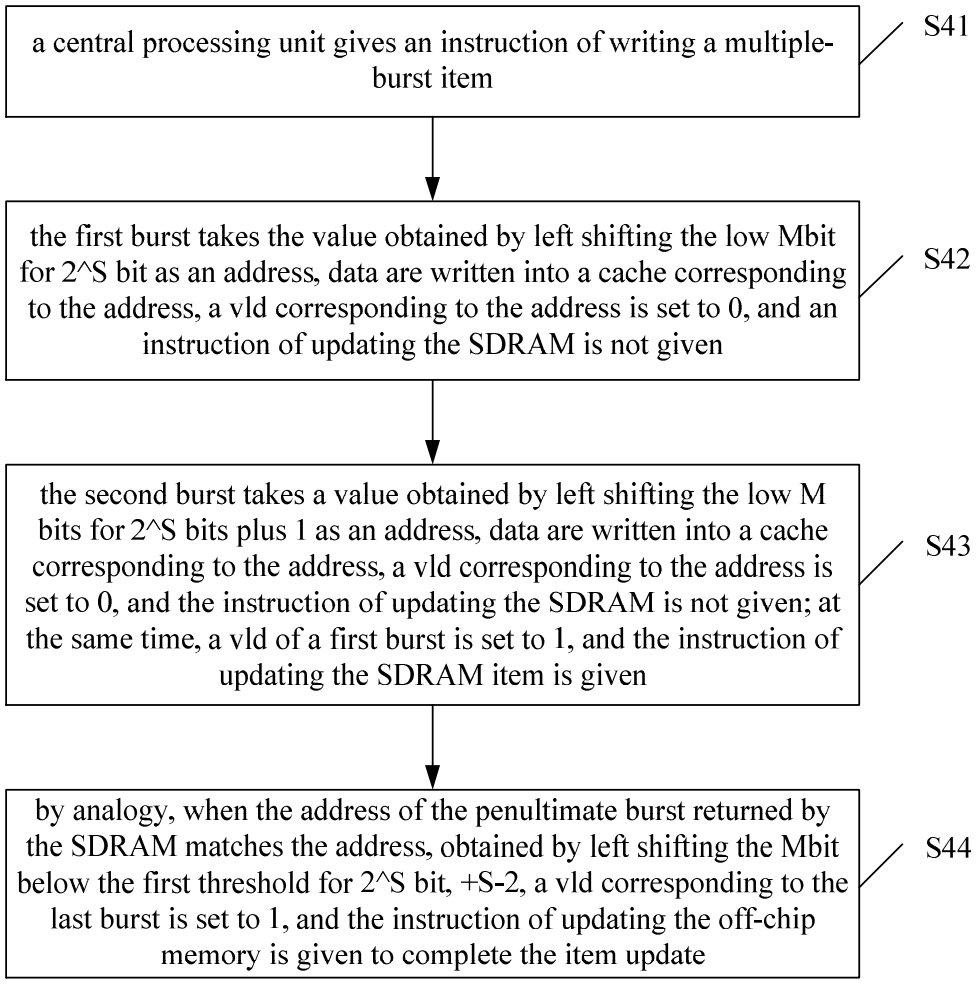
a central processing unit gives an instruction of writing a multiple-burst item
S41
the first burst takes the value obtained by left shifting the low Mbit for 2^S bit as an address, data are written into a cache corresponding to the address, a vld corresponding to the address is set to 0, and an instruction of updating the SDRAM is not given
S42
the second burst takes a value obtained by left shifting the low M bits for 2^S bits plus 1 as an address, data are written into a cache corresponding to the address, a vld corresponding to the address is set to 0, and the instruction of updating the SDRAM is not given; at the same time, a vld of a first burst is set to 1, and the instruction of updating the SDRAM item is given
S43
by analogy, when the address of the penultimate burst returned by the SDRAM matches the address, obtained by left shifting the Mbit below the first threshold for 2^S bit, +S-2, a vld corresponding to the last burst is set to 1, and the instruction of updating the off-chip memory is given to complete the item update
S44

FIG. 6