DESCRIPTION

TITLE: SEMICONDUCTOR SUBSTRATE FOR LASER SEPARATION AND PROCESS FOR MANUFACTURING THREE-DIMENSIONAL SEMICONDUCTOR STRUCTURES

FIELD OF THE INVENTION

The present invention relates to the field of the semiconductor industry and proposes a semiconductor substrate designed to allow laser separation of a single-crystal layer. The present invention also relates to a process for manufacturing a three-dimensional semiconductor structure using said substrate.

CONTEXT OF THE INVENTION

Semiconductor devices are becoming increasingly complex, vertically integrating a plurality of semiconductor chips fulfilling various functions. The main motivations for vertical integration are to reduce the distances between chips, and to reduce the overall lateral dimensions of the devices.

For decades, semiconductor devices were manufactured solely from bulk semiconductor materials, mainly silicon wafers several hundred micrometres thick. For cost and performance reasons, many semiconductor devices today are manufactured on relatively thin layers of semiconductor materials, less than 10 micrometres thick. In addition, the vertical integration mentioned above also requires semiconductor chips to be manufactured on thin films, so as to facilitate their integration into three-dimensionally designed devices.

In the industry, these integrations are known under the name 2.5D IC (2.5-Dimensional Integrated Circuit) or 3D IC (3-Dimensional Integrated Circuit), representing advanced encapsulation techniques that combine several integrated circuits, or microchips, on a single support. Stacked microchips can use vertical connections such as TSVs (Through Silicon Vias) and flip-chip assembly technology to ensure the electrical connection between microchips.

In the manufacturing chain for a single 2.5 ID or 3D IC technology housing, the industrial players who supply the semiconductor substrates are generally not the same as those who treat these substrates, used as the base material for manufacturing the microchips themselves, and the latter may also be different from the players who integrate a variety of microchips on a single support.

In addition, the manufacturing tools that have been developed for a specific range of manufacturing processes sometimes prove inadequate for newly developed manufacturing processes or applications. As these manufacturing tools are extremely expensive to replace, in order to recoup their development and purchase costs, they must be used to manufacture devices according to sub-optimal processes, but as efficiently as possible.

It is found that there is a need to provide semiconductor substrates and processes that are capable of being used by a variety of players in the semiconductor industry for various applications, including those requiring advanced encapsulation techniques. Also, these substrates must allow alternative manufacturing processes to be proposed that make optimum use of existing manufacturing tools.

SUBJECT OF THE INVENTION

A first aspect of the invention is a semiconductor substrate comprising an active material layer which can be readily separated by laser irradiation, this process being known as “laser lift-off”. The active material layer is intended to form an active layer of a semiconductor device.

A second aspect of the invention is a process for manufacturing said semiconductor substrate.

A third aspect of the invention is a process for manufacturing an active layer, formed from the active material layer of the first subject of the invention.

A fourth aspect of the invention is a process for manufacturing a 3D integrated semiconductor device.

SUMMARY OF THE INVENTION

A first subject of the invention is a semiconductor substrate designed to allow laser separation of an active material layer, comprising: a support substrate; an inorganic layer on the support substrate, the inorganic layer being formed from a material chosen from Al2O3, TiO2, WO3, La2O3, LaAlO3 and TiN; an electrically insulating layer on the inorganic layer; and the active material layer on the electrically insulating layer, the active material layer being single-crystal.

According to further features, in the semiconductor substrate, the support substrate may be formed from single-crystal silicon; the inorganic layer may have a thickness of between 10 nm and 2 μm; the insulating layer may comprise silicon oxide and have a thickness of between 10 nm and 1 μm; and the active material layer may be chosen from Si, SiGe, GaAs, SiC, GaN and PZT and may have a thickness of between 5 nm and 2 μm.

The substrate according to the invention benefits from the high quality of a single-crystal material and may be included in a cost-effective manner in a process for manufacturing highly integrated semiconductor devices. Specifically, the substrate is suitable for a fast, low-cost method for separating a treated active layer from an active material layer of the substrate.

A second subject of the invention is a process for manufacturing the semiconductor substrate of the invention, comprising the following steps: implanting a light ion species through a top surface of an active material donor substrate so as to form a fragile plane in the active material donor substrate; forming, in this order, the inorganic layer and the electrically insulating layer on a surface of a support substrate; bonding the top surface of the active material donor substrate to a free surface of the insulating layer; and cleaving the active material donor substrate at the fragile plane so as to leave the active material layer attached to the support substrate via the insulating layer and the inorganic layer.

A third subject of the invention is a process for manufacturing an active layer, involving the implementation of the process for manufacturing the semiconductor substrate according to the second subject of the invention in a first manufacturing unit, also comprising the following steps: sending the semiconductor substrate to a second manufacturing unit; and sending to said second manufacturing unit information representative of the fact that the active material layer of the semiconductor substrate is to be separated from the support substrate in a separation step involving irradiation of the inorganic layer with infrared radiation.

According to other non-limiting features of the invention, taken alone or in any technically feasible combination:

- the process for manufacturing an active layer for a semiconductor device, comprising the implementation of the process for manufacturing the semiconductor

substrate according to the first subject of the invention, may also comprise the steps of treating the active material layer so as to form the active layer; and separating the active layer from the support substrate at the inorganic layer by irradiating the inorganic layer with infrared radiation;

- the process for manufacturing an active layer for a semiconductor device, comprising the implementation of the process for manufacturing the semiconductor substrate according to the first subject of the invention, may also comprise the following steps: treating the active material layer so as to form the active layer; positioning and bonding connection pads of the active layer to connection pads of a receiving substrate; separating the support substrate from the active layer at the inorganic layer by irradiating the inorganic layer with infrared radiation; cleaning a surface of the active material layer opposite the receiving substrate after separation from the support substrate; after the cleaning step, treating the active material layer so as to form a finished active layer; and

- the active material may comprise a layer of semiconductor material less than 1 micrometre thick.

A fourth subject of the invention is a process for manufacturing a three-dimensional integrated semiconductor device, which involves reiterating the process for manufacturing an active layer for a semiconductor device on a same portion of a same receiving substrate so as to form a first stack consisting of a plurality of stacked active layers, one of the active material layers to be stacked on a previously obtained active layer being positioned thereon by means of a first handling device.

According to other non-limiting features of the invention, taken alone or in any technically feasible combination:

- the process for forming a three-dimensional integrated semiconductor device may also comprise the following steps: cutting the first stack in such a manner as to form a plurality of semiconductor elements each comprising an elementary portion of the first stack; on a control substrate, forming a second stack of a plurality of elementary portions, two adjacent stacked elementary portions of the second stack being connected to each other by first electrically conductive balls, the second stack being connected to the control substrate by second electrically conductive balls, in which, when forming the second stack, the elementary portions are positioned one

on top of the other by means of a second handling device different from the first handling device;

- the first handling device and the second handling device may have a first height limit and a second height limit for the objects they can position, respectively, the first height limit being smaller than the second height limit;

- the first handling device may be hybrid bonding equipment and the second handling device may be flip-chip bonding equipment; and

- the three-dimensional integrated semiconductor device may be a memory device, each elementary portion of the first stack being a digital memory element.

A manufacturing method according to the invention is an inexpensive and fast alternative to conventional transfer technologies. The method allows simple transfer of high-quality semiconductor layers, which may be thin and/or single-crystal layers. This method also serves to overcome equipment limitations relating to the maximum height of handled elements to be integrated into a semiconductor device.

Other features and advantages of the invention will become apparent from the following detailed description, which is given with reference to the appended figures, in which:

[Fig. 1] Figure 1 illustrates the formation of a fragile layer in a donor substrate for a process for manufacturing a semiconductor substrate according to the invention;

[Fig. 2] Figure 2 illustrates the manufacturing steps of the process for manufacturing a semiconductor substrate;

[Fig. 3] Figure 3 illustrates a manufacturing step of the process for manufacturing a semiconductor substrate;

[Fig. 4] Figure 4 illustrates the manufacturing steps of the method for manufacturing a semiconductor substrate;

[Fig. 5] Figure 5 illustrates the method for manufacturing a semiconductor substrate;

[Fig. 6] Figure 6 illustrates a method for manufacturing an active layer;

[Fig. 7] Figure 7 illustrates a method for forming a three-dimensional integrated semiconductor device;

[Fig. 8] Figure 8 illustrates the method for manufacturing an active layer;

[Fig. 9] Figure 9 illustrates the method for forming a three-dimensional integrated semiconductor device;

[Fig. 10] Figure 10 illustrates the method for forming a three-dimensional integrated semiconductor device;

[Fig. 11] Figure 11 illustrates the method for forming a three-dimensional integrated semiconductor device;

[Fig. 12] Figure 12 illustrates the method for manufacturing an active layer; and

[Fig. 13] Figure 13 illustrates conventional integration methods for three-dimensional semiconductor devices.

DETAILED DESCRIPTION OF A SPECIFIC EMBODIMENT OF THE INVENTION

Embodiment of the invention

Semiconductor substrate structure and manufacturing process

A first embodiment of the invention is explained using Figures 1 to 3 and Figure 5, which show the manufacturing steps for a semiconductor substrate designed to allow laser separation of an active material layer.

Figure 3 illustrates the semiconductor substrate Sub, which comprises: a support substrate Sprt; an inorganic layer Inorg on the silicon substrate, the inorganic layer being formed from a material chosen from TiN, Al2O3, TiO2, WO3, La2O3 and LaAlO3; an electrically insulating layer Ins on the inorganic layer; and the active material layer ActMat on the electrically insulating layer, the active material layer preferably being single-crystal. The organic layer is designed to be sufficiently absorbent with regard to infrared irradiation, such as laser irradiation, to effectively perform laser separation of the active material layer, as such or treated as an active layer, from the support substrate.

Figures 1 to 3 and 5 illustrate a method 100 for manufacturing the semiconductor substrate Sub, which comprises manufacturing steps 110 to 190.

Firstly, in step 110, an active material donor is provided. The active material donor is chosen from substrates, such as wafers, of Si, SiGe, GaAs, SiC, GaN and PZT (lead zirconate titanate), which may have a single-crystal structure.

During an ion implantation step 130, a light ion species, hydrogen H+ or helium He+, is introduced into the active material donor substrate Don through a top surface T.Surf of this donor substrate Don so as to form a fragile plane Frgl inside the donor substrate Don. The fragile plane is substantially parallel to the top surface T.Surf, as illustrated in Figure 1. The volume of the donor substrate Don comprised between the top surface T.Surf and the fragile plane Frgl defines the active material layer ActMat. In a subsequent step, this layer will be detached from the rest of the donor substrate Don by Smart Cut™ technology and transferred onto a support structure.

The introduction of ions may correspond to hydrogen implantation, i.e. ion bombardment of the T.Surf face of the donor substrate Don with hydrogen ions, as illustrated in Figure 1. Generally, the type, dose and energy of the implanted species are chosen as a function of the thickness of the layer to be transferred and the physicochemical properties of the donor substrate Don. These parameters may be adjusted to define an active material layer having a thickness of between 5 nm and 2 µm.

In parallel with steps 110 and 130, a support substrate Sprt is provided in step 120.

During a stack-forming step 140, the inorganic layer Inorg and the electrically insulating layer Ins are formed, in this order, on a surface of the support substrate Sprt, forming a first stack Stck comprising, in this order, the support substrate Sprt, the inorganic layer Inorg and the insulating layer Ins.

The inorganic layer Inorg is preferably formed from a material chosen from Al2O3, TiO2, WO3, La2O3, LaAlO3 and TiN, and in such a way as to have a thickness of between 20 nm and 2 µm. These materials have excellent compatibility with most semiconductor processes used in the industry, thus allowing a virtually universal substrate to be provided for a very wide range of applications already developed as well as potential applications. TiN is preferably chosen for its even higher overall compatibility with these processes and with the laser separation

operation which consists in detaching the active material layer from the support substrate. The inorganic layer Inorg may be formed by ALD (Atomic Layer Deposition), more particularly by PE-ALD (Plasma Enhanced Atomic Layer Deposition), PE-CVD (Plasma Enhanced Chemical Vapour Deposition), PVD (Physical Vapour Deposition), or by PCD (Photochemical Deposition), for example.

The semiconductor manufacturing processes mentioned in the above paragraph are to be understood as conventional processes used in the semiconductor industry for manufacturing microchips from starting materials, in particular semiconductor materials, such as FEOL (Front End Of Line), BEOL (Back End Of Line), SoL (Sea of Leads), RDL (Redistribution Layer) or TSV (Through Silicon Vias) manufacturing, for example. Specifically, some or several of these processes may be applied to the active material layer before the layer is detached from the support substrate, hence the need for the inorganic layer to be compatible with these processes.

The insulating layer Ins preferably comprises silicon oxide or silicon nitride and is between 10 nm and 1 µm thick. The insulating layer Ins may be formed by LPCVD (Low Pressure Chemical Vapour Deposition) or (Plasma Enhanced Chemical Vapour Deposition), for example. Silicon oxide is a material that promotes bonding between the donor substrate Don and the first stack Stck.

Next, during a bonding step 150, the top surface T.Surf of the donor substrate Don is brought into intimate contact with the free surface F.Surf of the insulating layer Ins, thus forming molecular adhesion and/or electrostatic bonding between the donor substrate and the insulating layer, as mentioned, for example, in the French patent application published under the number 2 914 492. The surfaces placed in intimate contact may be prepared by cleaning, brushing, drying, polishing or plasma activation, as is known in the field.

As is well known, during a molecular adhesion process, the exposed surfaces of the insulating layer and the donor substrate, which are perfectly clean, flat and smooth, are brought into intimate contact to promote electrostatic bonding or the development of molecular bonds, for example of the van der Waals or covalent type. The assembling of the two bodies is then achieved without the use of an adhesive. Bonding may involve the application of a low-temperature heat treatment (for

example between 50 and 300°C, typically 100°C) to heal crystal defects in the donor substrate and to reinforce the bonding energy sufficiently to allow any subsequent thinning step or another treatment.

Next, during a fractionation step 170, the active material donor substrate Don is fractionated, or split, at the fragile plane Frgl in such a manner as to leave the active material layer ActMat attached to the support substrate Sprt via the insulating layer Ins and the inorganic layer Inorg. The stack obtained after fractionation is the semiconductor substrate Sub illustrated in Figure 3.

More precisely, after the bonding step, the active material layer is detached from the rest of the donor substrate by fracturing at the fragile plane Frgl and thus transferred to the support Sprt, as illustrated in Figure 3, which shows the substrate Sub formed by assembly of the first stack Stck with the active material layer ActMat. This detachment step may also consist in applying a heat treatment at a temperature of between 350°C and 1000°C to detach the active material layer from the donor substrate and complete its transfer to the first stack. Alternatively, or in addition to heat treatment, this step may consist in applying a blade or a jet of gaseous or liquid fluid, or any other mechanical force to the fragile plane Frgl.

During step 170, which produces the structure Sub shown in Figure 3, a stabilizing heat treatment may optionally be applied to the structure Strc during a post-fragmentation step S190. The stabilizing heat treatment allows crystal defects in the active material layer to be healed and the bond between this active material layer and the insulator to be consolidated, for example by bringing the substrate Sub to a temperature of between 300°C and 600°C for a time of between 30 minutes and 10 hours. This heat treatment is preferably performed by exposing the free face of the active material layer to a neutral gaseous atmosphere.

The post-finishing step 190 also preferably comprises a step of levelling the free layer of the active material layer, for example by CMP (Chemical Mechanical Polishing) and/or wet etching. At this stage, the semiconductor substrate Sub may be ready for any treatment envisaged by the substrate user.

The semiconductor substrate can also be sent to the user without the levelling step having been performed, so as to allow the user to perform a levelling step of his choice. Specifically, the semiconductor substrate Sub is intended to be used by a

variety of actors, and the manufacturing unit where it has been manufactured will generally be different from the manufacturing unit where the active material layer will be treated to form a functional semiconductor device or part of such a device.

Transmission for active layer treatment

Figure 12 illustrates foreseeable situations in which semiconductor substrates Subs obtained as described above are manufactured in a first manufacturing unit U1, packed in a packaging box CBox and sent to a second manufacturing unit U2, where the active material layers ActMat of these semiconductor substrates Sub are treated to form the active layer ActLay, and optionally integrated into semiconductor housings Pack.

During the sending operation from U1 to U2, in addition to the substrates themselves, information Inf relating to the intended use of the substrates is transmitted to the manufacturing unit U2. More precisely, the information Inf may be representative of the fact that the substrates are to be subjected to a light irradiation treatment, such as an IR irradiation treatment by an IR laser, so as to detach the active material layer from the rest of the substrate Sub. It should be understood here that the detachment process applies to the active material layer ActMat as such, or to the active material layer after it has been transformed into the active layer ActLay, as will be seen below.

As illustrated in (A) of Figure 10, in a sending process Send0, the information Inf may take the form of a physical information leaflet directly attached to the box Cbox. The physical information notice may be sent separately by the manufacturing unit U1 to manufacturing unit U2.

Alternatively, as illustrated in (B) of Figure 10, the information Inf may take a dematerialized form such as an electronic message or file sent to the second manufacturing unit U2 in a sending process Send2 separately from the semiconductor substrates Sub which may be sent to the second manufacturing unit U2 in a first process Send1.

The starting and destination points for the semiconductor substrates must be the first and second manufacturing units, respectively, in which the semiconductor substrate treatment facilities are located. However, the starting and destination points

of the information may, in practice, be office buildings which manage or are linked to these manufacturing units. In the present document, to keep the explanations concise, it is understood that these office buildings are considered as forming part of the manufacturing units, even though they may be physically located in places other than the manufacturing facilities that process the semiconductor substrate.

Active layer Treatment - Generic

Figures 4 and 6 illustrate a generic treatment method 200 for allowing an active layer ActLay to be obtained from the semiconductor substrate Sub described above and shown in Figure 3.

During a treatment step 210, the active material layer ActMat is treated in such a way as to form the active layer ActLay, while the active material layer is still attached to the support substrate Sprt via the insulating layer Ins and the inorganic layer Inorg. The processes applied to the active material layer ActMat may be any or a combination of conventional processes used in the semiconductor industry, such as FEOL, BEOL, SoL, RDL or TSV manufacture, which may involve manufacturing techniques by addition or subtraction of material, doping, surface treatment, etc. The active layer is intended to be integrated into a semiconductor device such as a memory, a MEMS (Micro Electro Mechanical System) or a sensor.

Next, during a separation step 230, the inorganic layer (Inorg) is irradiated with IR radiation, which may be emitted by a laser, so that the active layer ActLay detaches from the support at the level of the inorganic layer, as illustrated in Figure 4. The irradiation preferably takes place through the substrate Sprt, which is chosen to be sufficiently transparent to the irradiation wavelength for the latter to reach and degrade the inorganic layer.

After the separation step 230, part or all of the insulating layer Ins and the inorganic layer Inorg may still remain attached to the active layer ActLay. During a cleaning step 250, these remnants of the insulating layer Ins and of the inorganic layer Inorg are removed by selective dry and/or wet etching so as to leave the active layer ActLay bare, as illustrated in Figure 4.

In the example shown in Figure 4, the active layer is simply detached from the support substrate Sprt. However, the active layer may be transferred to a permanent

support substrate, to a temporary substrate such as a cutting belt for further handling and/or treatment, or may be directly integrated into a semiconductor device as described below.

Active layer treatment - Integration

Figures 7 and 8 illustrate a treatment method 300 for allowing a finished active layer ActLay' to be obtained from the semiconductor substrate Sub described above and shown in Figure 3, and then integrating one or more of these active layers ActLay' into a semiconductor SC device.

During a treatment step 310 similar to process 210 described previously, the active material layer ActMat is treated in such a way as to form the active layer ActLay, while the active material layer is still part of the semiconductor substrate Sub. The processes applied to the active material layer ActMat may be any one or a combination of conventional processes used in the semiconductor industry, such as FEOL, BEOL, SoL, RDL or TSV manufacture, which may involve manufacturing techniques by addition or subtraction of material, doping, surface treatment, etc. The active layer is intended to be integrated into a semiconductor device, such as a memory, a MEMS (Micro Electro Mechanical System) or a sensor. The active layer ActLay has been structured in such a way as to be able to receive, process and/or transmit electrical signals. Specifically, to this end, it includes electrical connection pads on its surface.

During a bonding step 330, in order to integrate the active layer on a semiconductor device, the connection pads are positioned and attached to corresponding connection pads on this semiconductor device. The result of this step is illustrated in (A) of Figure 8.

The connection is preferably performed by hybrid bonding, which allows dielectric layers to be simultaneously bonded to dielectric layers and electrically conductive layers to dielectric conductive layers. Such hybrid bonding allows highly integrated devices to be obtained, with shortened electrical connections: the active layers bonded together are in direct contact with each other. Reference may be made to Figure 11 and the corresponding passage of the present description.

During a separation step 350, illustrated in (B) of Figure 8, the support substrate Sprt is separated from the active layer ActLay at the level of the inorganic

layer Inorg by light irradiation. Reference may be made to step 230 for further details, as steps 230 and 350 are identical in principle and performance, the actual parameters depending on the specific device being manufactured.

During a cleaning step 370, similar to cleaning step 250, the parts of the insulating layer Ins and inorganic layer Inorg remaining attached to the active material layer ActMat are removed, as illustrated in (C) of Figure 8, so that the active material layer can be further treated to form a functional layer of a semiconductor device.

During a treatment step 390, the active layer ActLay is treated so as to form a finished active layer ActLay', as shown in (D) of Figure 8. The processes applied to the active layer ActLay may be any one or a combination of conventional processes used in the semiconductor industry. In this example, the aim of the process is to ensure electrical connection between the two opposite sides of the active layer. In a specific example, it is a matter of allowing a functional connection between the control layer Cnt of the substrate Tmp and one or other of the active layers ActLay that may be stacked on the finished active layer ActLay'.

As indicated by number 395 in Figure 7, the sequence of manufacturing steps 310-330-350-370-390 may be repeated on the same part of the substrate Tmp so as to stack a plurality of finished active layers ActLay' one on top of the other, each being connected to the others and to the control layer Cnt of the substrate Tmp.

Three-dimensional integrated semiconductor device

Figures 9 to 11 illustrate a method for forming a three-dimensional integrated semiconductor device via the process 300 discussed above and illustrated in Figures 7 and 8.

As shown in Figure 8, an active layer ActLay' can be formed by bonding and treating an active layer on a substrate equipped with a control layer Cnt. The same process may be repeated to successively bonding several finished active layers ActLay' onto each other so as to obtain a first stack StckLay of interconnected active layers ActLay (or ActLay') on a carrier substrate Sub, as illustrated in figure 9. In practice, the sequence of manufacturing steps 310-330-350-370-390 may be repeated on the same portion of the same receiving substrate so as to form a first

stack StckLay consisting of a plurality of stacked active layers ActLay. The active layers ActLay to be stacked on a previously obtained active layer ActLay' are positioned and bonded thereon by means of a first handling device.

In principle, an arbitrary number of active layers may be stacked in this manner. However, the first handling device must be capable of performing both (i) precise positioning (also referred to as "alignment" of a wafer of an integrated circuit (denoted by "die") in the semiconductor industry) and (ii) hybrid bonding to ensure a functional and efficient electrical connection between the last added active layer ActLay and the previously obtained finished active layer ActLay'.

As illustrated in Figure 11, in this situation, a hybrid bonding process involves the precise alignment of the respective conductive pads Pad of an active layer ActLay and of a finished active layer ActLay'. These pads are embedded in the respective dielectric layers Diel. In an initial stage of the bonding process, the respective dielectric layers are brought into direct contact and bonded to each other at room temperature. Next, a heat treatment is applied and metal diffusion occurs between the wafers, forming electrical connections between the active layer ActLay and the finished active layer ActLay'.

The problem is that the available devices that are capable of performing such a process, known as hybrid bonding equipment, have only a limited handling capacity, more precisely a limited vertical capacity. As long as the specifications of the integrated device do not require too many active layers to be stacked, the available device can effectively position and bond the components involved. However, recent applications require the stacking of so many active layers that the available devices are not sufficient.

It is thus necessary to circumvent this height limitation of the devices currently available. This is an application of the process described using Figures 7 to 10.

Process 300, performed n times, allows n active layers ActLay' to be integrated into and connected to a substrate Tmp, as illustrated in the upper part of Figure 9, where n is a positive integer. The lower parts of Figures 9 and 10 illustrate a process developed to overcome the limited vertical capacity.

During a cutting step 410 following the n implementations of process 300, the first stack StckLay comprising a plurality of n finished active layers ActLay' is cut in

such a manner as to form a plurality of semiconductor elements D.Elmnt each comprising an elementary portion Elmnt of the first stack StckLay, as illustrated in Figure 9. In Figure 9, the elementary portions Elmnt are shown still attached to their respective portions of the substrate Tmp, but it is understood that they may also be detached from the substrate portions by any conventional method deemed suitable by the practitioner.

During an integration step 430, a second stack StckEl1 of a first plurality of elementary portions Elmnt and a third stack StckEl2 of a second plurality of elementary portions Elmnt are integrated onto a control substrate ContSub, which may be equipped with a connection pad (not shown in Figure 10).

Two adjacent stacked elementary portions Elmnt of a second stack StckEl1 and a third stack StckEl2 are connected to each other via first electrically conductive balls uBimp1, the second stack StckEl1 and the third stack StckEl2 each being connected to the control substrate ContSub via second respective electrically conductive balls uBimp2. These electrically conductive balls are known as “solder balls”.

When forming the second stack StckEl1 and the third stack StckEl2, the elementary portions Elmnt are positioned one on top of the other by means of a second handling device different from the first positioning device. This handling device is designed to establish electrical connections between adjacent stacked elements using electrically conductive balls in a well known manner such as the “flip-chip” bonding process. The corresponding handling device is denoted by the term “flip-chip bonding equipment”. Devices of this type may have a greater vertical capacity than that of the first available handling device. Thus, the height limitation mentioned above can be overcome.

Further advantages of this process include faster and more economical implementation than other transfer processes for an active material layer or an equivalent active layer.

Figure 13 illustrates generic conventional approaches for integrating three-dimensional functional semiconductor layers into one another. These approaches comprise the formation of (i) a first stack comprising a first substrate Sub1, a first functional layer Func.Lay1 and a first oxide layer Ox1; (ii) a second stack comprising

a second substrate Sub2, a buried oxide layer BOX, a second functional layer Func.Lay2 and a second oxide layer Ox2; (iii) assembling the two stacks through their respective oxide layers Ox1 and Ox2; and (iv) removing the second substrate Sub2 and the layer BOX.

Step (iv) is particularly time-consuming (generally several hours) and requires time-consuming and costly treatment such as mechanochemical polishing and wet and/or dry etching to thin and remove the second substrate Sub2 and the layer BOX.

The conventional approach of Figure 13 also generally uses an oxide-copper hybrid bond, not just an oxide-oxide bond as described above.

In contrast, in the present invention, step (iv) is replaced with a simple and rapid light irradiation. In addition, cleaning of the materials remaining attached to the functional layer (ActLay), which relates to thinner material layers than in the conventional processes illustrated collectively in Figure 13, is also easier.

In addition, the process according to the invention enables very thin layers of functional material (ActMat) to be transferred and integrated to form the active layer. For example, it is possible to form and transfer an active material layer of less than 1 micrometre.

A typical application that might benefit from these advantages is the manufacture of digital memories. For such applications, active layers may be considered to necessarily have a thickness of 0.8 micrometre, with each finished active layer typically being 5 micrometres thick. Stacks of eight active materials, representing a thickness of 40 micrometres, are already in production. However, it is expected that several dozen layers, for example 64, will have to be stacked in years to come, which will be limited by the vertical constraints of hybrid bonding equipment. The process described herein allows the limitations imposed by hybrid bonding equipment to be overcome.

The figures in the present document are not necessarily to scale. Certain features and components may be represented in an exaggerated manner relative to other components or in a somewhat schematic form, and certain details of conventional elements may not be shown, for the sake of clarity and conciseness.

Needless to say, the invention is not limited to the embodiment described, and other embodiments may be used without departing from the scope of the invention as defined by the claims.

CLAIMS

1. Semiconductor substrate (Sub) designed to allow laser separation of an active material layer (ActMat), comprising:

- a support substrate (Sprt);
- an inorganic layer (Inorg) on the support substrate, the inorganic layer being formed from a material chosen from Al2O3, TiO2, WO3, La2O3, LaAlO3 and TiN;
- an electrically insulating layer (Ins) on the inorganic layer; and
- the active material layer (ActMat) on the electrically insulating layer, the active material layer being single-crystal.

2. Semiconductor substrate (Sub) according to Claim 1, in which:

- the support substrate (Sprt) is made of single-crystal silicon;
- the inorganic layer (Inorg) has a thickness of between 10 nm and 2 µm;
- the insulating layer (Ins) comprises silicon oxide and has a thickness of between 10 nm and 1 µm; and
- the active material layer (ActMat) is chosen from Si, SiGe, GaAs, SiC, GaN and PZT and has a thickness of between 5 nm and 2 µm.

3. Process (100) for manufacturing the semiconductor substrate (Sub) according to Claim 1 or 2, comprising the following steps:

- implanting (130) a light ion species (H+) through a top surface (T.Surf) of an active material donor substrate (Don) so as to form a fragile plane (Frgl) inside the active material donor substrate (Don);
- forming (140), in this order, the inorganic layer (Inorg) and the electrically insulating layer (Ins) on a surface of a support substrate (Sprt);
- bonding (150) of the top surface (T.Surf) of the active material donor substrate (Don) to a free surface (F.Surf) of the insulating layer (Ins); and
- cleaving (170) the active material donor substrate (Don) at the fragile plane (Frgl) so as to leave the active material layer (ActMat) attached to the support substrate (Sprt) via the insulating layer (Ins) and the inorganic layer (Inorg).

4. Process (200) for manufacturing an active layer (ActLay) for a semiconductor device, comprising the implementation of the process (100) for manufacturing the semiconductor substrate (Sub) according to Claim 3, also comprising the steps of:

- treating (210) the active material layer (ActMat) so as to form the active layer (ActLay); and

- separating (230) the active layer (ActLay) from the support substrate (Sprt) at the inorganic layer (Inorg) by irradiating the inorganic layer with infrared (IR) radiation.

5. Process (300) for manufacturing an active layer (ActLay), comprising the implementation of the process (100) for manufacturing the semiconductor substrate (Sub) according to Claim 3, also comprising the steps of:

- treating (310) the active material layer (ActMat) so as to form the active layer (ActLay);

- positioning and attaching (330) the connection pads (Pad) of the active layer (ActLay) to the connection pads (Pad) of a receiving substrate (Tmp);

- separating (350) the support substrate (Sprt) from the active layer (ActLay) at the inorganic layer (Inorg) by irradiating the inorganic layer with infrared (IR) radiation;

- cleaning (370) a surface of the active material layer (ActMat) opposite the receiving substrate (Tmp) after separation from the support substrate (Sprt); and

- after the cleaning step, treating (390) the active material layer so as to form a finished active layer (ActLay').

6. Process (200, 300) for manufacturing an active layer (ActLay), comprising the implementation of the process (100) for manufacturing the semiconductor substrate (Sub) according to Claim 3 in a first manufacturing unit (U1), also comprising the steps of:

- sending (Snd0, Snd1) the semiconductor substrate (Sub) to a second manufacturing unit (U2); and

- sending (Snd0, Snd2) to said second manufacturing unit (U2) information representative of the fact that the active material layer (ActMat) of the semiconductor substrate (Sub) is to be separated from the support substrate (Sprt) in a separation step involving irradiation of the inorganic layer (Inorg) with infrared (IR) radiation.

7. Process (200) for manufacturing an active layer (ActLay) for a semiconductor device, comprising the implementation of the process (200, 300) for manufacturing the active layer (ActLay) according to Claim 6, also comprising the steps of:

- treating (210) the active material layer (ActMat) so as to form the active layer (ActLay); and
- separating (230) the active layer (ActLay) from the support substrate (Sprt) at the inorganic layer (Inorg) by irradiating the inorganic layer with infrared (IR) radiation.

8. Process (300) for manufacturing an active layer (ActLay), comprising the implementation of the process (200, 300) for manufacturing the active layer (ActLay) according to Claim 6, also comprising the steps of:

- treating (310) the active material layer (ActMat) so as to form the active layer (ActLay);
- positioning and attaching (330) the connection pads (Pad) of the active layer (ActLay) to the connection pads (Pad) of a receiving substrate (Tmp);
- separating (350) the support substrate (Sprt) from the active layer (ActLay) at the inorganic layer (Inorg) by irradiating the inorganic layer with infrared (IR) radiation;
- cleaning (370) a surface of the active material layer (ActMat) opposite the receiving substrate (Tmp) after separation from the support substrate (Sprt); and
- after the cleaning step, treating (390) the active material layer so as to form a finished active layer (ActLay').

9. Process according to any one of Claims 4 to 8 for manufacturing an active layer (ActLay), in which the active layer comprises a layer of semiconductor material with a thickness of less than 1 micrometre.

10. Process for forming a three-dimensional integrated semiconductor device (3D SC), which involves reiterating (380) the process (300) according to Claim 8 or 9 on the same portion of the same receiving substrate so as to form a first stack (StckLay) consisting of a plurality of stacked active layers (ActLay), one of the active material

layers (ActMat) intended to be stacked on a previously obtained active layer (ActLay) being positioned thereon by means of a first handling device.

11. Process according to Claim 10, also comprising the steps of:

- cutting (410) the first stack so as to form a plurality of semiconductor elements (D.Elmnt) each comprising an elementary portion (Elmnt) of the first stack (StckLay);
- on a control substrate (ContSub), forming (430) a second stack (StckEl1) of a plurality of elementary portions (Elmnt), two adjacent stacked elementary portions (Elmnt) of the second stack (StckEl1) being connected to each other by first electrically conductive balls (uBimp1), the second stack (StckEl1) being connected to the control substrate (ContSub) by second electrically conductive balls (uBimp2),

in which, when forming the second stack (StckEl1), the elementary portions (Elmnt) are positioned one on top of the other by means of a second handling device different from the first handling device.

12. Process according to Claim 11, in which the first handling device and the second handling device have a first height limit and a second height limit for the objects they can position, respectively, the first height limit being smaller than the second height limit.

13. Process according to Claim 11 or 12, in which the first handling device is hybrid bonding equipment and the second handling device is flip-chip bonding equipment.

14. Process according to one of Claims 10 to 13, in which the three-dimensional integrated semiconductor device is a memory device, each elementary portion (Elmnt) of the first stack (StckLay) being a digital memory element.