DOUBLE ANNEAL WITH IMPROVED RELIABILITY FOR DUAL CONTACT ETCH STOP LINER SCHEME

Abstract

A method for forming a device with both PFET and NFET transistors using a PFET compressive etch stop liner and a NFET tensile etch stop liner and two anneals in a deuterium containing atmosphere. The method comprises: providing a NFET transistor in a NFET region and a PFET transistor in a PFET region. We form a NFET tensile contact etch-stop liner over the NFET region. Then we perform a first deuterium anneal. We form a PFET compressive etch stop liner over the PFET region. We form a (ILD) dielectric layer with contact openings over the substrate. We perform a second deuterium anneal. The temperature of the second deuterium anneal is less than the temperature of the first deuterium anneal.

Figure 8