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DESCRIPTION

LEVEL SHIFT CIRCUIT, DISPLAY APPARATUS, AND PORTABLE

5 TERMINAL

Technical Field

The present invention relates to a level shift circuit,
a display apparatus, and a portable terminal. Particularly,
10 the present invention relates to a level shift circuit
formed on an insulating substrate using transistors with
large characteristic variations, a display apparatus using
the level shift circuit as a peripheral driving circuit, and
a portable terminal including the display apparatus as a
15 screen display unit.

Background Art

An example structure of a level shift circuit of the
related art is shown in Fig. 9. The level shift circuit in
20 this example level-shifts (level-converts) an input signal
IN with a low voltage amplitude of, for example, 3.3 V to a
signal with a high voltage amplitude of, for example, 6.5 V.
As is apparent from Fig. 9, the level shift circuit includes
two bias shift units 101 and 102, a level shift unit 103,
25 and an output unit 104.

If the level shift circuit of this type is formed of transistors with large characteristic variations, for example, TFTs (Thin Film Transistors), in addition to the input signal IN, a reverse-phase signal XIN of the input
5 signal IN must be input in order to reliably activate the circuit. Alternately, in place of the reverse-phase signal XIN, a reference potential Ref having an intermediate level of the amplitude of the input signal IN must be input. The input signals IN and XIN (or Ref) must be input directly to
10 a source of the input stage of the level shift unit 103.

As described above, in the structure in which, in addition to the input signal IN, the reverse-phase signal XIN is externally input, an external IC is required for generating the reverse-phase signal XIN based on the input
15 signal IN, and the number of input signal terminals required for the level shift circuit is two. On the other hand, in the structure in which the reference potential Ref is input, an external Ref power supply is required.

If the externally input signals IN and XIN (or Ref) are
20 input directly to the source of the input stage of the level shift unit 103, a current flows in an external input terminal, thus causing overcurrent into the external IC when the power supply is turned on or the like. This may induce latchup on the external IC.

25 The present invention has been made in view of the

foregoing problems, and it is an object of the present invention to provide a level shift circuit which can reliably level-shift a single-phase input signal when it is formed of transistors with large characteristic variations,
5 a display apparatus using the level shift circuit, and a portable terminal including the display apparatus as a screen display unit.

Disclosure of Invention

10 A level shift circuit of the present invention is formed on an insulating substrate, and includes a complementary generator unit driven by a first power supply having an amplitude voltage equal to an amplitude voltage of a signal input from the outside of the substrate for
15 generating a complementary signal from the single-phase input signal, and a level shift unit driven by a second power supply having a higher voltage than the first power supply for shifting the level of the complementary signal. The level shift circuit is used for a display apparatus
20 having a level shift circuit formed on the same transparent insulating substrate on which a display unit is formed for shifting the level of an input signal from the outside of the substrate so as to drive the display unit, and is used as this level shift circuit. The display apparatus using
25 such a level shift circuit is disposed on a portable

terminal, such as a PDA (Personal Digital Assistants) or a cellular phone, as a screen display unit thereof.

A circuit formed on an insulating substrate, such as a glass substrate, using transistors with large characteristic variations, for example, TFTs, exhibits lower TFT characteristics than that formed on a silicon substrate. Thus, a level shift circuit is required for shifting the level of an input signal to a high voltage amplitude. In a case where the level shift circuit is formed on the insulating substrate, when a single-phase signal is input from the outside of the substrate to the level shift circuit, a complementary generator unit of the level shift circuit formed on the substrate generates complementary signal from the single-phase signal, and supplies it to a level shift unit. The level shift unit level-shifts the complementary signal from low voltage amplitude to high voltage amplitude.

Brief Description of the Drawings

Fig. 1 is a circuit diagram showing an example structure of a level shift circuit according to a first embodiment of the present invention.

Fig. 2 is a timing chart showing the circuit operation of the level shift circuit according to the first embodiment.

Fig. 3 is a circuit diagram showing an example

structure of a level shift circuit according to a second embodiment of the present invention.

Fig. 4 is a timing chart showing the circuit operation of the level shift circuit according to the second

5 embodiment.

Fig. 5 is a block diagram showing an example structure of a liquid crystal display apparatus according to the present invention.

Fig. 6 is a circuit diagram showing an example of the
10 pixel structure.

Fig. 7 is a block diagram showing a specific example of the internal structure of an interface circuit.

Fig. 8 is an external view schematically showing the structure of a PDA according to the present invention.

15 Fig. 9 is a circuit diagram showing an example structure of a level shift circuit of the related art.

Best Mode for Carrying Out the Invention

Embodiments of the present invention are described
20 hereinbelow in detail with reference to the drawings.

[First Embodiment]

Fig. 1 is a circuit diagram showing an example structure of a level shift circuit according to a first embodiment of the present invention. It is assumed that the
25 level shift circuit according to this embodiment is formed

on an insulating substrate, such as a glass substrate, using transistors with large characteristic variations, for example, TFTs with high thresholds V_{th} . As is apparent from Fig. 1, the level shift circuit according to this embodiment includes a complementary generator unit 11, two bias shift units 12 and 13, a level shift unit 14, and an output unit 15. These units are formed on the insulating substrate using TFTs.

The level shift circuit has a ground (GND) terminal 16, a circuit input terminal 17, two power supply terminals 18 and 19, and a circuit output terminal 20. A first power supply voltage V_{CC} equal to the amplitude voltage (for example, 3.3 V) of a signal input from the outside of the substrate is applied to the power supply terminal 18. A second power supply voltage V_{DD} (for example, 6.5 V) higher than the first power supply voltage V_{CC} is applied to the power supply terminal 19.

The complementary generator unit 11 is formed of two cascaded inverters, for example, a first CMOS inverter having a PMOS transistor Q_{p11} and an NMOS transistor Q_{n11} connected in series between a V_{CC} power-supply line (hereinafter referred to as a V_{CC} line) and a GND line, each having a gate connected with the circuit input terminal 17, and a second CMOS inverter having a PMOS transistor Q_{p12} and an NMOS transistor Q_{n12} connected in series between the V_{CC}

line and the GND line, each having a gate connected with the common drain node of the MOS transistors Qp11 and Qn11.

In the complementary generator unit 11, when an input signal IN is input to the circuit input terminal 17, a
5 reverse-phase signal XIN of the input signal IN is output from the output end of the first CMOS inverter, i.e., the common drain node of the MOS transistors Qp11 and Qn11, and a signal IN that is in-phase with the input signal IN is output from the output end of the second CMOS inverter, i.e.,
10 the common drain node of the MOS transistors Qp12 and Qn12. In other words, the complementary generator unit 11 is driven by the first power supply voltage VCC, which is equal to the amplitude voltage of a signal input from the outside of the substrate, to generate the complementary signals IN
15 and XIN from the input signal IN.

The bias shift unit 12 is formed of PMOS transistors Qp13 and Qp14 connected in series between a VDD power-supply line (hereinafter referred to as a VDD line) and the GND line. A gate of the MOS transistor Qp13 is connected with
20 the GND line, and a gate of the MOS transistor Qp14 is connected with a signal line (hereinafter referred to as an IN line) for carrying the in-phase signal of the input signal IN. The bias shift unit 12 shifts a DC bias of the in-phase signal IN.

25 The bias shift unit 13 is formed of PMOS transistors

Qp15 and Qp16 connected in series between the VDD line and the GND line. A gate of the MOS transistor Qp15 is connected with the GND line, and a gate of the MOS transistor Qp16 is connected with a signal line (hereinafter referred to as an XIN line) for carrying the reverse-phase signal XIN of the input signal IN. The bias shift unit 13 shifts a DC bias of the reverse-phase signal XIN.

The level shift unit 14 includes two PMOS transistors Qp17 and Qp18, and four NMOS transistors Qn13 through Qn16.

The two PMOS transistors Qp17 and Qp18 have sources connected with the VDD line and gates commonly connected, and the gate and drain of the MOS transistor Qp17 are connected, thereby forming a current mirror circuit.

The NMOS transistor Qn13 has a drain connected with the drain of the PMOS transistor Qp17, a gate connected with the output end of the bias shift unit 12, i.e., the drain-source common node of the PMOS transistors Qp13 and Qp14, and a source connected with the XIN line. The NMOS transistor Qn14 has a drain connected with a drain of the PMOS transistor Qp18, a gate connected with the output end of the bias shift unit 13, i.e., the drain-source common node of the PMOS transistors Qp15 and Qp16, and a source connected with the IN line.

The NMOS transistor Qn15 has a drain connected with the output end of the bias shift unit 13, a gate connected with

the output end of the bias shift unit 12, and a source connected with the XIN line. The NMOS transistor Qn16 has a drain connected with the output end of the bias shift unit 12, a gate connected with the output end of the bias shift unit 13, and a source connected with the IN line. Therefore, the level shift unit 14 is formed of a source-input-type current mirror amp, that is, the reverse-phase signal XIN and the in-phase signal IN are input to the sources of the NMOS transistors Qn13 and Qn14 at the input stage, respectively.

The output unit 15 is formed of a first CMOS inverter having a PMOS transistor Qp19 and an NMOS transistor Qn19 connected in series between the VDD power-supply line and the GND line, each having a gate connected with the output end of the level shift unit 14, i.e., the common drain node of the MOS transistors Qp18 and Qn14, and a second CMOS inverter having a PMOS transistor Qp20 and an NMOS transistor Qn20 connected in series between the VDD line and the GND line, each having a gate connected with the common drain node of the MOS transistors Qp19 and Qn19.

The circuit operation of the level shift circuit according to the first embodiment having the above-described structure is described hereinbelow with reference to the timing chart shown in Fig. 2. In the following description, the input signal IN is a pulse signal, by way of example.

When a single-phase input pulse with 0 to 3.3 V amplitude is input via the circuit input terminal 17, the complementary generator unit 11 generates complementary (in-phase and reverse-phase) pulses of 0 V to 3.3 V from this input pulse. The generated complementary pulses, whose DC biases are shifted by the bias shift units 12 and 13 by certain voltages, are input to the gates of the NMOS transistors Qn13 and Qn14 of the level shift unit 14.

The complementary pulses, which have not been bias-shifted by the bias shift units 12 and 13, are crossed and input to the sources of the NMOS transistors Qn13 and Qn14. Specifically, the reverse-phase pulse, which has not been bias-shifted, is input to the source of the NMOS transistor Qn13 whose gate the bias-shifted in-phase pulse is input to. The in-phase pulse, which has not been bias-shifted, is input to the source of the NMOS transistor Qn14 whose gate the bias-shifted reverse-phase pulse is input to.

Accordingly, complementary pulses, which have not been bias-shifted, are crossed and input to the sources of the NMOS transistors Qn13 and Qn14 forming a current mirror amp, thus allowing rapid level shifting to a high voltage amplitude (in this example, 6.5 V) if the level shift circuit is formed of TFTs with large characteristic variations and high thresholds V_{th} . The level shift unit 14 has a structure in which the complementary pulses are input

directly to the sources; however, the D.C. currents flowing from the sources are supplied from the inverters of the complementary generator 11, resulting in no D.C. current flowing in an external clock line.

5 In the level shift unit 14 having such a current mirror amp, the complementary pulses with 0 to 3.3 V amplitude are level-shifted to pulses with 0 to 6.5 V amplitude, and are then output as a single-phase output pulse OUT that is in-phase with the input pulse IN from the circuit output
10 terminal 20 via the output unit 15.

As described above, a level shift circuit formed on an insulating substrate, such as a glass substrate, using transistors with large characteristic variations, for example, TFTs with high thresholds V_{th} , is provided with the
15 complementary generator unit 11 driven by a first power supply (VCC) having an amplitude voltage equal to the amplitude voltage of a signal input from the outside of the substrate to generate complementary signals from a single-phase input signal IN, and it is therefore no longer
20 necessary to externally input a reverse-phase signal XIN. Thus, no external IC is required for generating the reverse-phase signal XIN based on the input signal IN, and one terminal of the level shift circuit can be eliminated.

Moreover, the input signal IN is not input directly
25 from the outside to the sources of the source-input level

shift unit 14, but is received by the inverters of the complementary generator unit 11 so as to convert the signal into complementary signals, which are then input thereto.

This results in no D.C. current flowing in the input

5 terminal 17, and eliminates the danger of flowing overcurrent into an external signal line, which carries the input signal IN, when the power supply is turned on or the like.

Since the level shift circuit according to this
10 embodiment uses the level shift unit 14 of the source input type, some circuit delay can occur. However, this level shift circuit is able to level-shift the input signal IN and output it as the output signal OUT in real time, thus achieving very high operation speed. This is suitable for
15 level-shifting high-operation-frequency clock signals.

In a case where a circuit is formed on a silicon substrate using TFTs, a signal of a low voltage amplitude (in this example, 0 to 3.3 V) is sufficient to drive the circuit. Therefore, a level shift circuit for level-
20 shifting the input signal to a high voltage amplitude is not necessary. On the other hand, a circuit formed on an insulating substrate, such as a glass substrate, using TFTs exhibits lower TFT characteristics than that formed on a silicon substrate. Such a circuit must therefore include a
25 level shift circuit for level-shifting the input signal to a

high voltage amplitude in order to correctly activate the circuit. The level shift circuit according to this embodiment is suitable as such a level shift circuit formed on an insulating substrate using TFTs.

5 [Second Embodiment]

Fig. 3 is a circuit diagram showing an example structure of a level shift circuit according to a second embodiment of the present invention. It is assumed that the level shift circuit according to this embodiment is formed
10 on an insulating substrate, such as a glass substrate, using transistors with large characteristic variations, for example, TFTs with high thresholds V_{th} , like the level shift circuit according to the first embodiment. As is apparent from Fig. 3, the level shift circuit according to this
15 embodiment includes a complementary generator unit 21, a first latch unit 22, and a second latch unit 23. These units are formed on the insulating substrate using TFTs.

The level shift circuit has a control terminal 24, a ground (GND) terminal 25, a circuit input terminal 26, two
20 power supply terminals 27 and 28, and a circuit output terminal 29. A sampling pulse SP is input from the outside of the substrate to the control terminal 24. A first power supply voltage VCC equal to the amplitude voltage (for example, 3.3 V) of a signal input from the outside of the
25 substrate is applied to the power supply terminal 27. A

second power supply voltage VDD (for example, 6.5 V) higher than the first power supply voltage VCC is applied to the power supply terminal 28.

The complementary generator unit 21 is formed of two
5 cascaded inverters, for example, a first CMOS inverter having a PMOS transistor Qp21 and an NMOS transistor Qn21 connected in series between a VCC line and a GND line, each having a gate connected with the circuit input terminal 26, and a second CMOS inverter having a PMOS transistor Qp22 and
10 an NMOS transistor Qn22 connected in series between the VCC line and the GND line, each having a gate connected with the common drain node of the MOS transistors Qp21 and Qn21.

In the complementary generator unit 21, when an input signal IN is input to the circuit input terminal 26, a
15 reverse-phase signal XIN of the input signal IN is output from the output end of the first CMOS inverter, i.e., the common drain node of the MOS transistors Qp21 and Qn21, and a signal IN that is in-phase with the input signal IN is output from the output end of the second CMOS inverter, i.e.,
20 the common drain node of the MOS transistors Qp22 and Qn22. In other words, the complementary generator unit 21 is driven by the first power supply voltage VCC, which is equal to the amplitude voltage of an signal input from the outside of the substrate, to generate the complementary signals IN
25 and XIN from the input signal IN.

The first latch unit 22 is formed of a CMOS inverter 221, a CMOS latch cell 222, and an inverter circuit 223. The CMOS inverter 221 is formed of a PMOS transistor Qp23 and an NMOS transistor Qn23 connected in series between a VDD line and the GND line, gates thereof being commonly connected. The CMOS inverter 221 inverts the sampling pulse SP with 0 to 3.3 V amplitude input via the control terminal 24, and also level-shifts it to a sampling pulse SP with 6.5 to 0 V amplitude.

The CMOS latch cell 222 includes a first CMOS inverter having a PMOS transistor Qp24 and an NMOS transistor Qn24 connected in series, gates thereof being commonly connected, and a second CMOS inverter having a PMOS transistor Qp25 and an NMOS transistor Qn25 connected in series, gates thereof being commonly connected. The input and output ends of these CMOS inverters are cross-connected.

More specifically, the input end of the first CMOS inverter, i.e., the common gate node of the MOS transistors Qp24 and Qn24, is connected with the output end of the second CMOS inverter, i.e., the common drain node of the MOS transistors Qp25 and Qn25, and the input end of the second CMOS inverter, i.e., the common gate node of the MOS transistors Qp25 and Qn25 is connected with the output end of the first CMOS inverter, i.e., the common drain node of the MOS transistors Qp24 and Qn24.

A PMOS transistor Qp26 is connected between the power-supply side of the CMOS latch cell 222 and the VDD line. The PMOS transistor Qp26 is turned on for a low-level period of the sampling pulse SP input via the control terminal 24 to supply the power supply voltage VDD to the CMOS latch cell 222, and is turned off for a high-level period of the sampling pulse SP to interrupt the supply of the power supply voltage VDD to the CMOS latch cell 222. Therefore, the latch unit 22 of the sampling latch type is constructed as a level shift unit.

An NMOS transistor Qn26 is connected between the input end of the first CMOS inverter of the CMOS latch cell 222 and the output end of the second CMOS inverter of the complementary generator unit 21, and an NMOS transistor Qn27 is connected between the input end of the second CMOS inverter of the CMOS latch cell 222 and the output end of the first CMOS inverter of the complementary generator unit 21. The NMOS transistors Qn26 and Qn27 are turned on for the high-level period of the sampling pulse SP to sample the complementary signals, that is, the in-phase signal and the reverse-phase signal, and supply them to the CMOS latch cell 222.

The inverter circuit 223 is formed of a first CMOS inverter having a PMOS transistor Qp28 and an NMOS transistor Qn28 connected in series, gates thereof being

commonly connected, and a second CMOS inverter having a PMOS transistor Qp29 and an NMOS transistor Qn29 connected in series, gates thereof being commonly connected. The inverter circuit 223 is driven by the power supply voltage
5 VDD which is supplied via the PMOS transistor Qp26.

In the inverter circuit 223, the input ends of the first and second CMOS inverters, i.e., the common gate node of the MOS transistors Qp28 and Qn28 and the common gate node of the MOS transistors Qp29 and Qn29, are connected
10 with the output ends of the first and second CMOS inverters of the CMOS latch cell 222, respectively. The output ends of the first and second CMOS inverters, i.e., the common drain node of the MOS transistors Qp28 and Qn28 and the common drain node of the MOS transistors Qp29 and Qn29, are
15 connected with drains of NMOS transistors Qn30 and Qn31, respectively. The NMOS transistors Qn30 and Qn31 are turned on for a high-level period of the sampling pulse SP level-shifted by the CMOS inverter 221 to transmit the complementary signals latched in the CMOS latch cell 222 to
20 the subsequent second latch unit 23.

The second latch unit 23 is formed of a CMOS latch 231 and a CMOS inverter 232. The CMOS latch 231 has a first CMOS inverter having a PMOS transistor Qp32 and an NMOS transistor Qn32 connected in series between the VDD line and
25 the GND line, gates thereof being commonly connected, and a

second CMOS inverter having a PMOS transistor Qp33 and an NMOS transistor Qn33 connected in series between the VDD line and the GND line, gates thereof being commonly connected. The input and output ends of these CMOS

5 inverters are cross-connected.

More specifically, the input end of the first CMOS inverter, i.e., the common gate node of the MOS transistors Qp32 and Qn32, is connected with the output end of the second CMOS inverter, i.e., the common drain node of the MOS
10 transistors Qp33 and Qn33, and the input end of the second CMOS inverter, i.e., the common gate node of the MOS transistors Qp33 and Qn33, is connected with the output end of the first CMOS inverter, i.e., the common drain node of the MOS transistors Qp32 and Qn32. The input ends of the
15 first and second CMOS inverters are connected with the sources of the NMOS transistors Qn30 and Qn31 of the first latch unit 22, respectively.

The CMOS inverter 232 is formed of a PMOS transistor Qp34 and an NMOS transistor Qn34 connected in series between
20 the VDD line and the GND line, gates thereof being commonly connected. The input end of the CMOS inverter 232, i.e., the common gate node of the MOS transistors Qp34 and Qn34, is connected with the output end of the first CMOS inverter of the CMOS latch 231, and the output end of the CMOS
25 inverter 232, i.e., the common drain node of the MOS

transistors Qp34 and Qn34, is connected with the circuit output terminal 29.

The circuit operation of the level shift circuit according to the second embodiment having the above-described structure is described hereinbelow with reference to the timing chart shown in Fig. 4. In the following description, the input signal IN is a pulse signal, by way of example.

When a single-phase input pulse with 0 to 3.3 V amplitude is input via the circuit input terminal 26, the complementary generator unit 21 generates complementary (in-phase or reverse-phase) pulses of 0 V to 3.3 V from this input pulse. The generated complementary pulses are sampled by turning on the NMOS transistors Qn26 and Qn27 for the high-level period of the sampling pulse SP input via the control terminal 24, and are then input to the CMOS latch cell 222 of the second latch unit 22.

When the sampling pulse SP becomes low, the NMOS transistors Qn26 and Qn27 are turned off to interrupt the input of the complementary pulses to the CMOS latch cell 222. At the same time, the PMOS transistor 26 is turned on to supply the power supply voltage VDD to the CMOS latch cell 222. The first latch unit 22, namely, the CMOS latch cell 222, stores (latches) the data at the time when the sampling pulse SP becomes low.

In the same period, the sampling pulse SP inverted by the CMOS inverter 221 becomes high, and the NMOS transistors Qn30 and Qn31 of the first latch unit 22 are turned on, so that the data latched in the CMOS latch cell 222 is
5 transmitted to the second latch unit 23 and is also written to the CMOS latch cell 231. The written data is still stored in the CMOS latch cell 231 for a period in which the first latch unit 22 latches the next data. The latched data is inverted by the CMOS inverter 232, and is then output as
10 a single-phase output pulse OUT that is in-phase with the input pulse IN from the circuit output terminal 29.

As described above, a level shift circuit formed on an insulating substrate, such as a glass substrate, using transistors with large characteristic variations, for
15 example, TFTs with high thresholds V_{th} , is provided with the complementary generator unit 21 driven by a first power supply (VCC) having an amplitude voltage equal to the amplitude voltage of a signal input from the outside of the substrate to generate complementary signals from a single-
20 phase input signal IN, thus achieving similar advantages to the first embodiment.

Specifically, it is no longer necessary to input a reverse-phase signal XIN from the outside of the substrate. Thus, no external IC is required for generating the reverse-
25 phase signal XIN based on the input signal IN, and one

terminal of the level shift circuit can be eliminated.

Moreover, the input signal IN is not input directly from the outside to the first latch unit 22, but is received by the inverters of the complementary generator unit 21 so as to

5 convert the signal into complementary signals, which are then input thereto. This results in no D.C. current flowing in the input terminal 26, and eliminates the danger of flowing overcurrent into an external signal line, which carries the input signal IN, when the power supply is turned
10 on or the like.

In the level shift circuit according to this embodiment, basically, the level shift unit is implemented by a sampling-latch-type latch circuit, which does not cause a D.C. current to flow constantly, unlike the level shift
15 circuit according to the first embodiment, thus reducing the power consumption. The level shift circuit according to this embodiment is therefore suitable for the purpose of low power consumption.

In the foregoing embodiments, each of the complementary
20 generator units 11 and 21 is formed of two cascaded inverters, by way of example. The merit of this structure is that a D.C. current is not caused to flow in the input terminal 117 or 26. However, the complementary generator unit 11 or 21 is not necessarily formed of two inverters as
25 long as it can generate complementary signals from a single-

phase input signal, and may be formed of a single inverter in which complementary signals can be obtained from the input side and output side of this inverter.

The level shift circuits according to the above-
5 described first and second embodiments can be used as, for example, level shift circuits for use in an integrated-driving-circuit display apparatus having peripheral driving circuits integrally formed on the same transparent insulating substrate on which a display unit having a matrix
10 of pixels is formed for level-shifting a low-voltage-amplitude signal input from the outside of the substrate to a high-voltage-amplitude signal.

[Application Examples]

Fig. 5 is a block diagram showing an example structure
15 of a display apparatus according to the present invention, for example, a liquid crystal display apparatus. In Fig. 5, a display unit (pixel unit) 32 having a matrix of pixels is formed on a transparent insulating substrate, for example, a glass substrate 31. The glass substrate 31 faces another
20 glass substrate with a predetermined spacing therebetween, and a liquid crystal material is disposed between both substrates, thereby forming a display panel (an LCD panel).

An example of the pixel structure of the display unit 32 is shown in Fig. 6. Each of the pixels 50 arranged into
25 a matrix includes a TFT (Thin Film Transistor) 51 serving as

a pixel transistor, a liquid crystal cell 52 having a pixel electrode connected with a drain electrode of the TFT 51, and a storage capacitor 53 having one electrode connected with the drain electrode of the TFT 51. The liquid crystal
5 cell 52 means the liquid crystal capacitance generated between the pixel electrode and a counter electrode thereof.

In this pixel structure, the TFT 51 has a gate electrode connected with a gate line (scanning line) 54, and a source electrode connected with a data line (signal line)
10 55. The counter electrode of the liquid crystal cell 52 is connected with a VCOM line 56, as is common to the pixels. A common voltage VCOM (VCOM potential) is applied to the counter electrode of the liquid crystal cell 52 via the VCOM line 56, as is common to the pixels. The other electrode
15 (the terminal on the counter electrode side) of the storage capacitor 53 is connected with a CS line 57, as is common to the pixels.

In a case where 1H (H indicates a horizontal period) inversion driving or 1F (F indicates a field period)
20 inversion driving is performed, a display signal to be written to each pixel is polarity-inverted based on the VCOM potential. In a case where VCOM inversion driving in which the polarity of the VCOM potential is inverted every 1H or 1F is performed in combination with 1H inversion driving or
25 1F inversion driving, the polarity of the CS potential

applied to the CS line 57 is also inverted in synchronization with the VCOM potential. However, the liquid crystal display apparatus according to this embodiment is not limited to VCOM inversion driving.

5 Referring again to Fig. 5, formed on the same glass substrate 31 on which the display unit 32 is formed are, for example, an interface (IF) circuit 33, a timing generator (TG) 34, and a reference voltage driver 35 on the left of the display unit 32; a horizontal driver 36 on the upper
10 side of the display unit 32; a vertical driver 37 on the right of the display unit 32; and a CS driver 38 and a VCOM driver 39 on the lower side of the display unit 32. These peripheral driving circuits and the pixel transistors of the display unit 32 are made of low-temperature polysilicon or
15 CG (Continuous Grain) silicon.

In the liquid crystal display apparatus having the above-described structure, a low-voltage-amplitude (for example, 3.3-volt-amplitude) master clock MCK, horizontal synchronous pulse Hsync, vertical synchronous pulse Vsync,
20 and R (red), G (green), and B (blue) parallel-input display data Data are externally input to the glass substrate 31 via a flexible cable (substrate) 40, and are level-shifted (level-converted) by the interface circuit 33 to high-voltage-amplitude (for example, 6.5-volt) signals.

25 The level-shifted master clock MCK, horizontal

synchronous pulse Hsync, and vertical synchronous pulse Vsync are supplied to the timing generator 34. The timing generator 34 generates various timing pulses necessary for driving the reference voltage driver 35, the horizontal driver 36, the vertical driver 37, the CS driver 38, and the VCOM driver 39 based on the master clock MCK, the horizontal synchronous pulse Hsync, and the vertical synchronous pulse Vsync. The level-shifted display data Data is supplied to the horizontal driver 36.

The horizontal driver 36 includes, for example, a horizontal shift register 361, a data sampling latch circuit 362, and a DA (digital-to-analog) converter circuit (DAC) 363. The horizontal shift register 361 starts a shift operation in response to a horizontal start pulse HST supplied from the timing generator 34, and generates sampling pulses, which is sequentially transferred in one horizontal period in synchronization with a horizontal clock pulse HCK also supplied from the timing generator 34.

In synchronization with the sampling pulses generated by the horizontal shift register 361, the data sampling latch circuit 362 sequentially samples and latches the display data Data output from the interface circuit 33 in one horizontal period. The latched digital data corresponding to one line is further transferred to a line memory (not shown) in a horizontal blanking period. The

digital data corresponding to one line is converted by the DA converter circuit 363 into an analog display signal.

The DA converter circuit 363 is, for example, a reference-voltage-selection-type DA converter circuit for selecting a reference voltage corresponding to the digital data from reference voltages corresponding to the number of grayscales supplied from the reference voltage driver 35 and for outputting the selected voltage as an analog display signal. An analog display signal Sig corresponding to one line output from the DA converter circuit 363 is output to data lines 55-1 to 55-n corresponding to n horizontal pixels of the display unit 32.

The vertical driver 37 is formed of a vertical shift register and a gate buffer. In the vertical driver 37, the vertical shift register starts a shift operation in response to a vertical start pulse VST supplied from the timing generator 34, and generates scanning pulses to be sequentially transferred in one vertical period in synchronization with a vertical clock pulse VCK also supplied from the timing generator 34. The generated scanning pulses are sequentially output via the gate buffer to gate lines 54-1 to 54-m corresponding to m vertical pixels of the display unit 32.

When the scanning pulses are sequentially output to the gate lines 54-1 to 54-m by vertical scanning of the vertical

driver 37, the pixels of the display unit 32 are selected row-by-row (line-by-line) in turn. The analog display signal Sig corresponding to one line output from the DA converter circuit 363 is written at the same time to the
5 selected pixels corresponding to one line via the data lines 55-1 to 55-n. This line-by-line writing operation is repeated, thus allowing an image of one screen to be displayed.

The CS driver 38 generates the above-described CS
10 potential, and applies it to the other electrode of the storage capacitor 53 via the CS line 57 shown in Fig. 6, as is common to the pixels. Given that the amplitude of the display signals is, for example, 0 to 3.3 V, the CS potential is inverted alternately between 0 V (ground level)
15 as the minimum level and 3.3 V as the maximum level in a case where VCOM inversion driving is performed.

The VCOM driver 39 generates the above-described VCOM potential. The VCOM potential output from the VCOM driver 39 is once output to the outside of the glass substrate 31
20 via the flexible cable 40. The VCOM potential output to the outside passes through a VCOM adjusting circuit 41, and is again input to the glass substrate 31 via the flexible cable 40. The input VCOM potential is applied to the counter electrode of the liquid crystal cell 52 via the VCOM line 56
25 shown in Fig. 6, as is common to the pixels.

As used herein, the VCOM potential is an A.C. voltage having substantially the same amplitude as the CS potential. In practical use, however, a voltage drop occurs in the TFT 51 shown in Fig. 6 due to parasitic capacitance or the like
5 when the signal is written to the pixel electrode of the liquid crystal cell 52 from the gate line 54 via the TFT 51, and the VCOM potential must be an A.C. voltage which is DC shifted by the amount of voltage drop. The VCOM potential is DC shifted by the VCOM adjusting circuit 41.

10 The VCOM adjusting circuit 41 is formed of a capacitor C to which the VCOM potential is input, a variable resistor VR connected between the output end of the capacitor C and an external power supply VCC, and a resistor R connected between the output end of the capacitor C and a ground. The
15 VCOM adjusting circuit 41 adjusts the DC level of the VCOM potential applied to the counter electrode of the liquid crystal cell 52, that is, a DC offset is added to the VCOM potential.

In the liquid crystal display apparatus having the
20 above-described structure, the horizontal driver 36 and the vertical driver 37, as well as peripheral driving circuits, such as the interface circuit 33, the timing generator 34, the reference voltage driver 35, the CS driver 38, and the VCOM driver 39, are integrally formed on the same panel (the
25 glass substrate 31) on which the display unit 32 is formed.

Therefore, a display panel with all the driving circuits integrated can be constructed without any external substrate, IC, or transistor circuit, thus reducing the size and cost of the overall system.

5 In the integrated-driving-circuit liquid crystal display apparatus, level shift circuits forming the interface circuit 33 are implemented by the level shift circuits according to the first and second embodiments. As described above, the master clock MCK, the horizontal
10 synchronous pulse Hsync, the vertical synchronous pulse Vsync, and the R (red), G (green), and B (blue) parallel-input display data Data are input from the outside of the substrate to the interface circuit 33. Where one color is represented by, for example, 6 bits, the display data Data
15 is 18-bit data (= 6 bits $\times$ 3).

 Fig. 7 shows a specific example of the internal structure of the interface circuit 33. The interface circuit 33 in this example includes 21 input level shift (LS) circuits 42-1 to 42-21 corresponding to the externally
20 input master clock MCK, horizontal synchronous pulse Hsync, vertical synchronous pulse Vsync, and 18-bit display data Data. The input level shift circuits 42-1 to 42-21 are implemented by the level shift circuits according to the first and second embodiments. Since the level shift
25 circuits according to the first and second embodiments

support a single-phase input signal, a single-phase signal can be input to all of the input level shift circuits 42-1 to 42-21, thus greatly reducing the number of input terminals of the display panel.

5 The master clock MCK is a much-higher-frequency signal than any other signal of the low-voltage-amplitude (in this example, 0 V to 3.3 V) signals input from the outside of the substrate. It is preferable that the input level shift circuit 42-1 which level-shifts the master clock MCK be
10 implemented by the level shift circuit according to the first embodiment, that is, a source-input-type level shift circuit having a high operation speed. It is preferable that each of the input level shift circuits 42-2 to 42-21 which level-shift the remaining signals be implemented by
15 the level shift circuit according to the second embodiment, that is, a sampling-latch-type level shift circuit with low power consumption.

Accordingly, sampling-latch-type level shift circuits with low power consumption are used for the signals other
20 than the master clock MCK, i.e., the horizontal synchronous pulse Hsync, the vertical synchronous pulse Vsync, and the 18-bit display data Data. Therefore, the power consumption of the overall liquid crystal display apparatus can be reduced.

25 In the application example, a liquid crystal display

apparatus using liquid crystal cells as display elements is used, by way of example. However, the present invention is not limited to this application example, and may be

applicable to any display apparatus having a level shift

5 circuit formed on the same substrate on which a display unit is formed, such as an EL (electroluminescence) display apparatus using EL elements as display elements.

A display apparatus, such as the liquid crystal display apparatus in the above-described application example, is

10 suitably used as a screen display unit of small and light portable terminals, such as cellular phones and PDAs (Personal Digital Assistants).

Fig. 8 is an external view schematically showing the structure of a portable terminal according to the present

15 invention, for example, a PDA.

The PDA in this example has, for example, a folded structure in which a cover 62 is openable and closable with respect to a main body 61. An operation unit 63 having

various keys, such as a keyboard, is disposed on the top

20 surface of the main body 61. The cover 62 includes a screen display unit 64. The screen display unit 64 is implemented

by the liquid crystal display apparatus having the level shift circuits according to the first and second embodiments formed on the same substrate on which the display unit is

25 formed.

As described above, since the liquid crystal display apparatus using the level shift circuits according to the foregoing embodiments support a single-phase signal input from the outside of the substrate, no external circuit is required for generating a reverse-phase signal. Moreover, the number of input terminals of the display panel can be greatly reduced. The liquid crystal display apparatus is used as the screen display unit 64, thus making it possible to achieve the PDA with a simple overall structure and less wiring, which contributes to a reduction in size and cost.

Although an application to a PDA has been described, by way of example, the present invention is not limited to this application example. The liquid crystal display apparatus according to the present invention may be suitable for any small and light portable terminal, such as a cellular phone, in particular.

Industrial Applicability

According to the present invention, therefore, a level shift circuit formed on an insulating substrate using transistors with large characteristic variations is provided with a complementary generator unit driven by a first power supply having an amplitude voltage equal to the amplitude voltage of a signal input from the outside of the substrate to generate complementary signals from a single-phase input

signal. It is therefore no longer necessary to externally
input a reverse-phase signal. Thus, no external IC is
required for generating a reverse-phase signal of the
single-phase signal, and one terminal of the level shift
5 circuit can be eliminated. Moreover, the input signal is
not input directly from the outside, but is received by the
complementary generator unit so as to convert the signal
into complementary signals, which are then input. This
results in no D.C. current flowing in a signal input
10 terminal, and eliminates the danger of flowing overcurrent
into an external signal line, which carries the input signal,
when the power supply is turned on or the like.

CLAIMS

1. A level shift circuit formed on an insulating substrate, comprising:

5 a complementary generator unit driven by a first power supply having an amplitude voltage equal to an amplitude voltage of a signal input from the outside of the substrate for generating a complementary signal from the single-phase input signal; and

10 a level shift unit driven by a second power supply having a higher voltage than the first power supply for shifting the level of the complementary signal.

2. A level shift circuit according to claim 1, wherein the level shift unit includes a current mirror circuit, and has
15 a source-input circuit structure in which the complementary signal is input to sources of input-stage transistors of the current mirror circuit.

3. A level shift circuit according to claim 1, wherein the level shift unit has a sampling-latch circuit structure in
20 which the complementary signal is sampled in synchronization with a sampling pulse and is latched.

4. A display apparatus comprising:

 a display unit having a matrix of pixels formed on a transparent insulating substrate; and

25 a level shift circuit formed on the transparent

insulating substrate together with the display unit for shifting the level of an input signal from the outside of the substrate so as to drive the display unit,

wherein the level shift circuit includes:

- 5 a complementary generator unit driven by a first power supply having an amplitude voltage equal to an amplitude voltage of a signal input from the outside of the substrate for generating a complementary signal from a single-phase input signal; and
 - 10 a level shift unit driven by a second power supply having a higher voltage than the first power supply for shifting the level of the complementary signal.
5. A display apparatus according to claim 4, wherein the level shift unit includes a current mirror circuit, and has
- 15 a source-input circuit structure in which the complementary signal is input to sources of input-stage transistors of the current mirror circuit.
6. A display apparatus according to claim 4, wherein the level shift unit has a sampling-latch circuit structure in
- 20 which the complementary signal is sampled in synchronization with a sampling pulse and is latched.
7. A display apparatus according to claim 4, wherein the level shift unit uses a combination of a source-input-type level shift circuit and sampling-latch-type level shift
- 25 circuits for input signals including a master clock, a

horizontal synchronous pulse, a vertical synchronous pulse, and display data, and

the master clock is level-shifted by the source-input-type level shift circuit, and the horizontal synchronous pulse, the vertical synchronous pulse, and the display data are level-shifted by the sampling-latch-type level shift circuits.

8. A display apparatus according to claim 4, wherein the level shift circuit is formed on the transparent insulating substrate using low-temperature polysilicon or continuous grain silicon.

9. A portable terminal including a display apparatus as a screen display unit, the display apparatus comprising:

a display unit having a matrix of pixels formed on a transparent insulating substrate; and

a level shift circuit formed on the transparent insulating substrate together with the display unit for shifting the level of an input signal from the outside of the substrate so as to drive the display unit,

wherein the level shift circuit includes:

a complementary generator unit driven by a first power supply having an amplitude voltage equal to an amplitude voltage of a signal input from the outside of the substrate for generating a complementary signal from a single-phase input signal; and

a level shift unit driven by a second power supply having a higher voltage than the first power supply for shift the level of the complementary signal.