(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
13 March 2003 (13.03.2003)

PCT

(10) International Publication Number
WO 03/021661 A3

(51) International Patent Classification[7]: H01L 21/8242

(21) International Application Number: PCT/US02/25909

(22) International Filing Date: 13 August 2002 (13.08.2002)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
09/942,208 29 August 2001 (29.08.2001) US

(71) Applicant: **MOTOROLA, INC., A CORPORATION OF THE STATE OF DELAWARE** [US/US]; 1303 East Algonquin Road, Schaumburg, IL 60196 (US).

(72) Inventors: **ROBERTS, Douglas, R.**; 7608 Tisdale Drive, Austin, TX 78757 (US). **LUCKOWSKI, Eric,**; 3016 Flower Hill Drive, Round Rock, TX 78664 (US).

(74) Agents: **KOCH, William, E.**; Corporate Law Department, Intellectual Property Section, 7700 West Parmer Lane, MD: TX32/PL02, Austin, TX 78729 et al. (US).

(81) Designated States *(national)*: AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DZ, EC, EE, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, MZ, NO, NZ, OM, PH, PL, PT, RO, RU, SD, SE, SG, SI, SK, SL, TJ, TM, TN, TR, TT, TZ, UA, UG, UZ, VC, VN, YU, ZA, ZM, ZW.

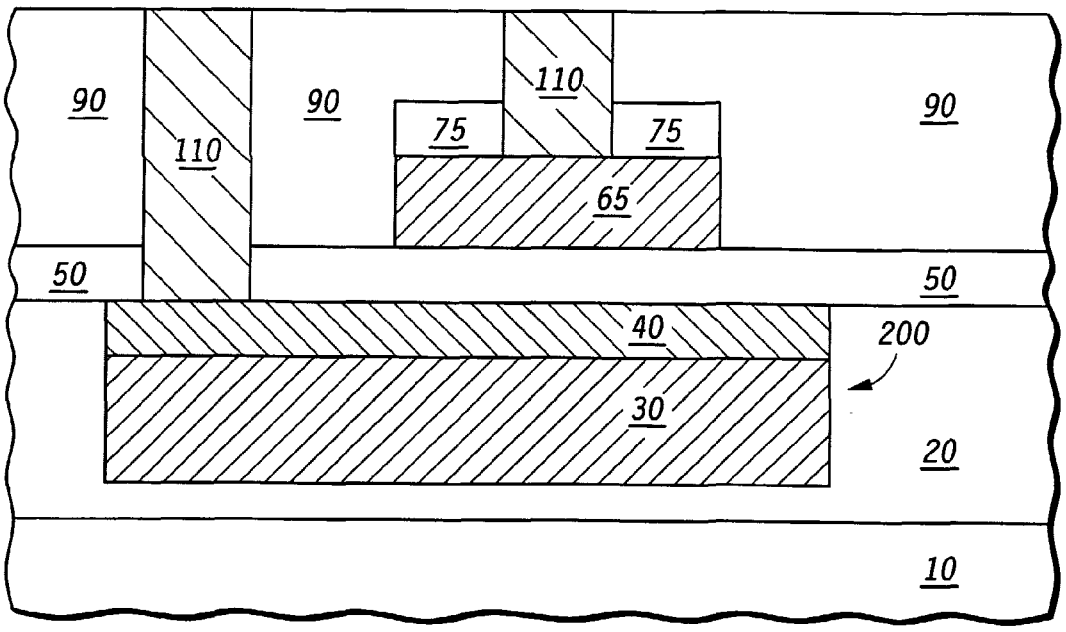
(84) Designated States *(regional)*: ARIPO patent (GH, GM, KE, LS, MW, MZ, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European patent (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE, SK, TR), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

Published:
— *with international search report*
— *with amended claims and statement*

(88) Date of publication of the international search report:
24 July 2003

[Continued on next page]

(54) Title: PROCESS FOR MAKING A MIM CAPACITOR



(57) Abstract: A process for forming a metal-insulator-metal (MIM) capacitor structure includes forming a recess in the dielectric layer (20) of a semiconductor substrate (10). A first capacitor electrode (30, 40) is formed in the recess having a copper first metal layer (30) with a conductive oxidation barrier (40) formed over the first metal layer (30). The first capacitor electrode (30, 40) is planarized relative to the dielectric layer (20). An insulator (50) is formed over the first capacitor electrode (30, 40) and a second capacitor electrode (65) is formed over the insulator (50). Forming the first capacitor electrode (30, 40) in the recess maintains the alignment of a periphery of the copper first metal layer (30) with the conductive oxidation barrier (40).

WO 03/021661 A3

Date of publication of the amended claims and statement:
12 September 2003

For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.